

1.1GHz Two-Modulus Prescaler

The MC12028A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1GHz in programmable frequency steps.

The MC12028B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 32/33 or 64/65 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- MC12028A for Positive Edge Triggered Synthesizers
- MC12028B for Negative Edge Triggered Synthesizers
- 6.5mA Maximum, -40° to +85°C, V_{CC} = 5.5Vdc
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL
- Low-Power 4.0mA Typical

FUNCTIONAL TABLE

| SW | MC | Divide Ratio |
|----|----|--------------|
| H | H | 32 |
| H | L | 33 |
| L | H | 64 |
| L | L | 65 |

Note: SW: H = V_{CC}, L = Open
MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V

DESIGN GUIDE

| Criteria | Value | Unit |
|---------------------------------|-------|------|
| Internal Gate Count* | 67 | ea |
| Internal Gate Propagation Delay | 200 | ps |
| Internal Gate Power Dissipation | 0.75 | mW |
| Speed Power Product | 0.15 | pJ |

* Equivalent to a two-input NAND gate

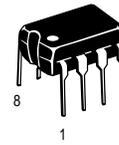
MAXIMUM RATINGS

| Symbol | Characteristic | Range | Unit |
|------------------|------------------------------|--------------|------|
| V _{CC} | Power Supply Voltage, Pin 2 | -0.5 to +7.0 | Vdc |
| T _A | Operating Temperature Range | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | -65 to +150 | °C |
| MC | Modulus Control Input, Pin 6 | -0.5 to +6.5 | Vdc |

MC12028A
MC12028B

MECL PLL COMPONENTS

÷32/33, ÷64/65
TWO-MODULUS
PRESCALER

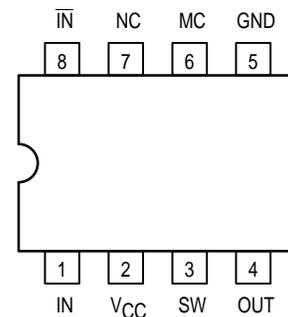


P SUFFIX
PLASTIC PACKAGE
CASE 626-05



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-05

Pinout: 8-Lead Plastic (Top View)



ELECTRICAL CHARACTERISTICS ($V_{CC} = 4.5$ to $5.5V \pm 10\%$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|-----------|--|-----------------|----------|-----------------|------------------|
| f_t | Toggle Frequency (Sine Wave Input) | 0.1 | 1.4 | 1.1 | GHz |
| I_{CC} | Supply Current Output Unloaded (Pin 2) | | 4.0 | 6.5 | mA |
| V_{IH1} | Modulus Control Input High (MC) | 2.0 | | | V |
| V_{IL1} | Modulus Control Input Low (MC) | | | 0.8 | V |
| V_{IH2} | Divide Ratio Control Input High (SW) | $V_{CC} - 0.5V$ | V_{CC} | $V_{CC} + 0.5V$ | Vdc |
| V_{IL2} | Divide Ratio Control Input Low (SW) | Open | Open | Open | — |
| V_{out} | Output Voltage Swing ($C_L = 12pF$; $R_L = 2.2k\Omega$) | 1.0 | 1.6 | | V _{p-p} |
| t_{set} | Modulus Setup Time MC to Out | | 11 | 16 | ns |
| V_{in} | Input Voltage Sensitivity 250–1100 MHz 100–250 MHz | 100 400 | | 1500 1500 | mVpp |
| I_O | Output Current ($C_L = 12pF$; $R_L = 2.2k\Omega$) | | | 0.2 | mA |

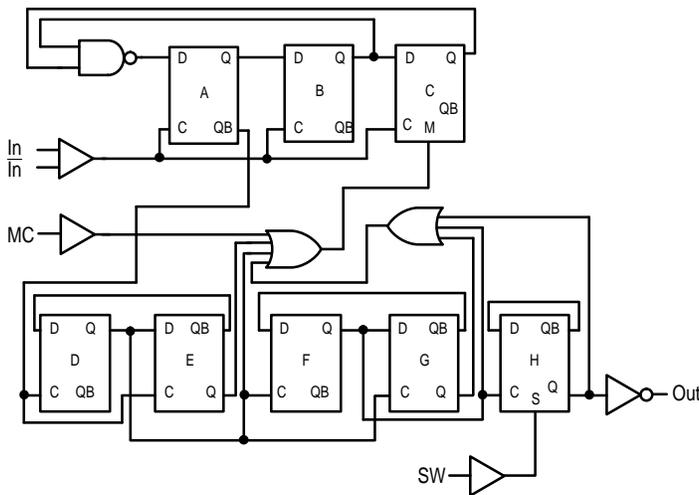
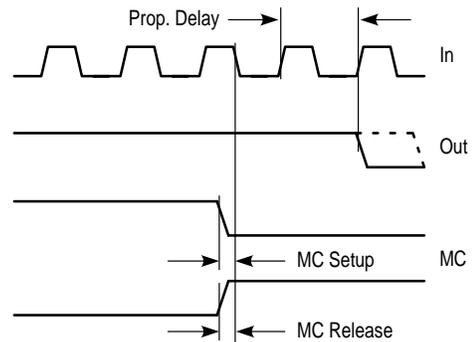


Figure 1. Logic Diagram (MC12028A)



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 2. Modulus Setup Time

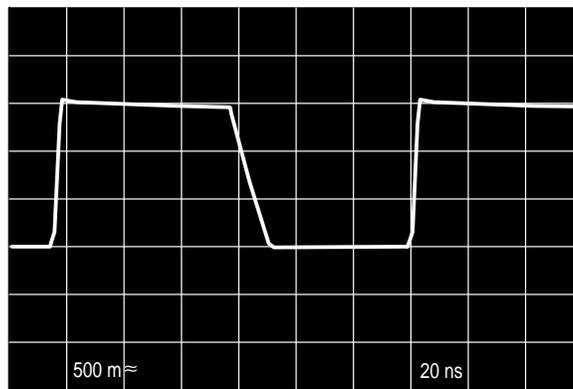


Figure 3. Typical Output Waveform

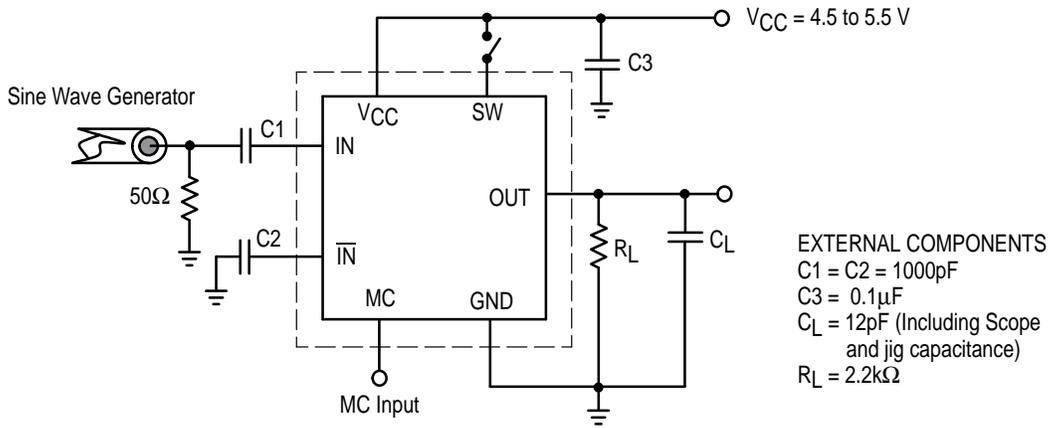


Figure 4. AC Test Circuit

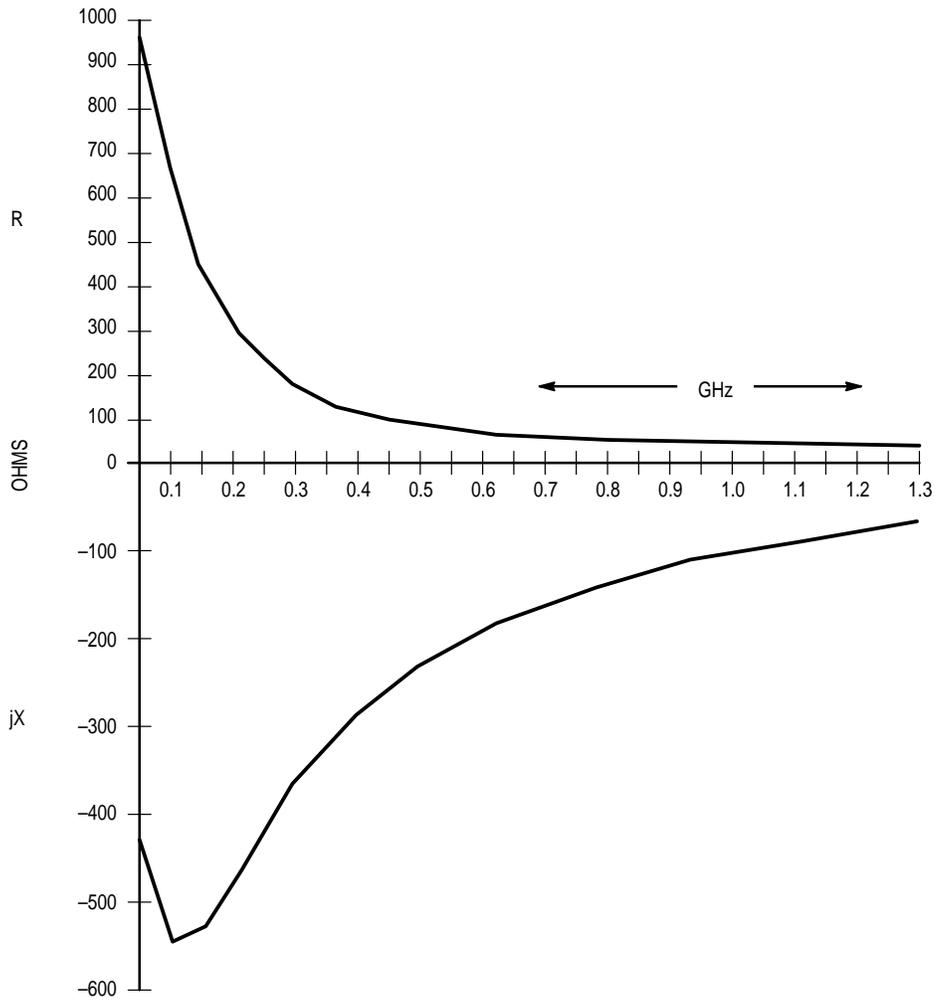


Figure 5. Typical Input Impedance versus Input Frequency

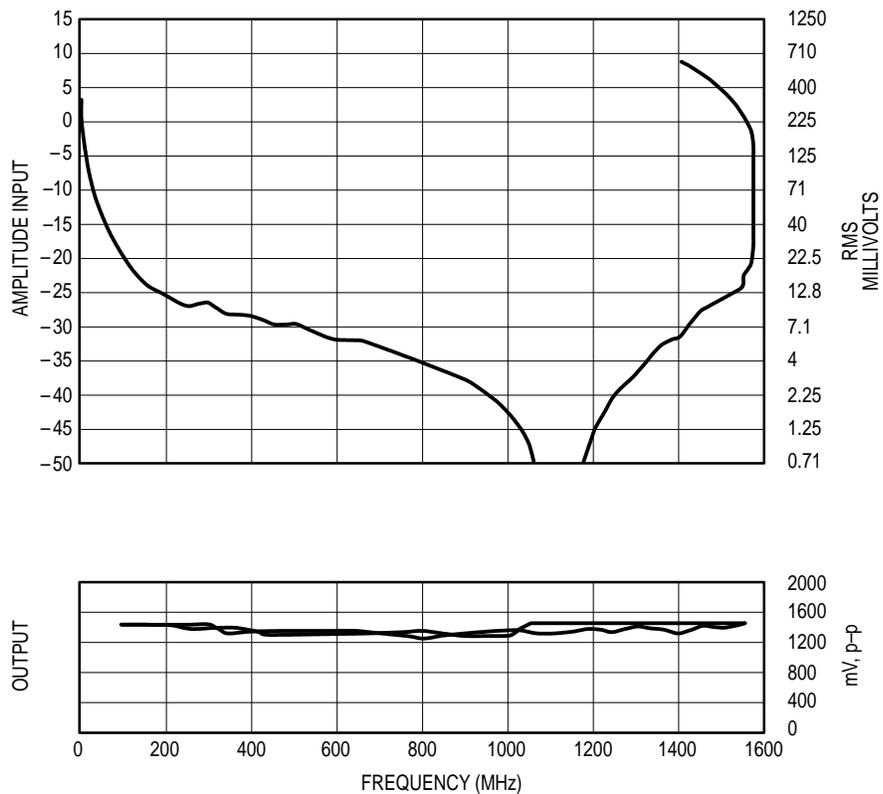
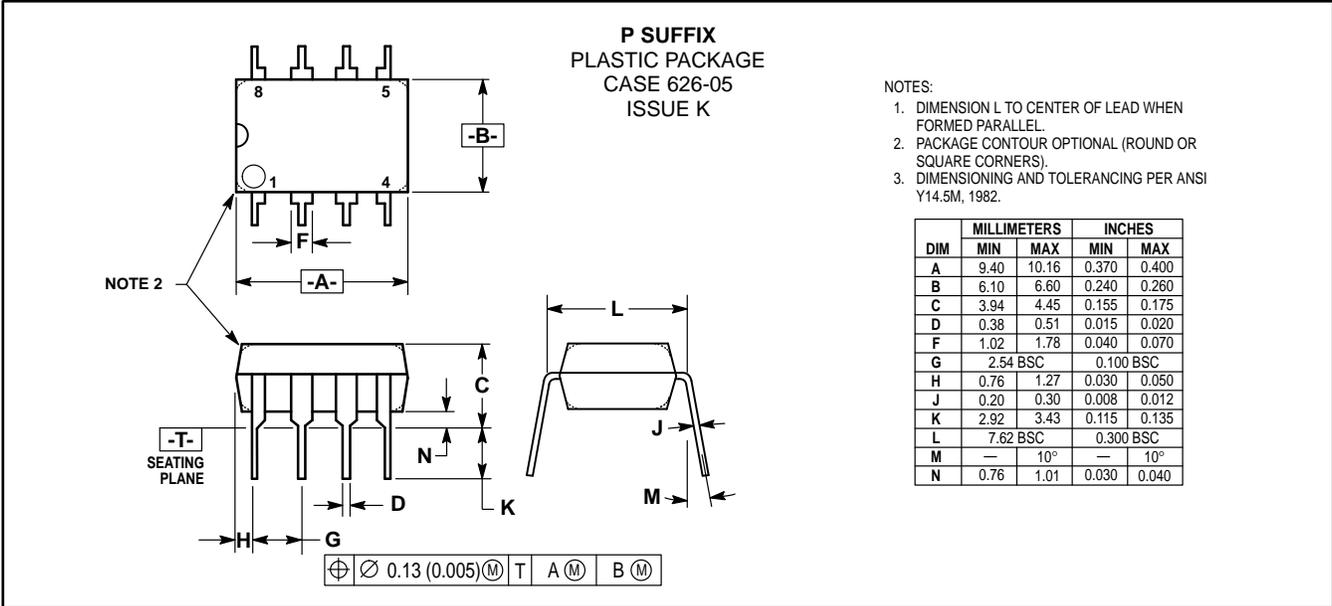
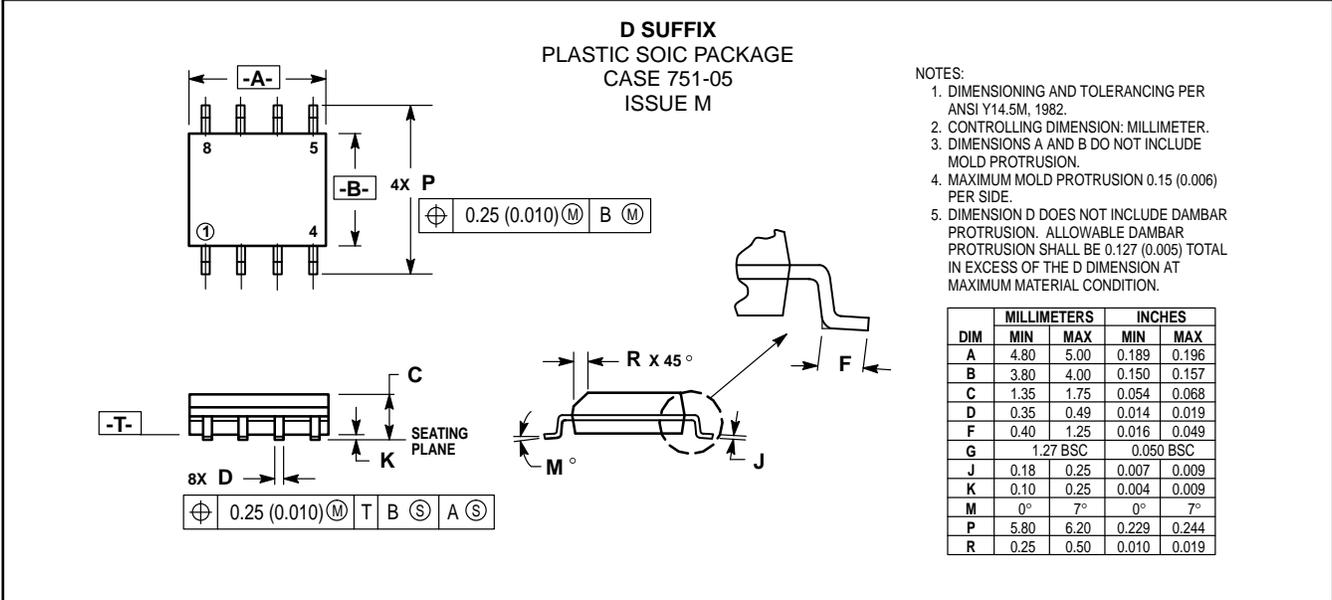


Figure 6. Input Signal Amplitude versus Input Frequency
Divide Ratio = 32

OUTLINE DIMENSIONS



- NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
 3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

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