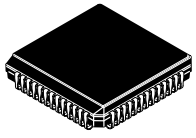
Product Preview

155Mb/s / 622Mb/s Receiver (Demultiplexer) with Clock Recovery

MC10SX1401

RECEIVER (DEMULTIPLEXER) WITH CLOCK RECOVERY



FJ SUFFIX
52–LEAD CLCC PACKAGE
CASE 778B-01

The MC10SX1401 receiver (Rx) chip is an integrated de–serialization SONET OC–3 (155.52 Mb/s) and OC–12 (622.08 Mb/s) interface device. It performs the data and clock recovery and serial–to–parallel conversion functions in conformance with SONET/SDH transmission standards. High performance and low power is achieved with MOSAIC V™, Motorola's most advanced high–performance silicon Bipolar process. A companion serialization (Tx) chip, the SX1405, is also available.

- Recovers a 155.52/622.08 MHz internal clock from an OC3/OC12 data stream
- Samples, quantizes and demultiplexes the input signal into a parallel TTL data stream
- Generates an EVEN parity bit with the demultiplexed data
- Provides a 155.52 MHz differential PECL timing reference clock
- No external input reference clock is required
- Detects the peak amplitude of the Rx signal and generates a proportional DC voltage
- Provides PLL Frequency Control Monitor and Out–of–Lock Indicator
- Adjustable phase offset of the Clock Recovery PLL
- Selectable eight or four bit parallel interface
- Single supply operation (+5V)

APPLICATIONS

- SONET/SDH–based transmission systems, modules, test equipment
- ATM using SONET
- Add drop multiplexers
- Other (non–SONET) data rate transmission systems

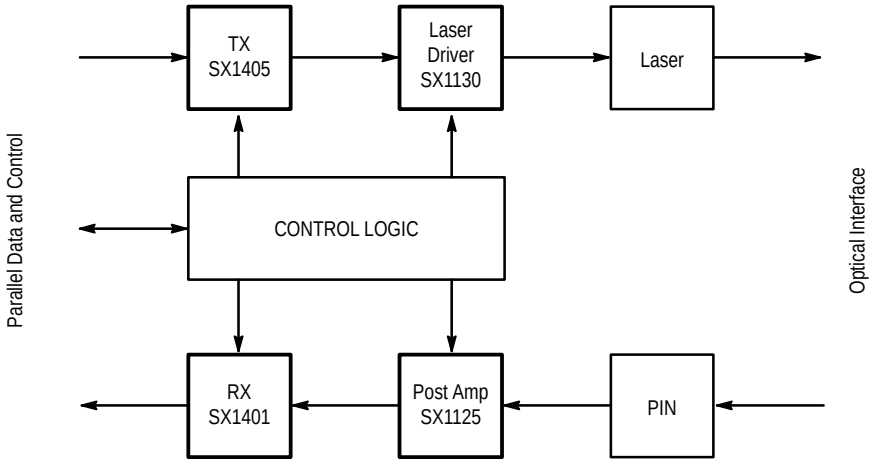


Figure 1. Typical OC3/OC12 Electro–Optical Interface

This document contains information on a new product. Specifications and information herein are subject to change without notice.

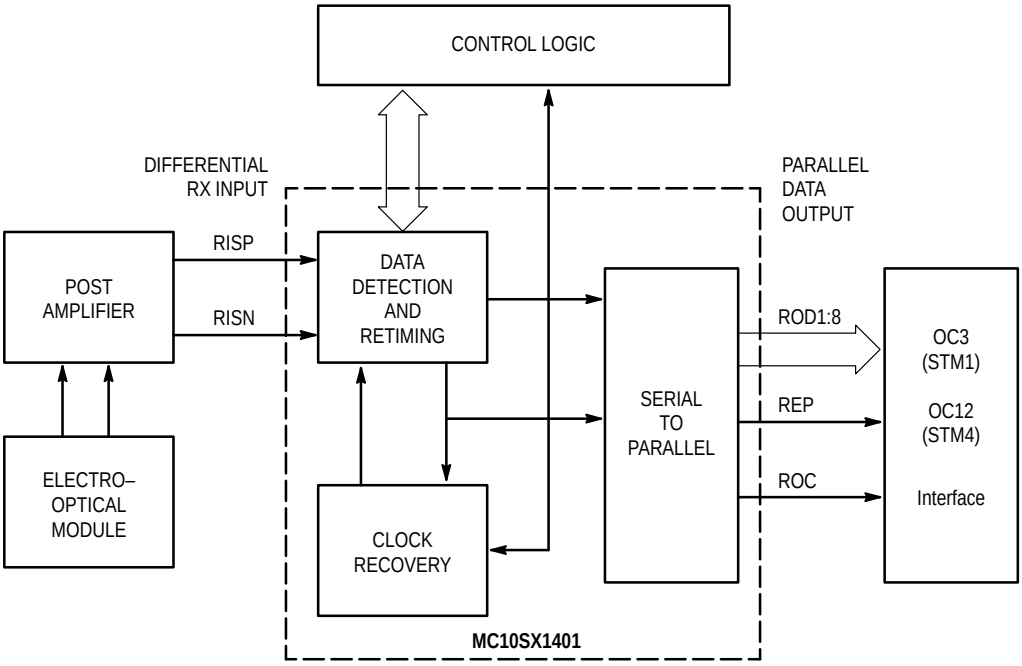


Figure 2. MC10SX1401 Simplified Block Diagram

MX10SX1401 Theory of Operation

Operation of the SX1401 is straight forward. The device recovers clock and data from the serial input. Serial–to–parallel conversion is performed. Then the parallel data, parity, and recovered clock is output. The bit–serial 622 Mbit/s or 155 Mbit/s data stream is converted into a 78 MByte/s or 19 MByte/s parallel data format.

The Data Clock is recovered from the incoming data stream. No external reference clock is required. For testing and applications which provide an external high–frequency bit clock, the internal clock recovery circuit may be bypassed.

SX1401 Block Diagram Functional Description

Data Detection and Retiming

Receives the differential input signal and retimes the serial data with the Recovered Clock.

The peak amplitude of the differential input signal is also detected and a proportional Peak Detector Output (PDO) DC voltage is output.

Clock Recovery

Using a standard phase locked loop (PLL) configuration, the clock recovery circuit locks the output of an internal VCO to the phase and frequency of the detected differential input signal. The internal VCO operates nominally at 1.2GHz. The output of the VCO is then divided to provide an internal Recovered Clock at either 622MHz or 155MHz.

An Out Of Lock indicator (OOL) is driven HIGH if the PLL is not locked.

Serial to Parallel Conversion

In OC3 mode, converts the retimed serial data into either a 4–bit (Nibble) or 8–bit (Byte) parallel format. This parallel data is output to the ROD1:8 Bus. In Nibble mode, the data appears on ROD2, 4, 6, 8.

In OC12 mode, the retimed serial data is converted into an 8–bit (Byte) parallel format. This parallel data is output to the ROD1:8 Bus.

A parity bit is also generated from the retimed serial data as it is shifted into the parallel register. the Receive Even Parity Output (REP) is toggled whenever the current nibble has EVEN parity.

The internal Recovered Clock is buffered and output as a TTL Receive Output Data Clock (ROC) at 78MHz, 39MHz, or 19MHz, depending on the selected mode. Also output is a PECL Differential Receiver Clock (RCKP/RCKM) at 155MHz.

SX1401 Control Signals

Reset (RSTN) – Used for testing and verification, the TTL outputs are set to Tri–State and all divider flip–flops are reset by applying RSTN LOW. An internal pull–up is provided on RSTN allowing the device to operate normally if RSTN is not used.

Low Speed Select (LSS) – Selects data rate. LOW = OC–12 (622.08 Mb/s), HIGH = OC–3 (155.52 Mb/s). An internal pull–up is provided on LSS allowing the device to operate in OC–12 mode if LSS is not used.

Byte / Nibble Select (BYTE) – In OC–3 mode, selects between 4–bit (Nibble) and 8–bit (Byte) parallel data output format. LOW = Nibble, HIGH = Byte. An internal pull–up is provided on BYTE allowing the device to operate in Byte mode if BYTE is not used.

External Clock Select (ECSN) – Allows external high–frequency bit clock to be applied and bypasses the internal clock recovery circuit. LOW = External bit clock. An internal pull–up is provided on ECSN allowing the device to operate normally if ECSN is not used.

VCO Frequency Control Monitor (FCM) – Single ended reference voltage output generated from the VCO control voltage. Typically 1.25V and varying from 0.25V to 2.25V.

Out of Lock Indicator (OOL) – Is set HIGH if the PLL is not frequency–locked to the incoming serial stream.

PLL Phase Offset (POS) – Analog input controlling variation of PLL Phase Offset. Typically 1.3V, varies from 0.25V to 2.25V.

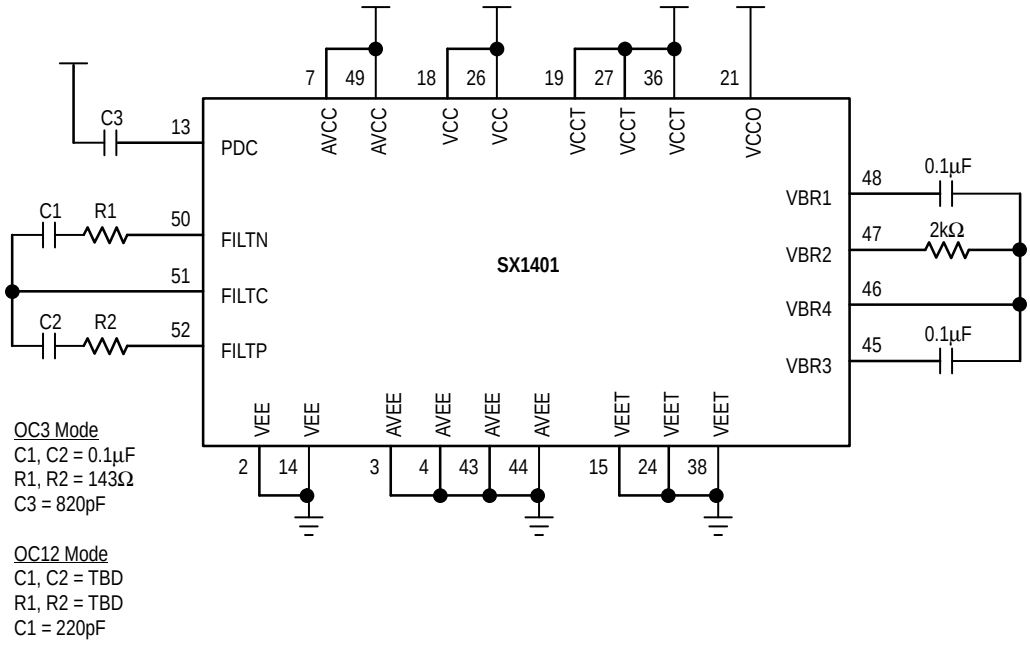


Figure 3. SX1401 Typical Operating Circuit

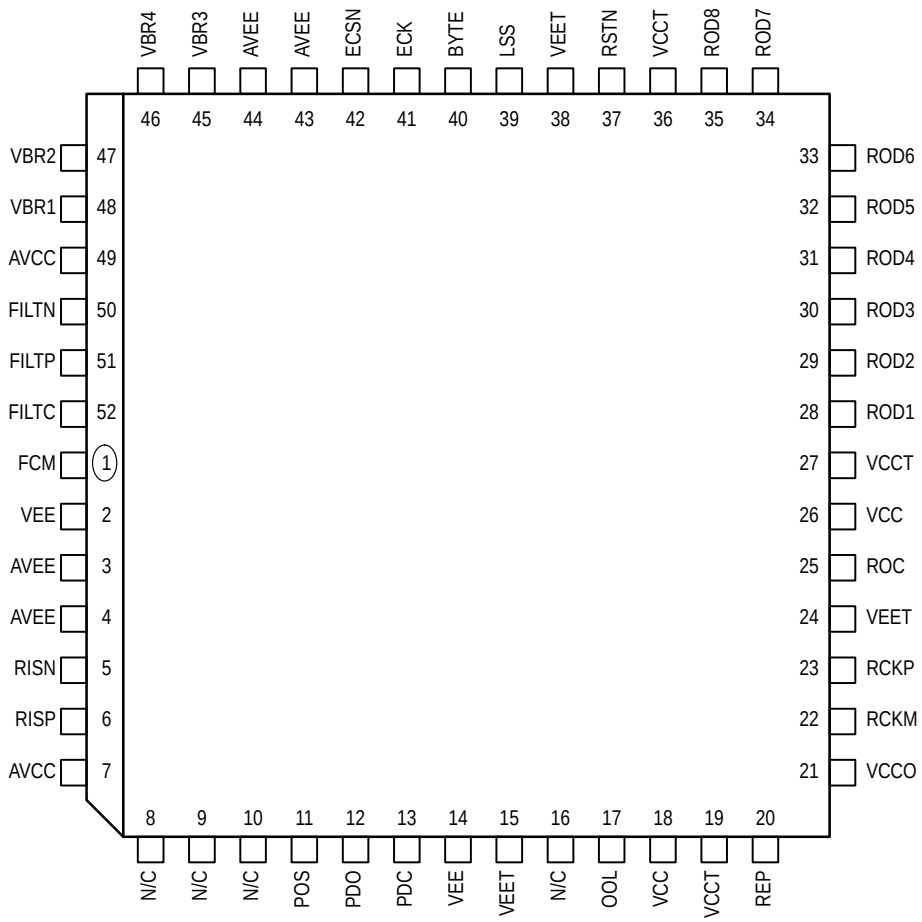


Figure 4. MC10SX1401 52–Lead Pinout (Top View)

Table 1. SX1401 Pin Descriptions

Name	Pin No	Description
TTL Compatible I/O		
OOL	17	Out of Lock Indicator Output
REP	20	Receive Even Parity Output
ROC	25	Receive Output Data Clock
ROD1	28	Parallel Output Data (Byte MSB)
ROD2	29	Parallel Output Data (Nibble MSB)
ROD3	30	Parallel Output Data
ROD4	31	Parallel Output Data (Nibble MSB–1)
ROD5	32	Parallel Output Data
ROD6	33	Parallel Output Data (Nibble MSB–2)
ROD7	34	Parallel Output Data
ROD8	35	Parallel Output Data (Byte and Nibble LSB)
RSTN	37	Reset Input
LSS	39	Low Speed Select Input
BYTE	40	Byte / Nibble Select Input
ECSN	42	External Clock Select Input
PECL Compatible I/O		
RCKM	22	Differential Receiver Clock Minus Output
RCKP	23	Differential Receiver Clock Plus Output
ECK	41	External Clock Output
Analog I/O		
FCM	1	VCO Frequency Control Monitor Output
RISN	5	Serial Data Input Negative
RISP	6	Serial Data Input Positive
POS	11	PLL Phase Offset
PDO	12	Peak Detector Output
PDC	13	Peak Detector Capacitor
VBR4–VBR1	45–48	VCO Filter Pins
FILTN	50	Loop Filter Negative
FILTC	51	Loop Filter Positive
FILTP	52	Loop Filter Common
Power and Ground Pins		
VEE	2, 14	PECL 0V Supply
AVEE	3, 4, 43, 44	Analog 0V Supply
AVCC	7, 49	Analog +5V Supply
VEET	15, 24, 38	Output TTL 0V Supply
VCC	18, 26	PECL +5V Supply
VCCT	19, 27, 36	Output TTL +5V Supply
VCCO	21	Output PECL +5V Supply
Reserved		
N/C	8–10, 16	Reserved for Factory Test

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
VCC, VCCO, VCCT, AVCC	Power Supply (VEE, VEET, AVEE, GVEE = 0V)	–0.5 to +6.5	V
VIN	Input Voltage (VEE, VEET, AVEE, GVEE = 0V)	–0.5 to +6.5	V
IOUT	PECL Output Current Continuous Surge	50 100	mA
IOUT–TTL	TTL Output Current	5	mA
TSTG	Storage Temperature	–50 to +175	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
VCC, VCCO, VCCT, AVCC	Power Supply (VEE, VEET, AVEE, GVEE = 0V)	5V ±5%	V
ICC	Device Current Drain	225	mA
TA	Operating Temperature	–40 to +85	°C
TJ	Junction Temperature	125	°C

TTL DC CHARACTERISTICS (VCC = VCCT = VCCO = AVCC = 5.0V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
IIH	Input HIGH Current			20	µA	VIN = V_{CC}
IIL	Input LOW Current			–0.6	mA	VIN = 0.5V
VOH	Output HIGH Voltage REP, ROD EDO, OOL	2.5 2.5			V	IOH = –2mA IOH = –300µA
VOL	Output LOW Voltage			0.5	V	IOL = 5mA
VIH	Input HIGH Voltage	2.0			V	
VIL	Input LOW Voltage			0.8	V	
IOZ	Tri–State Current			±50	µA	

100E PECL DC CHARACTERISTICS (VCC = VCCT = VCCO = AVCC = 5.0V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
IIH	Input HIGH Current			200	mA	
IIL	Input LOW Current	0.5			mA	
VOH	Output HIGH Voltage	3.93		4.19	V	NOTE 1.
VOL	Output LOW Voltage	3.19		3.45	V	NOTE 1.
VIH	Input HIGH Voltage	3.93		4.19	V	NOTE 1.
VIL	Input LOW Voltage	3.19		3.43	V	NOTE 1.

1. PECL levels are referenced to VCC and will vary 1:1 with the Power Supply. The Outputs are loaded with an equivalent 50Ω termination to +3.0V. The values shown are for VCC = VCCT = VCCO = AVCC = 5.0V.

PLL COMPONENT CHARACTERISTICS (VCC = VCCT = VCCO = AVCC = 5.0V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
IFILT	Loop Filter Currents (FILTP–FILTN)	250 –450 –20 –40 –40		450 –250 20 40 40	µA	PD Up, FD=Neutral PD Down, FD = Neutral PD, FD = Neutral FD Up, PD = Neutral FD Down, PD = Neutral
IUP + IDN	Phase Detector UP + DOWN Current	–40		40	µA	IUP + IDOWN
Kdt	Combined Phase Detector TZA Gain	45		80	µA/rad	
ADV	Loop Filter Amplifier Large Signal Differential Voltage Amplification	100	250		V/V	
ϕE	Phase Error	–0.5		0.5	radians	
VFCM	FCM Amplitude Range	0.4		2	V	
	FCM Locked PLL Range	0.65		1.85	V	
	FCM Shorted	1.1		1.4	V	FILTP, FILTN Shorted
EFCM	FCM Error	–100		100	mV	
KFCM	FCM Gain	0.45		0.55	gain	
RO	FCM Output Impedance		5000		Ω	
KPOS	POS Gain	150		350	µA/V	
fVCO	VCO Frequency	800	1244	1700	MHz	2000Ω (1%) – EXT. R
	VCO Frequency Shorted	1000		1450	MHz	FILTP, FILTN Shorted
KO	VCO Gain	120	180	260	MHz/V	2000Ω (1%) – EXT. R
KOVCC	VCC Supply (AVCC) Sensitivity	–80		80	MHz/V	0 < fVCC < 10MHz
ϕVCO	VCO Phase Noise		–30		dBc/Hz	at f = 1kHz
			–90		dBc/Hz	at f = 1kHz

DATA INPUT CHARACTERISTICS (VCC = VCCT = VCCO = AVCC = 5.0V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
VRIS	Input SIgnal Amplitude	40		2000	mV	PP–DIFF AC Coupled
VSO	Input Offset (DST)	–10	3	10	mV	VDST=VR=1.25V
ΔVSO	Relative Input Offset (DST/EST)	–10	3	10	mV	VDST=VEST=1.25V
VDT	Input Offset Sensitivity	0.05		0.15	V/V	VRIS= ±100mV
ΔVDT	Relative Input Offset Sensitivity	–0.05		0.05	V/V	VRIS= ±100mV
VDTO	Slicing Threshold Offset	–90		90	mV	VRIS=0V
ΔVDTO	Relative Slicing Threshold Offset	–90		90	mV	VRIS=0V
RI	Input Resistance – DC		2000		Ω	Across RISP, RISN
RI	Input Resistance – AC		1360		Ω	Across RISP, RISN
CI	Input Capacitance		1.0		pF	RISP, RISN

PEAK DETECTOR CHARACTERISTICS (VCC = VCCT = VCCO = AVCC = 5.0V +5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
VPDO	Peak Detector Output	1.30		1.65	V	PDC cap = 1000pF (OC3)
KPDO	Peak Detector Voltage Sensitivity	2.5		4.0	mV/mVpp	PDC cap = 1000pF (OC3)

AC CHARACTERISTICS (VCC = VCCT = VCCO = AVCC = 5.0V +5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
tr, tf	PECL Rise/Fall Time			1.6	nS	20–80%
tr, tf	TTL Rise/Fall Time ROC ROD, REP			3.2 5.0	nS	20–80%, 500Ω, 20pF
tpd	Skew: ROC → ROD, ROP	–3.0		3.0	nS	
tdc	Duty Cycle: ROC, OC3	–15		15	%	th/(tl+th)
tdc	Duty Cycle: RCK, OC3	–15		15	%	th/(tl+th)

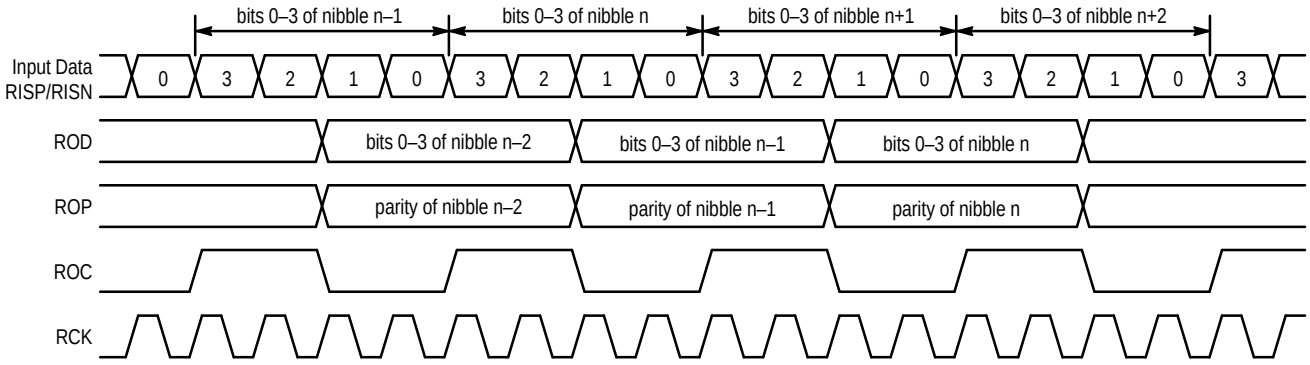


Figure 5. SX1401 Timing Diagram — OC–3, 4 Bits

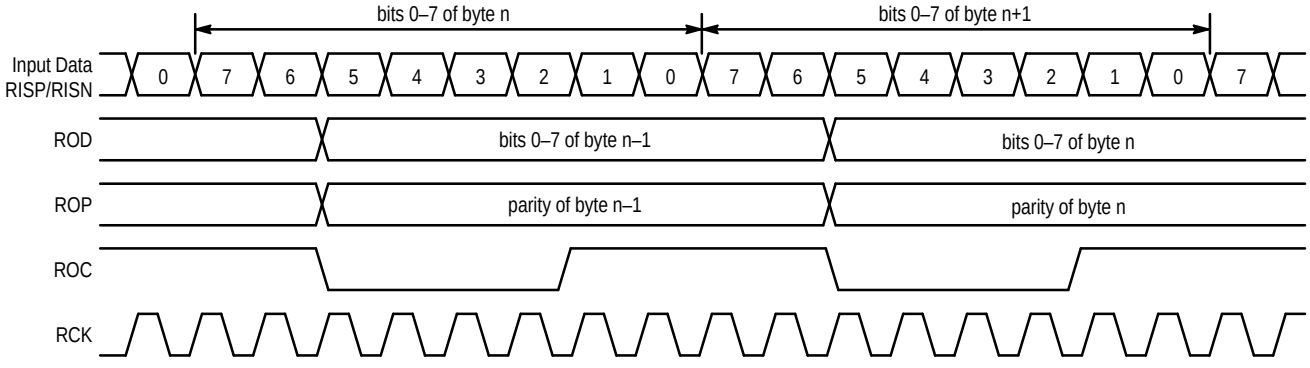


Figure 6. SX1401 Timing Diagram — OC–3, 8 Bits

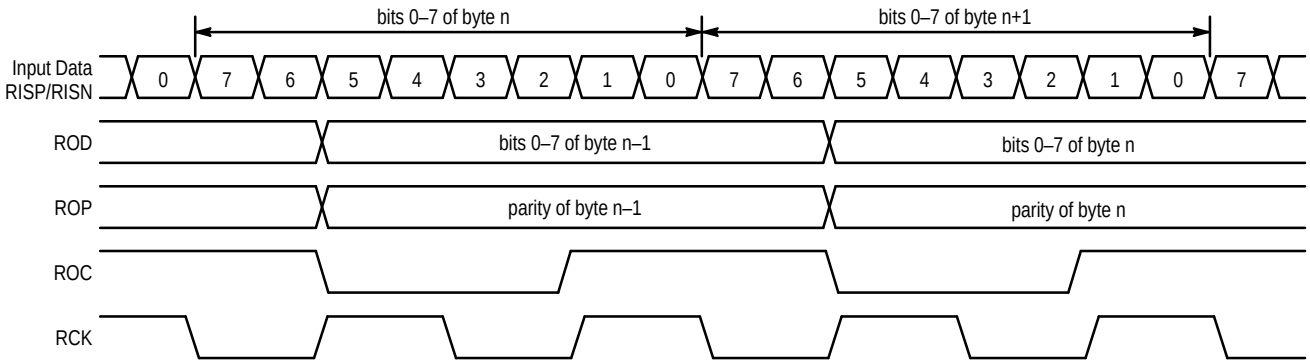
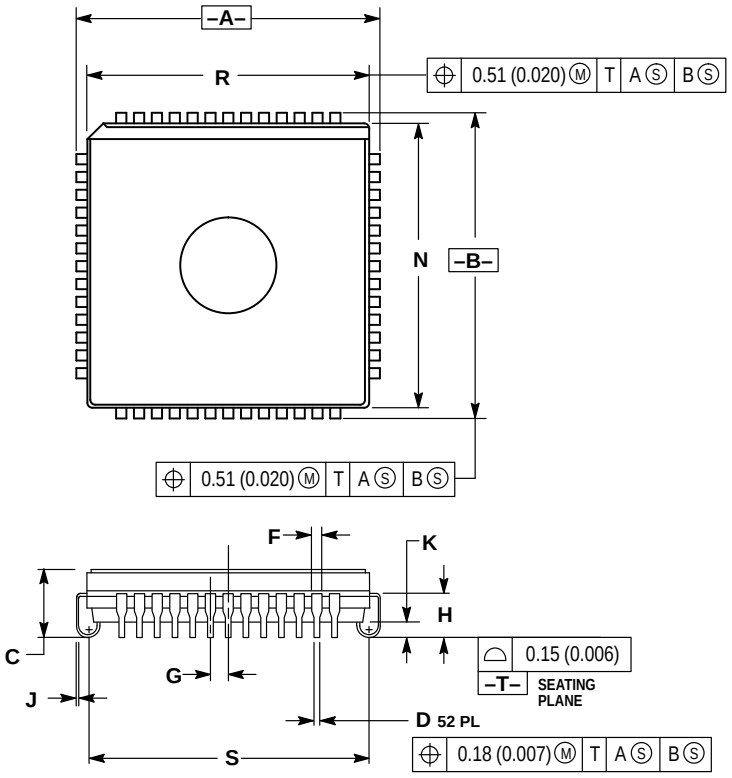


Figure 7. SX1401 Timing Diagram — OC–12, 8 Bits
(Note: The relative phase of RCK with ROD, ROP and ROC is not guaranteed.
The depiction here is merely to show relative frequency)

OUTLINE DIMENSIONS

FJ SUFFIX
CLCC PACKAGE
CASE 778B–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION R AND N DO NOT INCLUDE GLASS PROTRUSION. GLASS PROTRUSION TO BE 0.25 (0.010) MAXIMUM.
4. ALL DIMENSIONS AND TOLERANCES INCLUDE LEAD TRIM OFFSET AND LEAD FINISH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.200	4.20	5.08
D	0.017	0.021	0.44	0.53
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
H	0.090	0.130	2.29	3.30
J	0.006	0.010	0.16	0.25
K	0.035	0.045	0.89	1.14
N	0.735	0.756	18.67	19.20
R	0.735	0.756	18.67	19.20
S	0.690	0.730	17.53	18.54

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