

68030/040 ECL/TTL Clock Driver

The MC10H/100H640 generates the necessary clocks for the 68030, 68040 and similar microprocessors. It is guaranteed to meet the clock specifications required by the 68030 and 68040 in terms of part-to-part skew, within-part skew and also duty cycle skew.

The user has a choice of using either TTL or ECL (referenced to +5.0V) for the input clock. TTL clocks are typically used in present MPU systems. However, as clock speeds increase to 50MHz and beyond, the inherent superiority of ECL (particularly differential ECL) as a means of clock signal distribution becomes increasingly evident. The H640 also uses differential ECL internally to achieve its superior skew characteristic.

The H640 includes divide-by-two and divide-by-four stages, both to achieve the necessary duty cycle skew and to generate MPU clocks as required. A typical 50MHz processor application would use an input clock running at 100MHz, thus obtaining output clocks at 50MHz and 25MHz (see Logic Symbol).

The 10H version is compatible with MECL 10H™ ECL logic levels, while the 100H version is compatible with 100K levels (referenced to +5.0V).

- Generates Clocks for 68030/040
- Meets 030/040 Skew Requirements
- TTL or ECL Input Clock
- Extra TTL and ECL Power/Ground Pins
- Asynchronous Reset
- Single +5.0V Supply
- Choice of ECL Compatibility: MECL 10H (10Hxxx) or 100K (100Hxxx)

Function

Reset (R): LOW on RESET forces all Q outputs LOW and all \bar{Q} outputs HIGH.

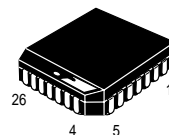
Power-Up: The device is designed to have the POS edges of the ± 2 and ± 4 outputs synchronized at power up.

Select (SEL): LOW selects the ECL input source (DE/DE). HIGH selects the TTL input source (DT).

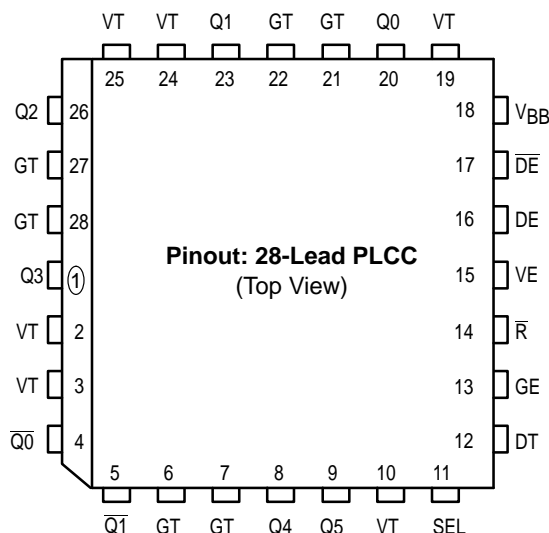
The H640 also contains circuitry to force a stable state of the ECL input differential pair, should both sides be left open. In this case, the DE side of the input is pulled LOW, and DE goes HIGH.

MC10H640
MC100H640

68030/040
ECL/TTL CLOCK
DRIVER



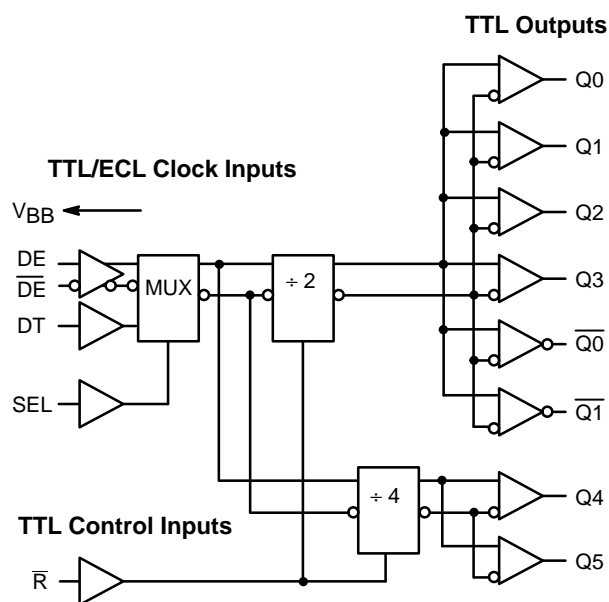
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02



LOGIC DIAGRAM

PIN NAMES

PIN	FUNCTION
GT	TTL Ground (0 V)
VT	TTL V_{CC} (+5.0 V)
VE	ECL V_{CC} (+5.0 V)
GE	ECL Ground (0 V)
DE, \overline{DE}	ECL Signal Input (positive ECL)
V_{BB}	V_{BB} Reference Output
DT	TTL Signal Input
$Q_n, \overline{Q_n}$	Signal Outputs (TTL)
SEL	Input Select (TTL)
\overline{R}	Reset (TTL)



AC CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic		0°C		25°C		85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t _{PLH}	Propagation Delay ECL D to Output	Q0–Q3	4.9	5.9	4.9	5.9	5.2	6.2	ns	CL = 25pF
t _{PLH}	Propagation Delay TTL D to Output		5.0	6.0	5.0	6.0	5.3	6.3	ns	CL = 25pF
tskwd*	Within-Device Skew			0.5		0.5		0.5	ns	CL = 25pF
t _{PLH}	Propagation Delay ECL D to Output	Q0, Q1	4.9	5.9	4.9	5.9	5.2	6.2	ns	CL = 25pF
t _{PLH}	Propagation Delay TTL D to Output		5.0	6.0	5.0	6.0	5.3	6.3	ns	CL = 25pF
t _{PLH}	Propagation Delay ECL D to Output	Q4, Q5	4.9	5.9	4.9	5.9	5.2	6.2	ns	CL = 25pF
t _{PLH}	Propagation Delay TTL D to Output		5.0	6.0	5.0	6.0	5.3	6.3	ns	CL = 25pF
t _{PD}	Propagation Delay R to Output	All Outputs	4.3	6.3	4.3	6.3	5.0	7.0	ns	CL = 25pF
t _R t _F	Output Rise/Fall Time 0.8 V – 2.0 V	All Outputs		2.5 2.5		2.5 2.5		2.5 2.5	ns	CL = 25pF
f _{max}	Maximum Input Frequency		135		135		135		MHz	CL = 25pF
t _{pw}	Minimum Pulse Width		1.50		1.50		1.50		ns	
t _{rr}	Reset Recovery Time		1.25		1.25		1.25		ns	

* Within-Device Skew defined as identical transitions on similar paths through a device.

V_{CC} and CLOAD RANGES TO MEET DUTY CYCLE REQUIREMENTS (0°C ≤ T_A ≤ 85°C Output Duty Cycle Measured Relative to 1.5V)

Symbol	Characteristic		Min	Nom	Max	Unit	Condition
	Range of V _{CC} and CL to meet minimum pulse width (HIGH or LOW) = 11.5 ns at f _{out} ≤ 40 MHz	V _{CC} CL	4.75 10	5.0	5.25 50	V pF	Q0–Q3 Q0–Q1
	Range of V _{CC} and CL to meet minimum pulse width (HIGH or LOW) = 9.5 ns at 40 < f _{out} ≤ 50 MHz	V _{CC} CL	4.875 15	5.0	5.125 27	V pF	Q0–Q3

DC CHARACTERISTICS (V_T = V_E = 5.0 V ±5%)

Symbol	Characteristic		0°C		25°C		85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
I _{EE}	Power Supply Current	ECL		57		57		57	mA	VE Pin
I _{CCH}		TTL		30		30		30	mA	Total all VT pins
I _{CCL}				30		30		30	mA	

TTL DC CHARACTERISTICS (V_T = V_E = 5.0 V ±5%)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V _{IH} V _{IL}	Input HIGH Voltage Input LOW Voltage	2.0	0.8	2.0	0.8	2.0	0.8	V	
I _{IH}	Input HIGH Current		20 100		20 100		20 100	μA	V _{IN} = 2.7V V _{IN} = 7.0V
I _{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V _{IN} = 0.5V
V _{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I _{OH} = –3.0mA I _{OH} = –15mA
V _{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I _{OL} = 24mA
V _{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I _{IN} = –18mA
I _{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V _{OUT} = 0V

10H ECL DC CHARACTERISTICS ($V_T = V_E = 5.0\text{ V} \pm 5\%$)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	0.5	225	0.5	175	0.5	175	μA	
V_{IH}^* V_{IL}^*	Input HIGH Voltage Input LOW Voltage	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.555	V	$V_E = 5.0\text{V}$
V_{BB}^*	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	

*NOTE: ECL levels are referenced to V_{CC} and will vary 1:1 with the power supply. The values shown are for $V_{CC} = 5.0\text{V}$.

100H ECL DC CHARACTERISTICS ($V_T = V_E = 5.0\text{ V} \pm 5\%$)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	0.5	225	0.5	175	0.5	175	μA	
V_{IH}^* V_{IL}^*	Input HIGH Voltage Input LOW Voltage	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	V	$V_E = 5.0\text{V}$
V_{BB}^*	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	

*NOTE: ECL levels are referenced to V_{CC} and will vary 1:1 with the power supply. The values shown are for $V_{CC} = 5.0\text{V}$.

10/100H640 DUTY CYCLE CONTROL

To maintain a duty cycle of $\pm 5\%$ at 50MHz, limit the load capacitance and/or power supply variation as shown in Figures 1 and 2. For a $\pm 2.5\%$ duty cycle limit, see Figures 3 and 4. Figures 5 and 6 show duty cycle variation with temperature. Figure 7 shows typical TPD versus load. Figure 8 shows reset recovery time. Figure 9 shows output states after power up.

Best duty cycle control is obtained with a single μP load and minimum line length.

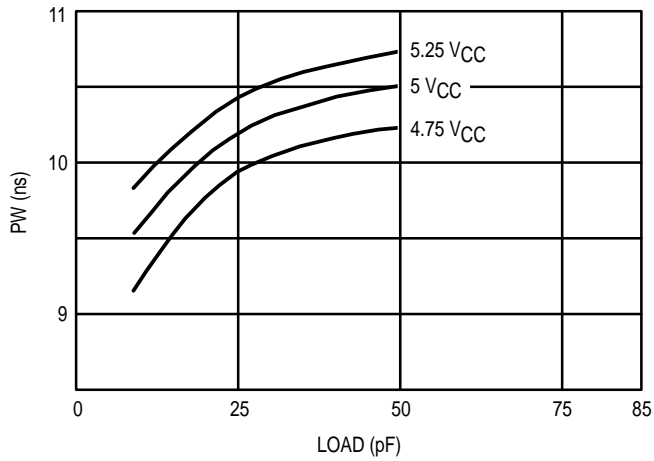


Figure 1. Positive Pulse Width at 25°C Ambient and 50 MHz Out

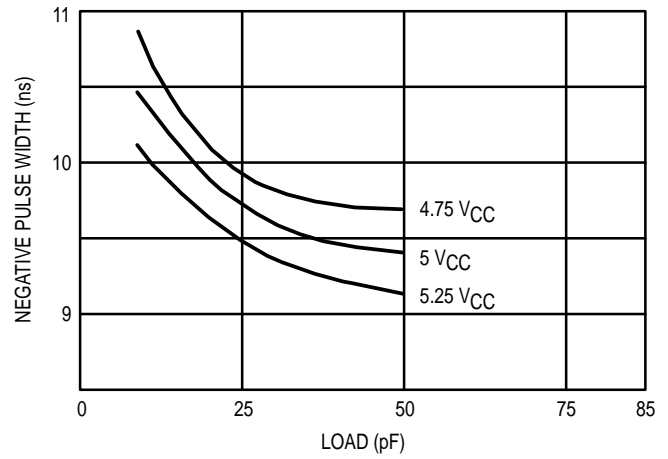


Figure 2. Negative Pulse Width @ 50 MHz Out and 25°C Ambient

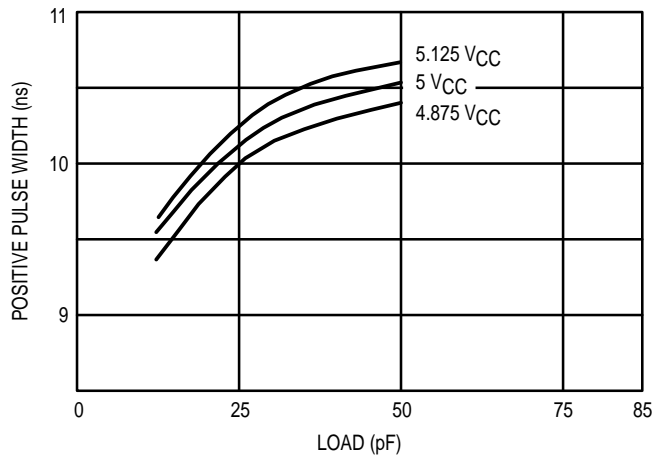


Figure 3. Positive Pulse Width at 25°C Ambient at 50 MHz Out

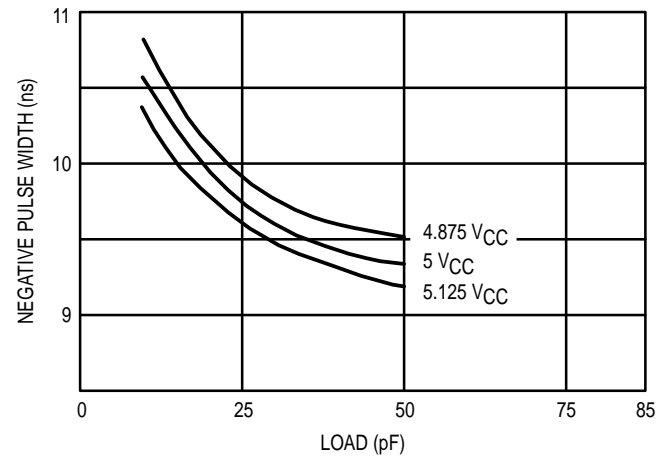


Figure 4. Negative Pulse Width @ 50 MHz Out and 25°C Ambient

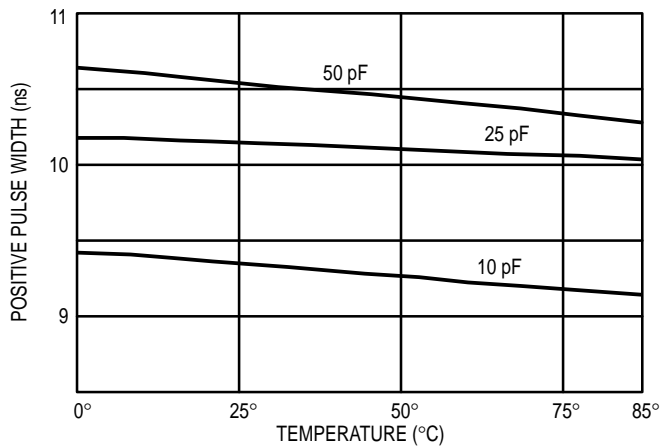


Figure 5. Temperature versus Positive Pulse Width for 100H640 at 50 MHz and +5.0 V V_{CC}

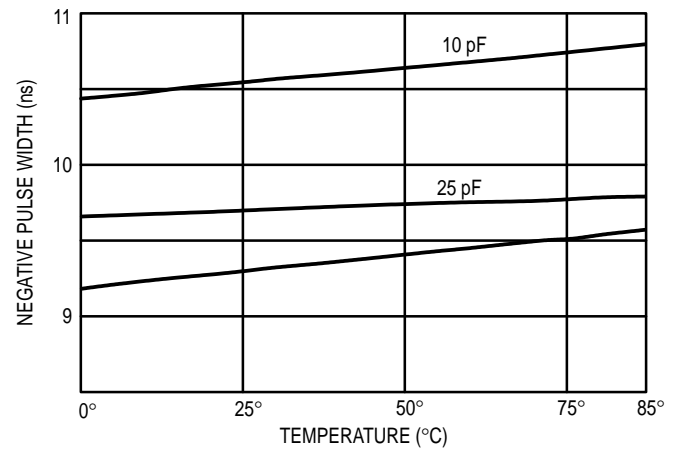


Figure 6. Temperature versus Negative Pulse Width for MC100H640 @ 50 MHz and +5.0 V V_{CC}

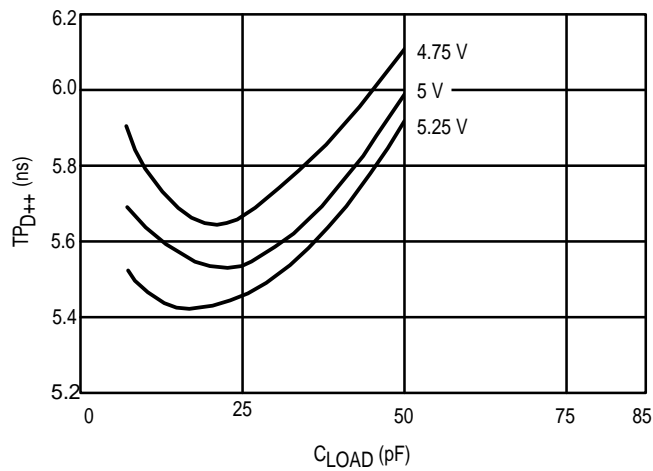


Figure 7. TP versus Load Typical at TA = 25°C

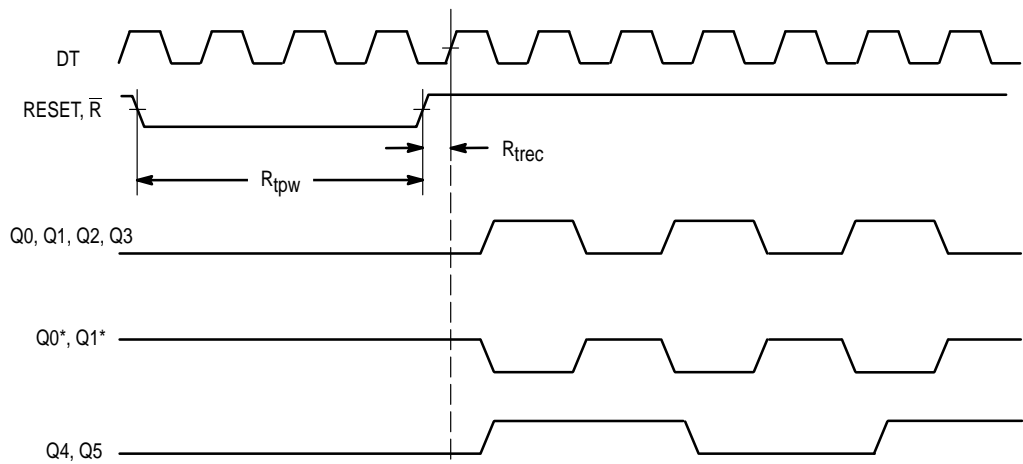
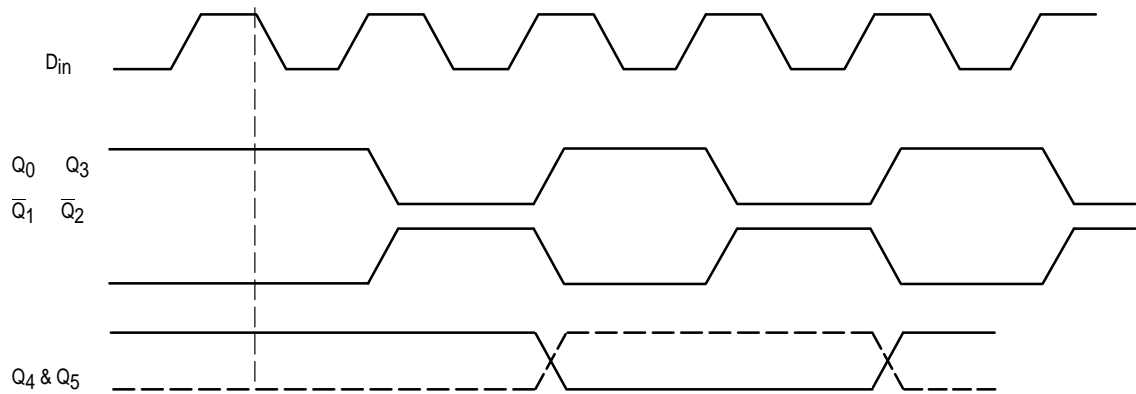


Figure 8. MC10H/100H640 Clock Phase and Reset Recovery Time After Reset Pulse

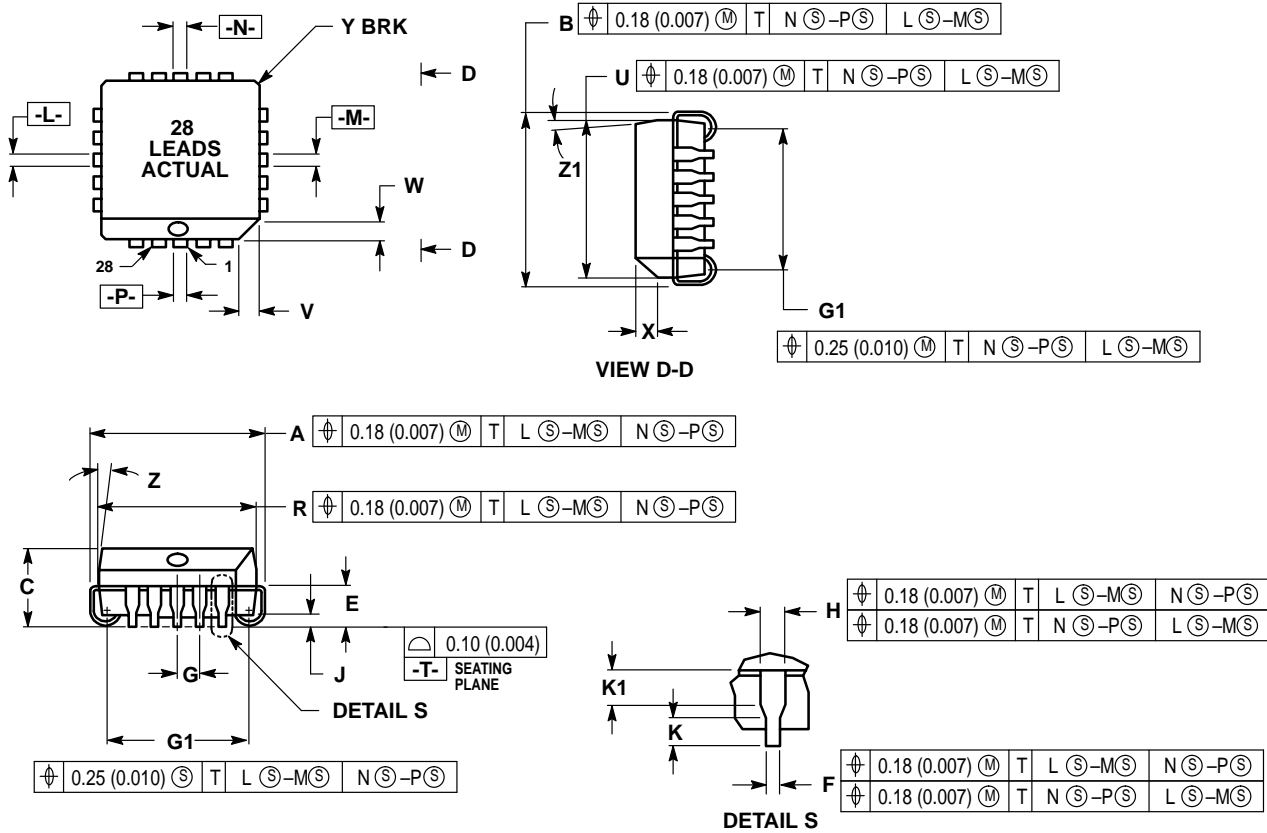


AFTER POWER UP
OUTPUTS Q4 & Q5 WILL SYN WITH POSITIVE EDGES OF D_{in} & Q0 Q3 & NEGATIVE EDGES OF \bar{Q}_0 & \bar{Q}_1

Figure 9. Output Timing Diagram


OUTLINE DIMENSIONS

FN SUFFIX
PLASTIC PACKAGE
CASE 776-02
ISSUE D



NOTES:

1. DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.
7. 776-01 IS OBSOLETE, NEW STANDARD 776-02.

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MC10H640/D

