5-Bit Differential Register

The MC10E/100E452 is a 5-bit differential register with differential data (inputs and outputs) and clock. The registers are triggered by a positive transition of the positive clock (CLK) input. A high on the Master Reset (MR) asynchronously resets all registers so that the Q outputs go LOW.

The differential input structures are clamped so that the inputs of unused registers can be left open without upsetting the bias network of the device. The clamping action will assert the D and the CLK sides of the inputs. Because of the edge triggered flip-flop nature of the device simultaneously opening both the clock and data inputs will result in an output which reaches an unidentified but valid state. Note that the input clamps only operate when both inputs fall to 2.5V below V_{CC}.

The fully differential design of the device makes it ideal for very high frequency applications where a registered data path is necessary.

- Differential D, CLK and Q; VBB Reference Available
- 1100MHz Min. Toggle Frequency
- Asynchronous Master Reset
- Extended 100E V_{EE} Range of 4.2V to 5.46V
 Pinout: 28-Lead PLCC (Top View)



 * All V_CC and V_CCO pins are tied together on the die.

PIN NAMES

Pin	Function
D[0:4], D[0:4]	Differential Data Inputs
MR	Master Reset Input
CLK, CLK	Differential Clock Input
VBB	VBB Reference Output
Q[0:4], Q[0:4]	Differential Data Outputs

12/93







DC CHARACTERISTICS (VEE = VEE(min) to VEE(max); VCC = VCCO = GND)

			–40°C			0°C			25°C			85°C				
Symbol	Characteri	istic	Min	Тур	Max	Unit	Cond									
V _{BB}	Output Refe Voltage	rence 10E 100E	-1.43 -1.38		-1.30 -1.26	-1.38 -1.38		-1.27 -1.26	-1.35 -1.38		-1.25 -1.26	-1.31 -1.38		-1.19 -1.26	V	
ΙΗ	Input HIGH Current				150			150			150			150	μA	
IEE	Power Supp Current	ly 10E 100E		74 74	89 89		74 74	89 89		74 74	89 89		74 85	89 102	mA	
VCMR	Common Mo Range	ode	-2.0		-0.4	-2.0		-0.4	-2.0		-0.4	-2.0		-0.4	V	1

V_{CMR} is referenced to the most positive side of the differential input signal. Normal specified operation is obtained when the input signals are within the V_{CMR} range and the input swing is greater than V_{PP}.

AC CHARACTERISTICS ($V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$)

			–40°C		0)°C to 85°0				
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Unit	Condition	
fMAX	Maximum Toggle Frequency		1000	1400		1100	1400		MHz	
^t PLH ^t PHL	Propagation Delay to Output	CLK (Diff) CLK (SE) MR	425 375 375	600 600 625	850 900 900	475 425 425	600 600 625	800 850 850	ps	
tS	Setup Time	D	175	-50		150	-50		ps	
tн	Hold Time	D	225	50		200	50		ps	
^t RR	Reset Recovery Time		750	450		700	450			
^t PW	Minimum Pulse Width	CLK MR	400 400			400 400			ps	
^t skew	Within-Device Skew			50			50		ps	1
VPP	Minimum Input Swing		150			150			mV	2
t _r /t _f	Rise/Fall Times		250	475	725	275	475	675	ps	20–80%

Within-device skew is defined as identical transitions on similar paths through a device.
 Minimum input swing for which AC parameters are guaranteed.





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