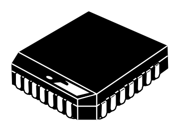
# 1:9 Differential ECL/PECL RAMBus Clock Buffer

## MC10E411

**1:9 DIFFERENTIAL ECL/PECL RAMBUS CLOCK BUFFER**



**FN SUFFIX**
PLASTIC PACKAGE
CASE 776-02

The MC10E411 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. The MC10E411's function and performance are similar to the popular MC10E111, with the added feature of 1.2V output swings. It accepts one signal input, which can be either differential or single-ended if the $V_{BB}$ output is used. The signal is fanned out to 9 identical differential outputs.

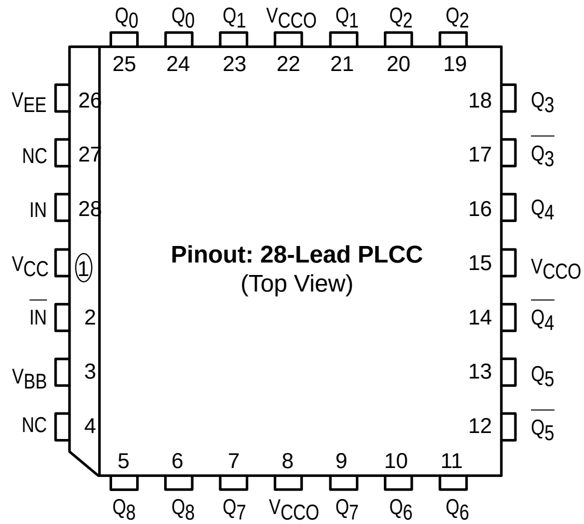
- 200ps Part-to-Part Skew
- 50ps Output-to-Output Skew
- Differential Design
- $V_{BB}$ Output
- Voltage Compensated Outputs
- $V_{EE}$ Range of –4.5 to –5.5V
- 75kΩ Input Pulldown Resistors

The output voltage swing of the E411 is larger than a standard ECL swing. The 1.2V output swings provide a signal which can be AC coupled into RAMBus compatible input loads. The larger output swings are produced by lowering the $V_{OL}$ of the device. With the exception of the lower $V_{OL}$, the E411 is identical to the MC10E111. Note that the larger output swings eliminate the possibility of temperature compensated outputs, thus the E411 is only available in the 10E style of ECL. In addition, because the $V_{OL}$ is lower than standard ECL, the outputs cannot be terminated to –2.0V. This datasheet provides a few termination alternatives.

The E411 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent $t_{pd}$ distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated, even if only one side is being used. In most applications, all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

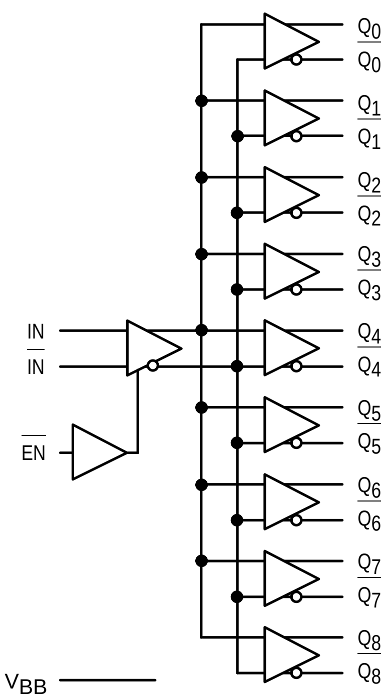
The MC10E411, as with most other ECL devices, can be operated from a positive $V_{CC}$ supply in PECL mode. This allows the E411 to be used for high performance clock distribution in +5.0V systems. Designers can take advantage of the E411's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to Motorola Application Note AN1406/D.



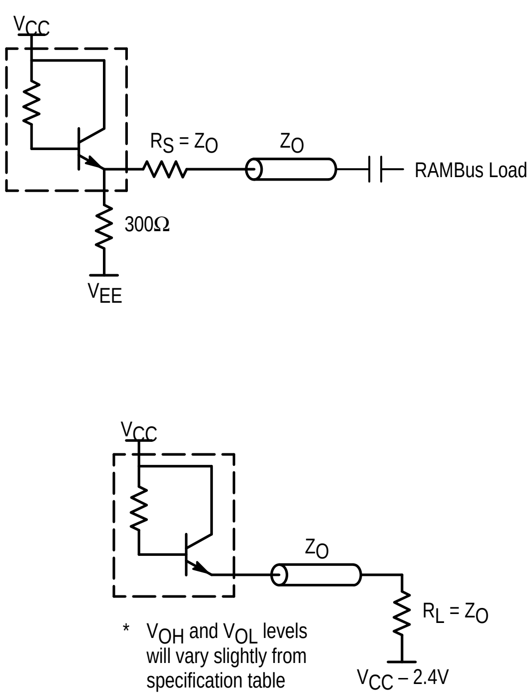

**PIN NAMES**

| Pins | Function |
|---|---|
| IN, $\overline{IN}$ | Differential Input Pair |
| $Q_0$, $Q_0$–$Q_8$, $\overline{Q_8}$ | Differential Outputs |
| $V_{BB}$ | $V_{BB}$ Output |

**LOGIC SYMBOL**




**TERMINATION ALTERNATIVES**



**ECL DC CHARACTERISTICS**

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{OH}$ | Output HIGH Voltage[1] | –1.020 | | –0.840 | –0.980 | –0.890 | –0.810 | –0.910 | | –0.720 | V |
| $V_{OL}$ | Output LOW Voltage[1] | –2.420 | | –2.140 | –2.380 | –2.250 | –2.110 | –2.310 | | –2.020 | V |
| $V_{IH}$ | Input HIGH Voltage | –1.170 | | –0.840 | –1.130 | | –0.810 | –1.060 | | –0.720 | V |
| $V_{IL}$ | Input LOW Voltage | –1.950 | | –1.480 | –1.950 | | –1.480 | –1.950 | | –1.445 | V |
| $V_{BB}$ | Output Reference Voltage | –1.38 | | –1.27 | –1.35 | | –1.25 | –1.31 | | –1.19 | V |
| $V_{EE}$ | Power Supply Voltage | –4.5 | | –5.5 | –4.5 | | –5.5 | –4.5 | | –5.5 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | µA |
| $I_{EE}$ | Power Supply Current | | 55 | 65 | | 55 | 65 | | 55 | 65 | mA |

1. Measured with 300Ω to $V_{EE}$ output pulldown.

**PECL DC CHARACTERISTICS**

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{OH}$ | Output HIGH Voltage[1,2] | 3.98 | | 4.16 | 4.02 | 4.11 | 4.19 | 4.09 | | 4.28 | V |
| $V_{OL}$ | Output LOW Voltage[1,2] | 2.58 | | 2.86 | 2.62 | 2.75 | 2.89 | 2.69 | | 2.98 | V |
| $V_{IH}$ | Input HIGH Voltage[1] | 3.83 | | 4.16 | 3.87 | | 4.19 | 3.94 | | 4.28 | V |
| $V_{IL}$ | Input LOW Voltage[1] | 3.05 | | 3.52 | 3.05 | | 3.52 | 3.05 | | 3.56 | V |
| $V_{BB}$ | Output Reference Voltage[1] | 3.62 | | 3.73 | 3.65 | | 3.75 | 3.69 | | 3.81 | V |
| $V_{CC}$ | Power Supply Voltage | 4.5 | | 5.5 | 4.5 | | 5.5 | 4.5 | | 5.5 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | µA |
| $I_{EE}$ | Power Supply Current | | 55 | 65 | | 55 | 65 | | 55 | 65 | mA |

1. These values are for $V_{CC}$ = 5.0V. Level Specifications will vary 1:1 with $V_{CC}$.
2. Measured with 300Ω to $V_{EE}$ output pulldown.

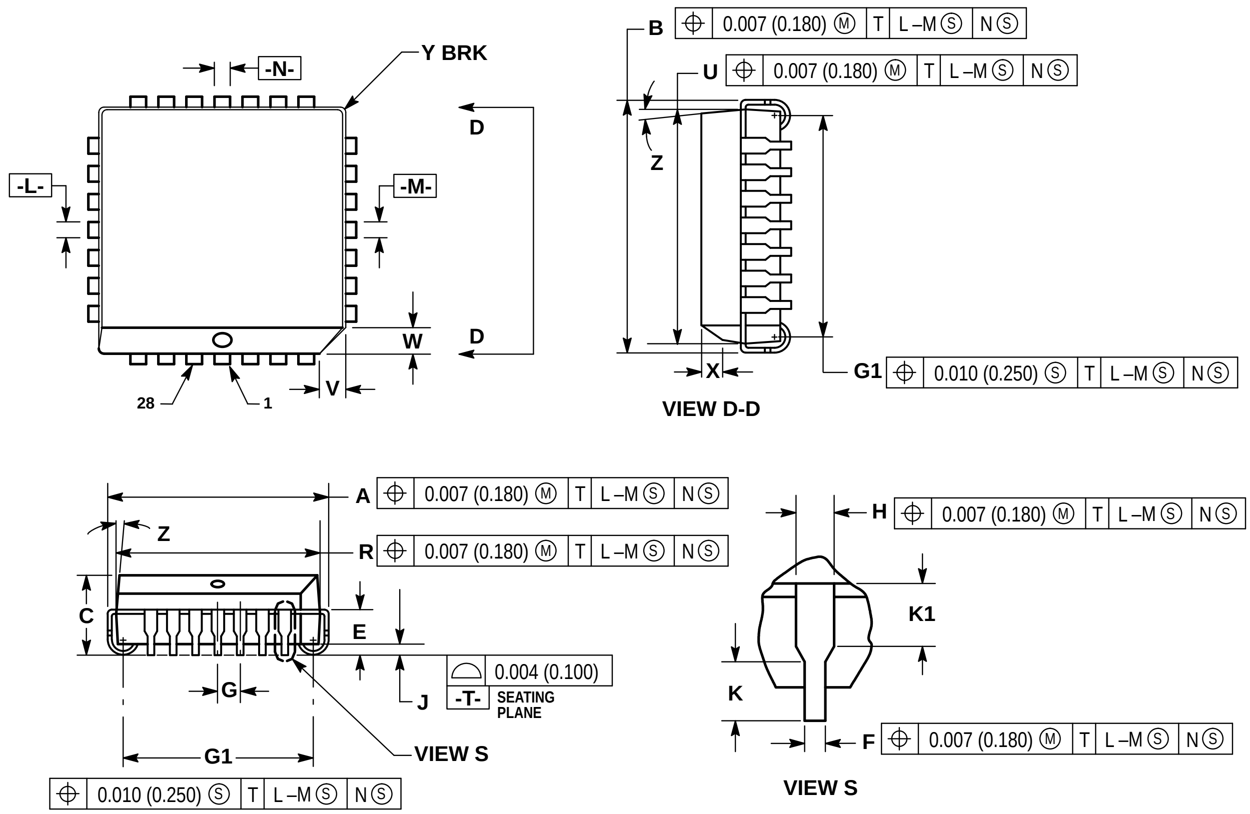
**AC CHARACTERISTICS** ($V_{EE}$ = $V_{EE}$ (min) to $V_{EE}$ (max); $V_{CC}$ = $V_{CCO}$ = GND)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay to Output<br>IN (differential)<br>IN (single-ended)<br>EN to Q | <br>400<br>350<br>450 | | <br>600<br>650<br>850 | <br>430<br>380<br>450 | | <br>630<br>680<br>850 | <br>500<br>450<br>450 | | <br>700<br>750<br>850 | ps | <br>Note 1.<br>Note 2. |
| $t_s$ | Setup Time $\overline{\text{EN}}$ to IN | 200 | 0 | | 200 | 0 | | 200 | 0 | | ps | Note 3. |
| $t_H$ | Hold Time IN to $\overline{\text{EN}}$ | 0 | –200 | | 0 | –200 | | 0 | –200 | | ps | Note 4. |
| $t_R$ | Release Time $\overline{\text{EN}}$ to IN | 300 | 100 | | 300 | 100 | | 300 | 100 | | ps | Note 5. |
| $t_{skew}$ | Within-Device Skew<br>Part-to-Part Skew (Diff) | | | 50<br>200 | | | 50<br>200 | | | 50<br>200 | ps | Note 6. |
| $V_{PP}$ | Minimum Input Swing | 250 | | | 250 | | | 250 | | | mV | Note 7. |
| $V_{CMR}$ | Common Mode Range | –1.6 | | –0.4 | –1.6 | | –0.4 | –1.6 | | –0.4 | V | Note 8. |
| $t_r/t_f$ | Output Rise/Fall Time | 275 | | 600 | 275 | | 600 | 275 | | 600 | ps | 20%–80% |

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
3. The setup time is the minimum time that $\overline{\text{EN}}$ must be asserted prior to the next transition of IN/$\overline{\text{IN}}$ to prevent an output response greater than ±75 mV to that IN/$\overline{\text{IN}}$ transition (see Figure 1).
4. The hold time is the minimum time that $\overline{\text{EN}}$ must remain asserted after a negative going IN or a positive going $\overline{\text{IN}}$ to prevent an output response greater than ±75 mV to that IN/$\overline{\text{IN}}$ transition (see Figure 2).
5. The release time is the minimum time that $\overline{\text{EN}}$ must be deasserted prior to the next IN/$\overline{\text{IN}}$ transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (see Figure 3).
6. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
7. $V_{PP}$(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The $V_{PP}$(min) is AC limited for the E411 as a differential input as low as 50 mV will still produce full ECL levels at the output.
8. $V_{CMR}$ is defined as the range within which the $V_{IH}$ level may vary, with the device still meeting the propagation delay specification. The $V_{IL}$ level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to $V_{PP}$(min).

## OUTLINE DIMENSIONS

**FN SUFFIX**
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE D




NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.485 | 0.495 | 12.32 | 12.57 |
| B | 0.485 | 0.495 | 12.32 | 12.57 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.019 | 0.33 | 0.48 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | — | 0.51 | — |
| K | 0.025 | — | 0.64 | — |
| R | 0.450 | 0.456 | 11.43 | 11.58 |
| U | 0.450 | 0.456 | 11.43 | 11.58 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | — | 0.020 | — | 0.50 |
| Z | 2° | 10° | 2° | 10° |
| G1 | 0.410 | 0.430 | 10.42 | 10.92 |
| K1 | 0.040 | — | 1.02 | — |

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