Quad Driver

The MC10E/100E112 is a quad driver with two pairs of OR/NOR outputs from each gate, and a common, buffered enable input. Using the data inputs the device can serve as an ECL memory address fan-out driver. Using just the enable input, the device serves as a clock driver, although the MC10E/100E111 is designed specifically for this purpose, and offers lower skew than the E112. For memory address driver applications where scan capabilities are required, please refer to the E212 device.

- 600ps Max. Propagation Delay
- Common Enable Input
- Extended 100E VEE Range of 4.2V to 5.46V
- 75kΩ Input Pulldown Resistors



* All V_{CC} and V_{CCO} pins are tied together on the die.

PIN NAMES

Pin	Function
$\frac{D_0 - D_3}{EN}$	Data Inputs
EN	Enable Input
Q _{na} , Q _{nb}	True Outputs
Q _{na} , Q _{nb}	Inverting Outputs

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QUAD DRIVER



LOGIC DIAGRAM





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MC10E112 MC100E112

DC CHARACTERISTICS (VEE = VEE(min) to VEE(max); VCC = VCCO = GND)

		0°C		25°C			85°C					
Symbol	Characteristic	min	typ	max	min	typ	max	min	typ	max	Unit	Condition
ЧΗ	Input HIGH Current										μA	
	D			200			200			200		
	EN			200			200			200		
IEE	Power Supply Current										mA	
	10E		47	56		47	56		47	56		
	100E		47	56		47	56		54	65		

AC CHARACTERISTICS (VEE = VEE(min) to VEE(max); VCC = VCCO = GND)

		O°C		25°C			85°C					
Symbol	Characteristic	min	typ	max	min	typ	max	min	typ	max	Unit	Condition
^t PLH ^t PHL	Propagation Delay to Output D EN	200 275	400 450	600 675	200 275	400 450	600 675	200 275	400 450	600 675	ps	
^t SKEW	Within-Devi <u>ce S</u> kew Dn to Qn, Qn Qna to Qnb		80 40			80 40			80 40		ps	1 2
t _r t _f	Rise/Fall Times 20 - 80%	275	425	700	275	425	700	275	425	700	ps	

Within-device skew is defined as identical transitions on similar paths through a device.
Skew defined between common OR or common NOR outputs of a single gate.





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