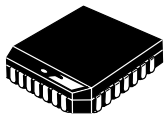
Low-Voltage 1:9 Differential ECL/PECL Clock Driver

MC100LVE111

LOW-VOLTAGE 1:9 DIFFERENTIAL ECL/PECL CLOCK DRIVER

The MC100LVE111 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. The MC100LVE111's function and performance are similar to the popular MC100E111, with the added feature of low voltage operation. It accepts one signal input, which can be either differential or single-ended if the V_{BB} output is used. The signal is fanned out to 9 identical differential outputs.

- 200ps Part-to-Part Skew
- 50ps Output-to-Output Skew
- Differential Design
- V_{BB} Output
- Voltage and Temperature Compensated Outputs
- Low Voltage V_{EE} Range of –3.0 to –3.8V
- 75kΩ Input Pulldown Resistors



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PLASTIC PACKAGE
CASE 776-02

The LVE111 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within a device, and empirical modeling is used to determineprocess control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The MC100LVE111, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVE111 to be used for high performance clock distribution in +3.3V systems. Designers can take advantage of the LVE111's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For systems incorporating GTL, parallel termination offers the lowest power by taking advantage of the 1.2V supply as a terminating voltage. For more information on using PECL, designers should refer to Motorola Application Note AN1406/D.

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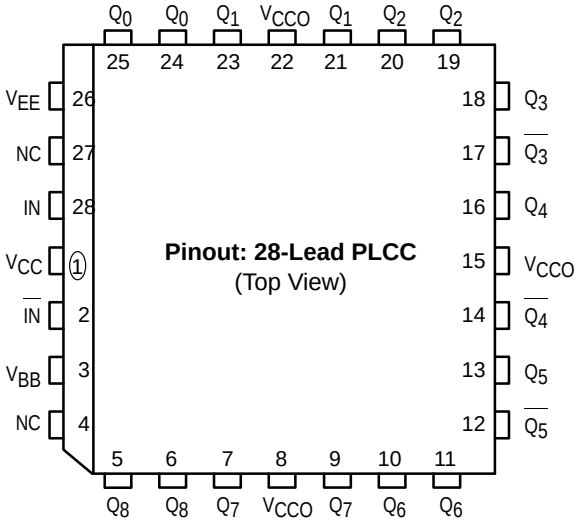
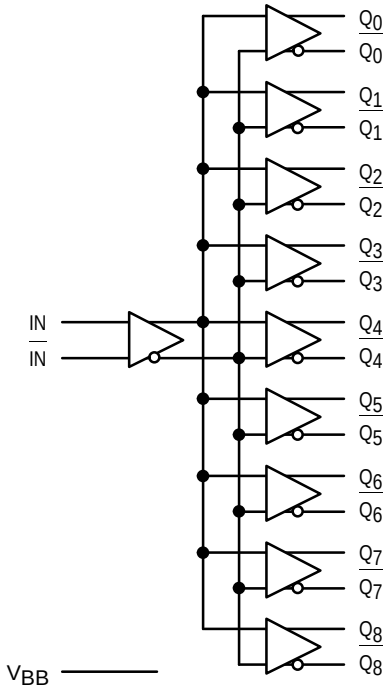


PIN NAMES

Pins	Function
IN, $\overline{IN}$	Differential Input Pair
Q_0, Q_0–Q_8, $\overline{Q_8}$	Differential Outputs
V_{BB}	V_{BB} Output

LOGIC SYMBOL



ECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	V
V_{OL}	Output LOW Voltage	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	V
V_{IH}	Input HIGH Voltage	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	V
V_{IL}	Input LOW Voltage	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	V
V_{BB}	Output Reference Voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{EE}	Power Supply Voltage	–3.0		–3.8	–3.0		–3.8	–3.0		–3.8	–3.0		–3.8	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{EE}	Power Supply Current		55	66		55	66		55	66		65	78	mA

PECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	2.275	2.345	2.420	2.275	2.345	2.420	2.275	2.345	2.420	2.275	2.345	2.420	V
V_{OL}	Output LOW Voltage[1]	1.490	1.595	1.680	1.490	1.595	1.680	1.490	1.595	1.680	1.490	1.595	1.680	V
V_{IH}	Input HIGH Voltage[1]	2.135		2.420	2.135		2.420	2.135		2.420	2.135		2.420	V
V_{IL}	Input LOW Voltage[1]	1.490		1.825	1.490		1.825	1.490		1.825	1.490		1.825	V
V_{BB}	Output Reference Voltage[1]	1.92		2.04	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{CC}	Power Supply Voltage	3.0		3.8	3.0		3.8	3.0		3.8	3.0		3.8	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{EE}	Power Supply Current		55	66		55	66		55	66		65	78	mA

1. These values are for V_{CC} = 3.3V. Level Specifications will vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single-ended)	 400 350		 650 700	 435 385		 625 675	 440 390		 630 680	 445 395		 635 685	ps	 Note 1 Note 2
t_{skew}	Within-Device Skew Part-to-Part Skew (Diff)			50 250			50 200			50 200			50 200	ps	Note 3
V_{PP}	Minimum Input Swing	500			500			500			500			mV	Note 4
V_{CMR}	Common Mode Range	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	V	Note 5
t_r/t_f	Output Rise/Fall Time	200		600	200		600	200		600	200		600	ps	20%–80%

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
3. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
4. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the E111 as a differential input as low as 50 mV will still produce full ECL levels at the output.
5. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

OUTLINE DIMENSIONS

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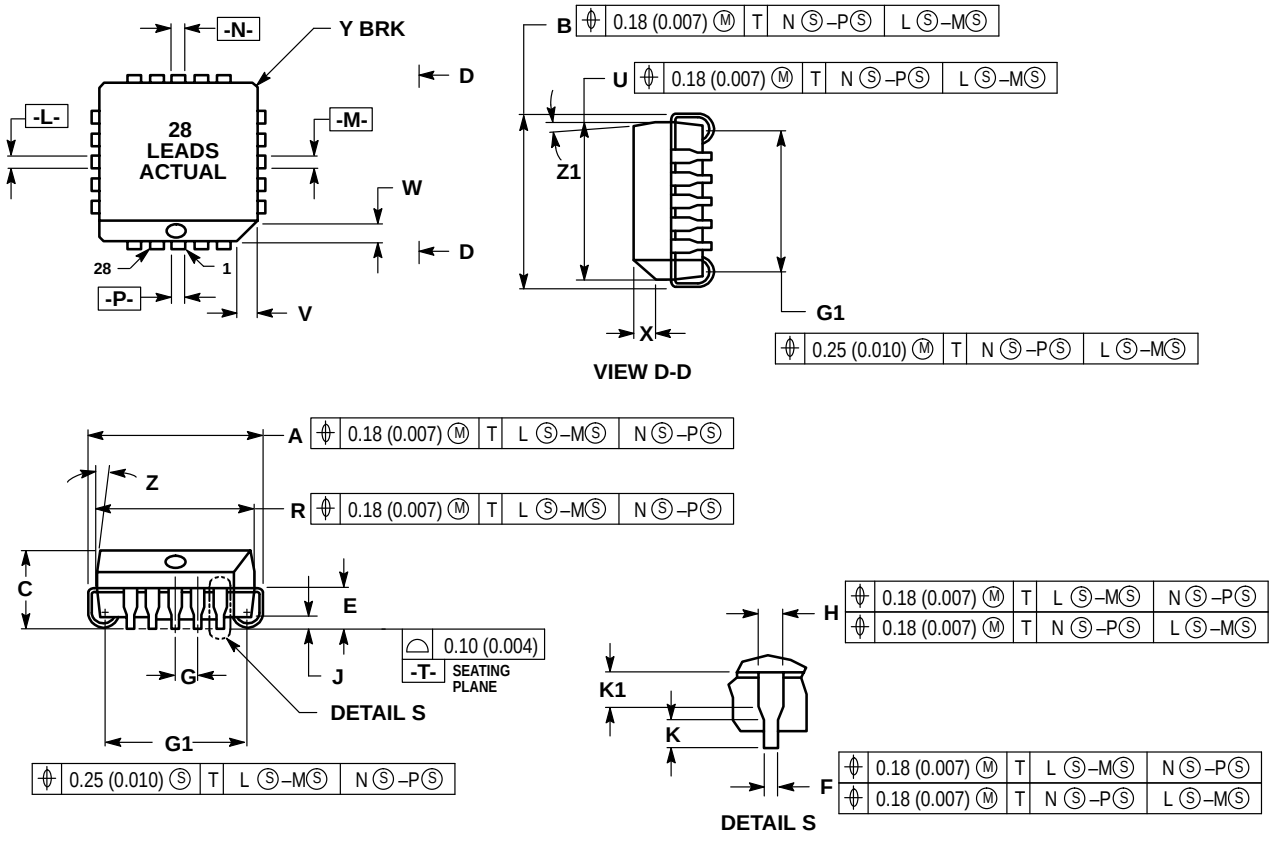
PLASTIC PACKAGE
CASE 776-02
ISSUE D



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	10.42	10.92	0.410	0.430
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.
7. 776-01 IS OBSOLETE, NEW STANDARD 776-02.

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