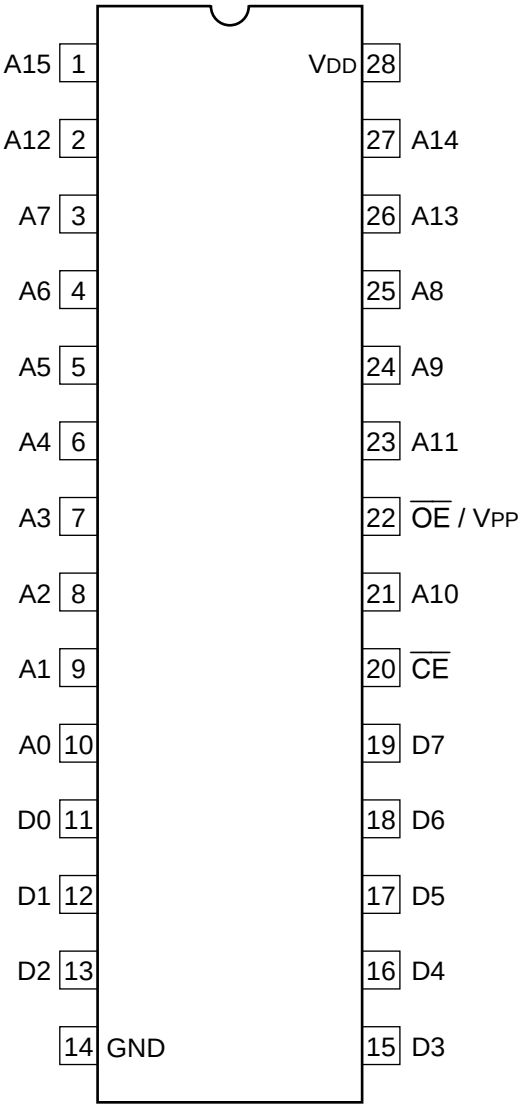
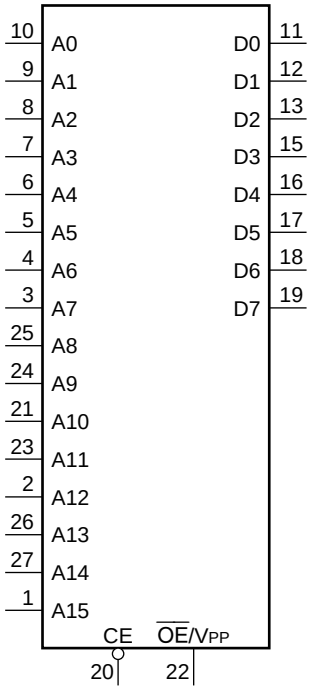
C-MOS 512 K (65,536 × 8)-BIT EPROM

—TOP VIEW—





A0 - A15	:	ADDRESS INPUTS
$\overline{CE}$	:	CHIP ENABLE INPUT
D0 - D7	:	DATA OUTPUTS
$\overline{OE}$	:	OUTPUT ENABLE INPUT
V_{PP}	:	PROGRAM POWER SUPPLY

An	CE	$\overline{OE}$/VPP	VDD	Dn	FUNCTION
AIN	0	0	+5 V	DOUT	READ
AIN	0	1	+5 V	HI-Z	OUTPUT DISABLE
×	1	×	+5 V	HI-Z	STANDBY
AIN	0	+12.5 V	+6 V	DIN	PGM
AIN	0	0	+6 V	DOUT	PGM VERIFY
×	1	+12.5 V	+6 V	HI-Z	PGM INH

0 : LOW LEVEL
1 : HIGH LEVEL
× : DON'T CARE
HI-Z : HIGH IMPEDANCE