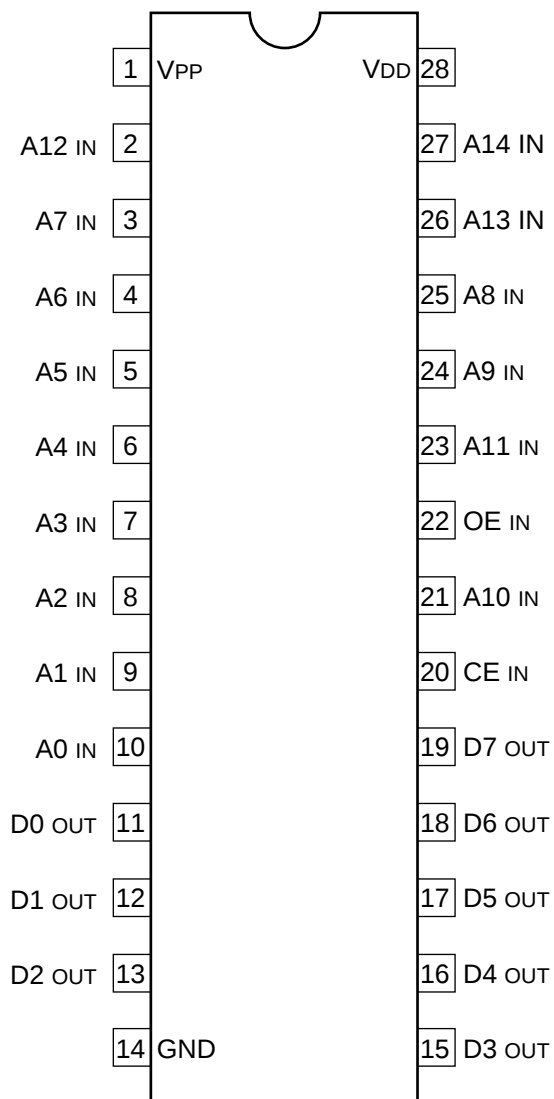
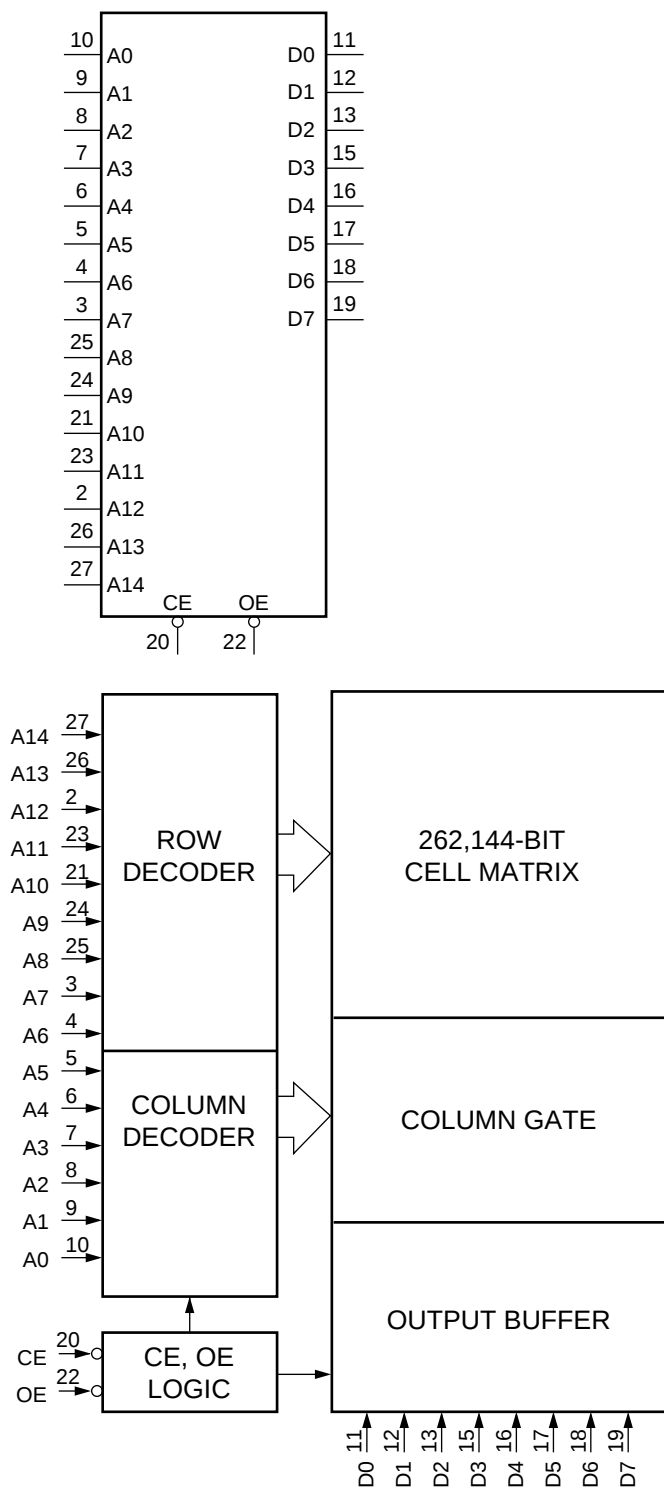


C-MOS 256 K (32 K × 8)-BIT UV ERASABLE PROM WITH 3-STATE OUTPUTS

—TOP VIEW—



A0 - A14 : ADDRESS INPUTS
 $\overline{\text{CE}}$: CHIP ENABLE INPUT
 D0 - D7 : DATA OUTPUTS
 $\overline{\text{OE}}$: OUTPUT ENABLE INPUT
 VPP : PROGRAM POWER SUPPLY



An	CE	OE	VDD	VPP	Dn	FUNCTION
An	0	0	+5 V	+5 V	D OUT	READ
An	0	1	+5 V	+5 V	HI-Z	OUTPUT DISABLE
x	1	x	+5 V	+5 V	HI-Z	STANDBY
An	0	1	+6 V	+12.5 V	D IN	PGM
An	1	0	+6 V	+12.5 V	D OUT	PGM VERIFY (1)
An	0	0	+6 V	+12.5 V	D OUT	PGM VERIFY (2)
x	1	1	+6 V	+12.5 V	HI-Z	PGM INH
AO	0	0	+5 V	+5 V	DEVICE CODE	ELECTRONIC SIGNATURE*

0 : LOW LEVEL
 1 : HIGH LEVEL
 x : DON'T CARE
 HI-Z : HIGH IMPEDANCE

* SEE FOLLOWING DESCRIPTION

ELECTRONIC SIGNATURE FOR P ROM WRITER
 ADDRESS SETTINGS IN READ MODE

A1 - A8	A9	A10 - A13	A14, Vpp
0	12 V	0	1

	AO	CODE DATA								
		D7	D6	D5	D4	D3	D2	D1	D0	
MAKER CODE	0	0	0	0	0	0	1	0	0	04H
DEVICE CODE	1	0	1	1	0	0	0	1	0	62H