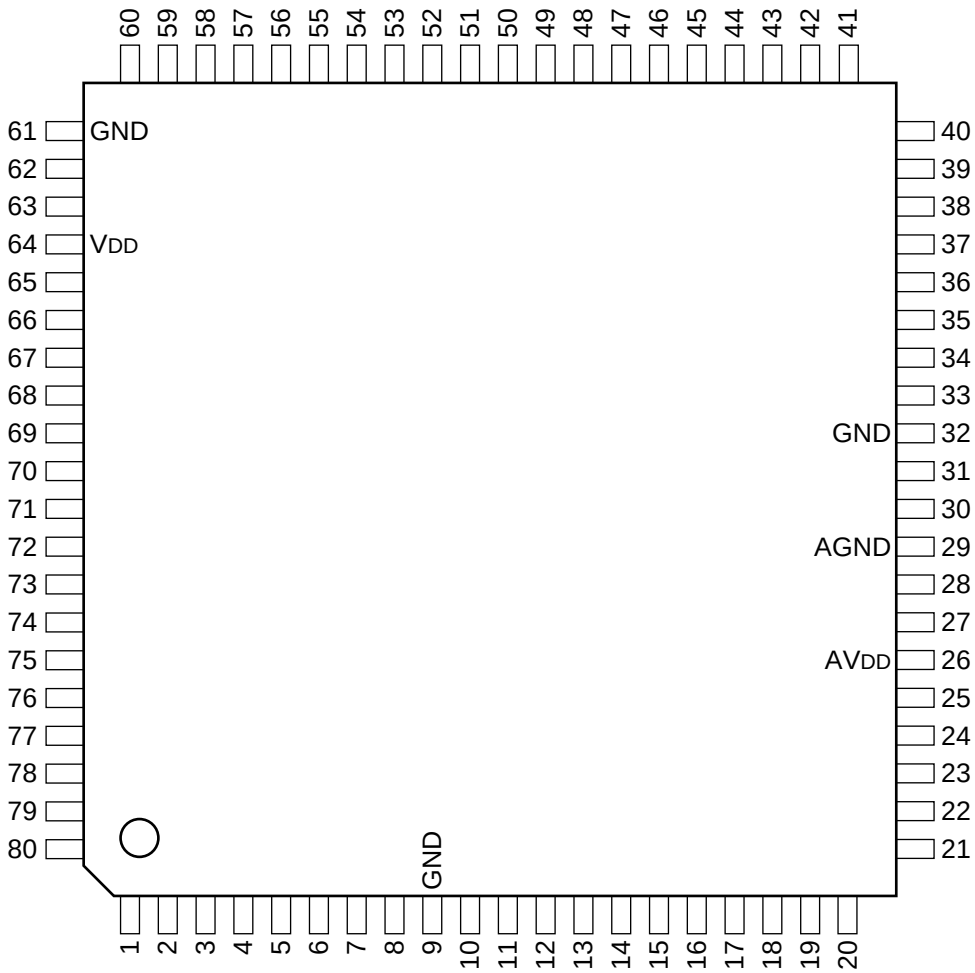
C-MOS 16-BIT 1-CHIP MICROCONTROLLER

—TOP VIEW—



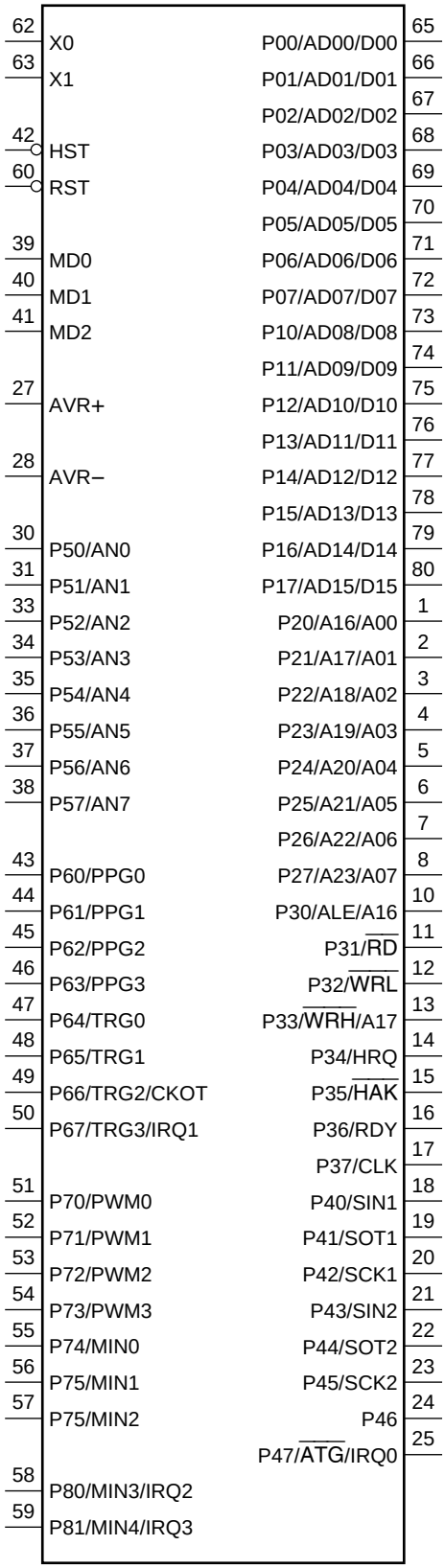
PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I/O	P20/A16/A00	21	I/O	P43/SIN2	41	I	MD2	61	—	GND
2	I/O	P21/A17/A01	22	I/O	P44/SOT2	42	I	$\overline{\text{HST}}$	62	I	X0
3	I/O	P22/A18/A02	23	I/O	P45/SCK2	43	I/O	P60/PPG0	63	I	X1
4	I/O	P23/A19/A03	24	I/O	P46	44	I/O	P61/PPG1	64	—	V_{DD}
5	I/O	P24/A20/A04	25	I/O	P47/$\overline{\text{ATG}}$/IRQ0	45	I/O	P62/PPG2	65	I/O	P00/AD00/D00
6	I/O	P25/A21/A05	26	—	AV_{DD}	46	I/O	P63/PPG3	66	I/O	P01/AD01/D01
7	I/O	P26/A22/A06	27	I	AVR+	47	I/O	P64/TRG0	67	I/O	P02/AD02/D02
8	I/O	P27/A23/A07	28	I	AVR−	48	I/O	P65/TRG1	68	I/O	P03/AD03/D03
9	—	GND	29	—	A_{GND}	49	I/O	P66/TRG2/CKOT	69	I/O	P04/AD04/D04
10	I/O	P30/ALE/A16	30	I/O	P50/AN0	50	I/O	P67/TRG3/IRQ1	70	I/O	P05/AD05/D05
11	I/O	P31/$\overline{\text{RD}}$	31	I/O	P51/AN1	51	I/O	P70/PWM0	71	I/O	P06/AD06/D06
12	I/O	P32/$\overline{\text{WRL}}$	32	—	GND	52	I/O	P71/PWM1	72	I/O	P07/AD07/D07
13	I/O	P33/$\overline{\text{WRH}}$/A17	33	I/O	P52/AN2	53	I/O	P72/PWM2	73	I/O	P10/AD08/D08
14	I/O	P34/HRQ	34	I/O	P53/AN3	54	I/O	P73/PWM3	74	I/O	P11/AD09/D09
15	I/O	P35/$\overline{\text{HAK}}$	35	I/O	P54/AN4	55	I/O	P74/MIN0	75	I/O	P12/AD10/D10
16	I/O	P36/RDY	36	I/O	P55/AN5	56	I/O	P75/MIN1	76	I/O	P13/AD11/D11
17	I/O	P37/CLK	37	I/O	P56/AN6	57	I/O	P76/MIN2	77	I/O	P14/AD12/D12
18	I/O	P40/SIN1	38	I/O	P57/AN7	58	I/O	P80/MIN3/IRQ2	78	I/O	P15/AD13/D13
19	I/O	P41/SOT1	39	I	MD0	59	I/O	P81/MIN4/IRQ3	79	I/O	P16/AD14/D14
20	I/O	P42/SCK1	40	I	MD1	60	I	$\overline{\text{RST}}$	80	I/O	P17/AD15/D15

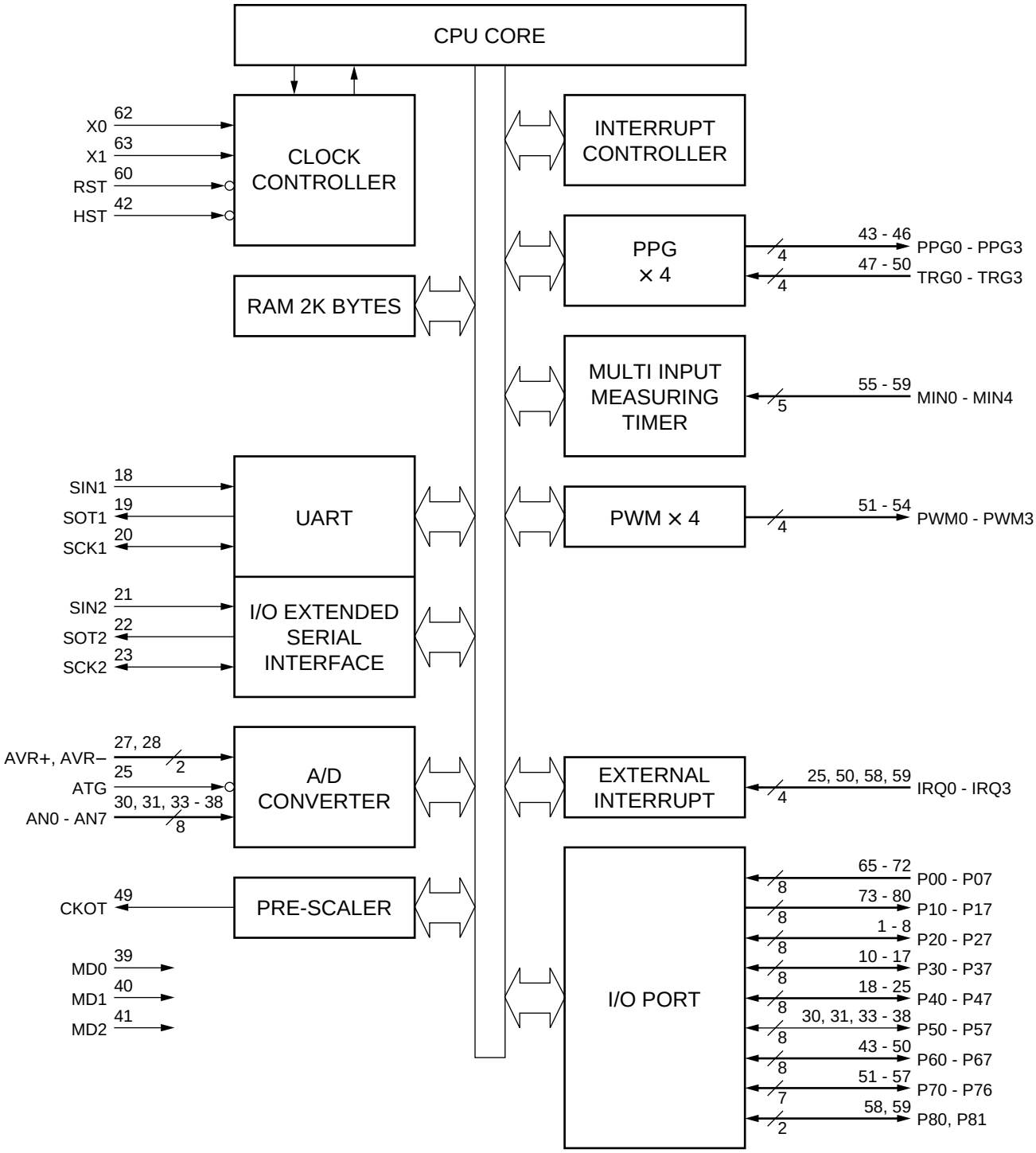
INPUT

AVR+, AVR–	;	EXTERNAL REFERENCE VOLTAGE FOR A/D CONVERTER
$\overline{HST}$	;	HARDWARE STANDBY
MD0 - MD2	;	MB90T736 OPERATION MODE SELECT
$\overline{RST}$	;	RESET
X0, X1	;	CRYSTAL CONNECTION

INPUT/OUTPUT

P00/AD00/D00 - P07/AD07/A07	;	I/O PORT 00 - 07 (SINGLE CHIP MODE) ADDRESS/DATA BUS LINE 0 - 7 (MULTIPLEX BUS MODE) DATA BUS LINE 0 - 7 (NON-MULTIPLEX BUS MODE)
P10/AD08/A08 - P17/AD15/A15	;	I/O PORT 10 - 17 (SINGLE CHIP MODE) ADDRESS/DATA BUS LINE 8 - 15 (MULTIPLEX BUS MODE) ADDRESS BUS LINE 8 - 15 (NON-MULTIPLEX BUS MODE)
P20/A16/A00 - P27/A23/A07	;	I/O PORT 20 - 27 (SINGLE CHIP MODE) ADDRESS BUS LINE 16 - 23 (MULTIPLEX BUS MODE) ADDRESS BUS LINE 0 - 7 (NON-MULTIPLEX BUS MODE)
P30/ALE/A16	;	I/O PORT 30 (SINGLE CHIP MODE) ADDRESS LATCH ENABLE OUT (MULTIPLEX BUS MODE) ADDRESS BUS LINE 16 (NON-MULTIPLEX BUS MODE)
P31/$\overline{RD}$	;	I/O PORT 31 (SINGLE CHIP MODE) READ STROBE OUT (EXCEPT SINGLE CHIP MODE)
P32/$\overline{WRL}$	;	I/O PORT 32 (SINGLE CHIP MODE) LOWER DATA WRITE STROBE OUT (EXCEPT SINGLE CHIP MODE)
P33/$\overline{WRH}$/A17	;	I/O PORT 33 (SINGLE CHIP MODE) UPPER DATA WRITE STROBE OUT (MULTIPLEX BUS MODE) ADDRESS BUS LINE 17 (NON-MULTIPLEX BUS MODE)
P34/HRQ	;	I/O PORT 34 (SINGLE CHIP MODE) HOLD REQUEST IN (EXCEPT SINGLE CHIP MODE)
P35/$\overline{HAK}$	;	I/O PORT 35 (SINGLE CHIP MODE) HOLD ACKNOWLEDGE OUT (EXCEPT SINGLE CHIP MODE)
P36/RDY	;	I/O PORT 36 (SINGLE CHIP MODE) EXTERNAL READY IN (EXCEPT SINGLE CHIP MODE)
P37/CLK	;	I/O PORT 37 (SINGLE CHIP MODE) MECHAN-CYCLE CLOCK OUT (EXCEPT SINGLE CHIP MODE)
P40/SIN1	;	I/O PORT 40 SERIAL DATA IN WHEN UART OPERATION MODE
P41/SOT1	;	I/O PORT 41 SERIAL DATA OUT OF UART
P42/SCK1	;	I/O PORT 42 SERIAL CLOCK OUT WHEN UART OPERATION IS EXTERNAL CLOCK MODE
P43/SIN2	;	I/O PORT 43 SERIAL DATA IN WHEN EXTENDED I/O SERIAL OPERATION MODE
P44/SOT2	;	I/O PORT 44 SERIAL DATA OUT OF EXTENDED I/O SERIAL I/F
P45/SCK2	;	I/O PORT 45 SERIAL CLOCK OUT WHEN EXTENDED I/O SERIAL OPERATION MODE
P46	;	I/O PORT 46
P47/$\overline{ATG}$/IRQ0	;	I/O PORT 47 (INTERRUPT REQUEST O IN) A/D CONVERTER STARTING TRIGGER IN
P50/AN0 - P57/AN7	;	I/O PORT 50 - 57 ANALOG IN PORT 0 - 7 WHEN A/D CONVERTER OPERATION MODE
P60/PPG0 - P63/PPG3	;	I/O PORT 60 - 63 PPG OUT 0 - 3 WHEN PPG OPERATION MODE
P64/TRG0, P65/TRG1	;	I/O PORT 64, 65 PPG 0/1 STARTING TRIGGER IN WHEN PPG OPERATION IS EXTERNAL STARTING TRIGGER MODE
P66/TRG2/CKOT	;	I/O PORT 66 PPG 2 STARTING TRIGGER IN WHEN PPG OPERATION IS EXTERNAL STARTING TRIGGER MODE CLOCK OUT
P67/TRG3/IRQ1	;	I/O PORT 67 (INTERRUPT REQUEST 1 IN) PPG 3 STARTING TRIGGER IN WHEN PPG OPERATION IS EXTERNAL STARTING TRIGGER MODE
P70/PWM0 - P73/PWM3	;	I/O PORT 70 - 73 PWM OUT 0 - 3 WHEN PWM OPERATION MODE
P74/MIN0 - P76/MIN2	;	I/O PORT 74 - 76 MIC TIMER 0/1/2 START/END TRIGGER IN WHEN MIC TIMER OPERATION MODE
P80/MIN3/IRQ2, P81/MIN4/IRQ3	;	I/O PORT 80, 81 (INTERRUPT REQUEST 2, 3 IN) MIC TIMER 3/4 START/END TRIGGER IN WHEN MIC TIMER OPERATION MODE


62 X0
63 X1
42 HST
60 RST
39 MD0
40 MD1
41 MD2
27 AVR+
28 AVR−
30 P50/AN0
31 P51/AN1
33 P52/AN2
34 P53/AN3
35 P54/AN4
36 P55/AN5
37 P56/AN6
38 P57/AN7
43 P60/PPG0
44 P61/PPG1
45 P62/PPG2
46 P63/PPG3
47 P64/TRG0
48 P65/TRG1
49 P66/TRG2/CKOT
50 P67/TRG3/IRQ1
51 P70/PWM0
52 P71/PWM1
53 P72/PWM2
54 P73/PWM3
55 P74/MIN0
56 P75/MIN1
57 P75/MIN2
58 P80/MIN3/IRQ2
59 P81/MIN4/IRQ3
65 P00/AD00/D00
66 P01/AD01/D01
67 P02/AD02/D02
68 P03/AD03/D03
69 P04/AD04/D04
70 P05/AD05/D05
71 P06/AD06/D06
72 P07/AD07/D07
73 P10/AD08/D08
74 P11/AD09/D09
75 P12/AD10/D10
76 P13/AD11/D11
77 P14/AD12/D12
78 P15/AD13/D13
79 P16/AD14/D14
80 P17/AD15/D15
1 P20/A16/A00
2 P21/A17/A01
3 P22/A18/A02
4 P23/A19/A03
5 P24/A20/A04
6 P25/A21/A05
7 P26/A22/A06
8 P27/A23/A07
10 P30/ALE/A16
11 P31/RD
12 P32/WRL
13 P33/WRH/A17
14 P34/HRQ
15 P35/HAK
16 P36/RDY
17 P37/CLK
18 P40/SIN1
19 P41/SOT1
20 P42/SCK1
21 P43/SIN2
22 P44/SOT2
23 P45/SCK2
24 P46
25 P47/ATG/IRQ0


CPU CORE
CLOCK CONTROLLER
X0
62
X1
63
RST
60
HST
42
INTERRUPT CONTROLLER
PPG × 4
43 - 46
PPG0 - PPG3
47 - 50
TRG0 - TRG3
4
4
RAM 2K BYTES
MULTI INPUT MEASURING TIMER
55 - 59
MIN0 - MIN4
5
UART
SIN1
18
SOT1
19
SCK1
20
PWM × 4
51 - 54
PWM0 - PWM3
4
I/O EXTENDED SERIAL INTERFACE
SIN2
21
SOT2
22
SCK2
23
A/D CONVERTER
AVR+, AVR−
27, 28
2
ATG
25
AN0 - AN7
30, 31, 33 - 38
8
EXTERNAL INTERRUPT
25, 50, 58, 59
IRQ0 - IRQ3
4
PRE-SCALER
CKOT
49
MD0
39
MD1
40
MD2
41
I/O PORT
65 - 72
P00 - P07
73 - 80
P10 - P17
1 - 8
P20 - P27
10 - 17
P30 - P37
18 - 25
P40 - P47
30, 31, 33 - 38
P50 - P57
43 - 50
P60 - P67
51 - 57
P70 - P76
58, 59
P80, P81
8
8
8
8
8
8
8
7
2