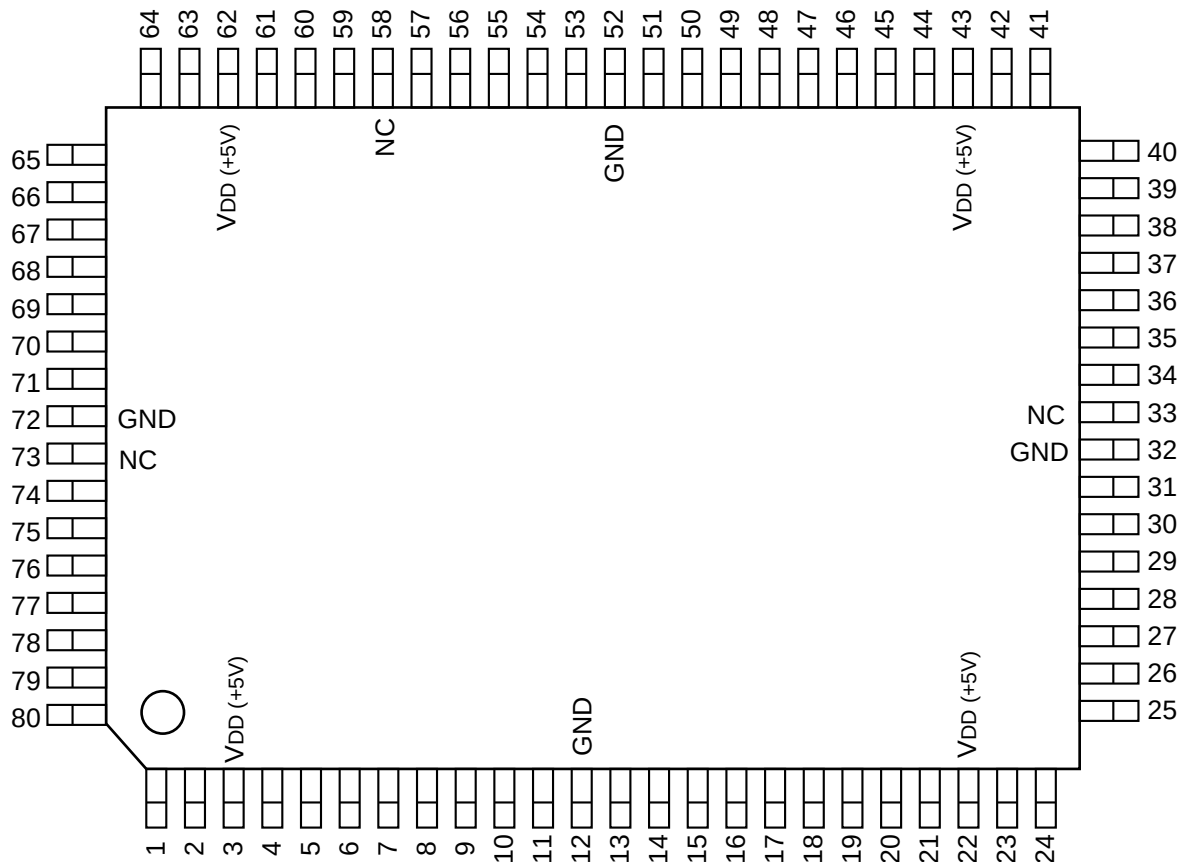

C-MOS ENCAPSULATED PERIPHERAL PROCESSOR
—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	GATE0	21	I	$\overline{\text{CS0}}$	41	I	IRQ13	61	O	$\overline{\text{DTR}}$
2	I	CLK0	22	—	VDD	42	I	IRQ12	62	—	VDD
3	—	VDD	23	I/O	C12	43	—	VDD	63	O	$\overline{\text{RTS}}$
4	I/O	DB7	24	I/O	C02	44	I	IRQ11	64	I	$\overline{\text{DSR}}$
5	I/O	DB6	25	I/O	C11	45	I	IRQ10	65	I	RST
6	I/O	DB5	26	I/O	C01	46	I	IRQ07	66	O	TRNDT
7	I/O	DB4	27	I/O	C10	47	I	IRQ06	67	O	TRNEMP/STI
8	I/O	DB3	28	I/O	$\overline{\text{C00}}$	48	I	IRQ05	68	I	$\overline{\text{CTS}}$
9	I/O	DB2	29	I	$\overline{\text{INTA1}}$	49	I	IRQ04	69	I/O	SYNC/BRK
10	I/O	DB1	30	I	$\overline{\text{INTA0}}$	50	I	IRQ03	70	O	TRNRDY
11	I/O	DB0	31	O	INT1	51	I	IRQ02	71	I	CK
12	—	GND	32	—	GND	52	—	GND	72	—	GND
13	I	A1	33	—	NC	53	I	IRQ01	73	—	NC
14	I	A0	34	O	INT0	54	I	IRQ00	74	O	OUT2
15	I	$\overline{\text{W}}$	35	I/O	SLCT1	55	I	RSLCT	75	I	GATE2
16	I	$\overline{\text{R}}$	36	I/O	SLCT0	56	I	$\overline{\text{RCVDT}}$	76	I	CLK2
17	I	$\overline{\text{CS4}}$	37	I	IRQ17	57	I	TRNCLK	77	O	OUT1
18	I	$\overline{\text{CS3}}$	38	I	IRQ16	58	—	NC	78	I	GATE1
19	I	$\overline{\text{CS2}}$	39	I	IRQ15	59	O	$\overline{\text{RCVRDY}}$	79	I	CLK1
20	I	$\overline{\text{CS1}}$	40	I	IRQ14	60	I	RCVCLK	80	O	OUT0

14	A0	DB0	11
13	A1	DB1	10
21	CS0	DB2	9
20	CS1	DB3	8
19	CS2	DB4	7
18	CS3	DB5	6
17	CS4	DB6	5
		DB7	4
54	IRQ00		
53	IRQ01		
51	IRQ02	CO0	28
50	IRQ03	CO1	26
49	IRQ04	CO2	24
48	IRQ05	SLCT0	36
47	IRQ06	INT0	34
46	IRQ07		
30	INTA0		
45	IRQ10	C10	27
44	IRQ11	C11	25
42	IRQ12	C12	23
41	IRQ13	SLCT1	35
40	IRQ14	INT1	31
39	IRQ15		
38	IRQ16		
37	IRQ17		
29	INTA1		
64	DSR	DTR	61
68	CTS	RTS	63
56	RCVDT	TRNDY	66
69	SYNC/BRK	TRNRDY	70
55	RSLCT	RCVRDY	59
60	RCVCLK	TRNEMP/STI	67
57	TRNCLK		
1	GATE 0	OUT0	80
78	GATE 1	OUT1	77
75	GATE 2	OUT2	74
2	CLK 0		
79	CLK 1		
76	CLK 2		
15	W		
16	R		
65	RST		
71	> CK		

A0, A1 ; ADDRESS BUS
 C00-C02 ; CASCADE CONTROL
 CLK0-CLK2 ; CLOCK IN
 CK ; CLOCK FOR REFERENCE OF TIMING
 CS0-CS4 ; CHIP SELECT
 CTS ; CLEAR TO SEND
 DB0-DB7 ; DATA BUS
 DSR ; DATA SET READY
 DTR ; DATA TERMINAL READY
 GATE0-GATE2 ; GATE IN
 INT0, INT1 ; INTERRUPT
 INTA0, INTA1 ; INTERRUPT ACKNOWLEDGE
 IRQ00-IRQ07 ; INTERRUPT REQUESTS
 IRQ10-IRQ17 ; INTERRUPT REQUESTS
 OUT1-OUT2 ; COUNT OUT
 R ; READ
 RCVCLK ; RECEIVER CLOCK
 RCVDT ; RECEIVE DATA
 RCVRDT ; RECEIVER READY
 RSLCT ; REGISTER SELECT
 RST ; RESET
 RTS ; REQUEST TO SEND
 SLCT0, SLCT1 ; SELECT
 SYNC/BRK ; SYNCHRONIZATION CHARACTER/
 BREAK CODE DETECT
 TRNCLK ; TRANSMIT CLOCK
 TRNDT ; TRANSMIT DATA
 TRNEMP/STI ; TRANSMITTER EMPTY/BAUD
 RATE CLOCK OUT
 TRNRDT ; TRANSMIT READY
 W ; WRITE

