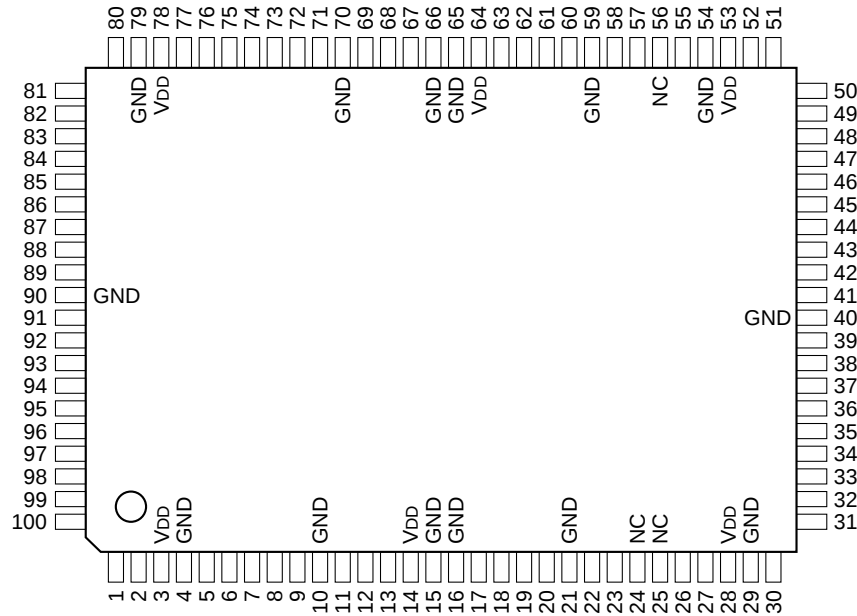


C-MOS SCSI-2 PROTOCOL CONTROLLER

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	WE (LDS)	26	I	IOWR (DMLDS)	51	I	DACK	76	I	A4
2	I	RD (R/W)	27	I	IORD (DMR/W)	52	O	DREQ	77	I	CS0
3	—	VDD	28	—	VDD	53	—	VDD	78	—	VDD
4	—	GND	29	—	GND	54	—	GND	79	—	GND
5	I	CLK	30	I	DMA0	55	I	TP	80	I	CS1
6	I	RESET	31	I/O	LDMDP	56	—	—	81	I/O	LDP
7	O	INT (INT)	32	I/O	DMD0	57	I	TEST2	82	I/O	D0
8	I	MODE	33	I/O	DMD1	58	I/O	I/O	83	I/O	D1
9	I/O	DBP	34	I/O	DMD2	59	—	GND	84	I/O	D2
10	—	GND	35	I/O	DMD3	60	I/O	REQ	85	I/O	D3
11	I/O	DB7	36	I/O	DMD4	61	I/O	C/D	86	I/O	D4
12	I/O	DB6	37	I/O	DMD5	62	I/O	SEL	87	I/O	D5
13	I/O	DB5	38	I/O	DMD6	63	I/O	MSG	88	I/O	D6
14	—	VDD	39	I/O	DMD7	64	—	VDD	89	I/O	D7
15	—	GND	40	—	GND	65	—	GND	90	—	GND
16	—	GND	41	I/O	DMD8	66	—	GND	91	I/O	D8
17	I/O	DB4	42	I/O	DMD9	67	I/O	RST	92	I/O	D9
18	I/O	DB3	43	I/O	DMD10	68	I/O	ACK	93	I/O	D10
19	I/O	DB2	44	I/O	DMD11	69	I/O	BSY	94	I/O	D11
20	I/O	DB1	45	I/O	DMD12	70	—	GND	95	I/O	D12
21	—	GND	46	I/O	DMD13	71	I/O	ATN	96	I/O	D13
22	I/O	DB0	47	I/O	DMD14	72	I	A0	97	I/O	D14
23	I	TEST1	48	I/O	DMD15	73	I	A1	98	I/O	D15
24	—	—	49	I/O	UDMDP	74	I	A2	99	I/O	UDP
25	—	—	50	I	DMBHE (DMUDS)	75	I	A3	100	I	BHE (UDS)

() ; AT LOW LEVEL

SCSI INTERFACE

INPUT/OUTPUT

$\overline{\text{ACK}}$	: ACKNOWLEDGE
$\overline{\text{ATN}}$	: ATTENTION
$\overline{\text{BSY}}$	: BUSY
$\overline{\text{C/D}}$	: CONTROL/DATA
$\overline{\text{DB0}} - \overline{\text{DB7}}$	: DATA BUS0 - DATA BUS7
$\overline{\text{DBP}}$	: DATA BUS PARITY
$\overline{\text{I/O}}$	: INPUT/OUTPUT
$\overline{\text{MSG}}$	: MESSAGE
$\overline{\text{REQ}}$	: REQUEST
$\overline{\text{RST}}$	: RESET
$\overline{\text{SEL}}$	: SELECT

MPU INTERFACE

INPUT

$\overline{\text{A0}} - \overline{\text{A4}}$	: ADDRESS0 - ADDRESS4
$\overline{\text{BHE}} (\overline{\text{UDS}})$	: BUS HIGH ENABLE (UPPER DATA STOROE)
$\overline{\text{CS0}}$	: CHIP SELECT 0
$\overline{\text{CS1}}$	: CHIP SELECT 1
$\overline{\text{MODE}}$	: MODE
$\overline{\text{RD}} (\text{R/W})$	: READ (READ/WRITE)
$\overline{\text{WR}} (\text{LDS})$	: WRITE (LOWER DATA STOROE)

OUTPUT

$\overline{\text{INT}} (\overline{\text{INT}})$	: INTERRUPT REQUEST
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INPUT/OUTPUT

$\overline{\text{D0}} - \overline{\text{D15}}$	: DATA0 - DATA15
$\overline{\text{LDP}}$	: LOWER DATA PARITY
$\overline{\text{UDP}}$	: UPPER DATA PARITY

DMA INTERFACE

INPUT

$\overline{\text{DACK}}$	: DMA ACKNOWLEDGE
$\overline{\text{DMA0}}$	: DMA ADDRESS 0
$\overline{\text{DMBHE}} (\text{DMUDS})$	: DMA BUS HIGH ENABLE (DMA UPPER DATA STOROE)
$\overline{\text{IORD}} (\text{DMR/W})$	: I/O READ (DMA READ/WRITE)
$\overline{\text{IOWR}} (\text{DMLDS})$	: I/O WRITE (DMA LOWER DATA STOROE)
$\overline{\text{TP}}$	: TRANSFER PERMISSION

OUTPUT

$\overline{\text{DREQ}}$	: DMA REQUEST
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INPUT/OUTPUT

$\overline{\text{DMD0}} - \overline{\text{DMD15}}$	: DMD DATA0 - DMD DATA15
$\overline{\text{LDMDP}}$	: LOWER DMA DATA PARITY
$\overline{\text{UDMDP}}$	: UPPER DMA DATA PARITY

INPUT

$\overline{\text{CLK}}$	: CLOCK
$\overline{\text{RESET}}$	: RESET
$\overline{\text{TEST1, 2}}$	: TEST

() ; WHEN "MODE" (8PIN) IS "L" LEVEL INPUT.

