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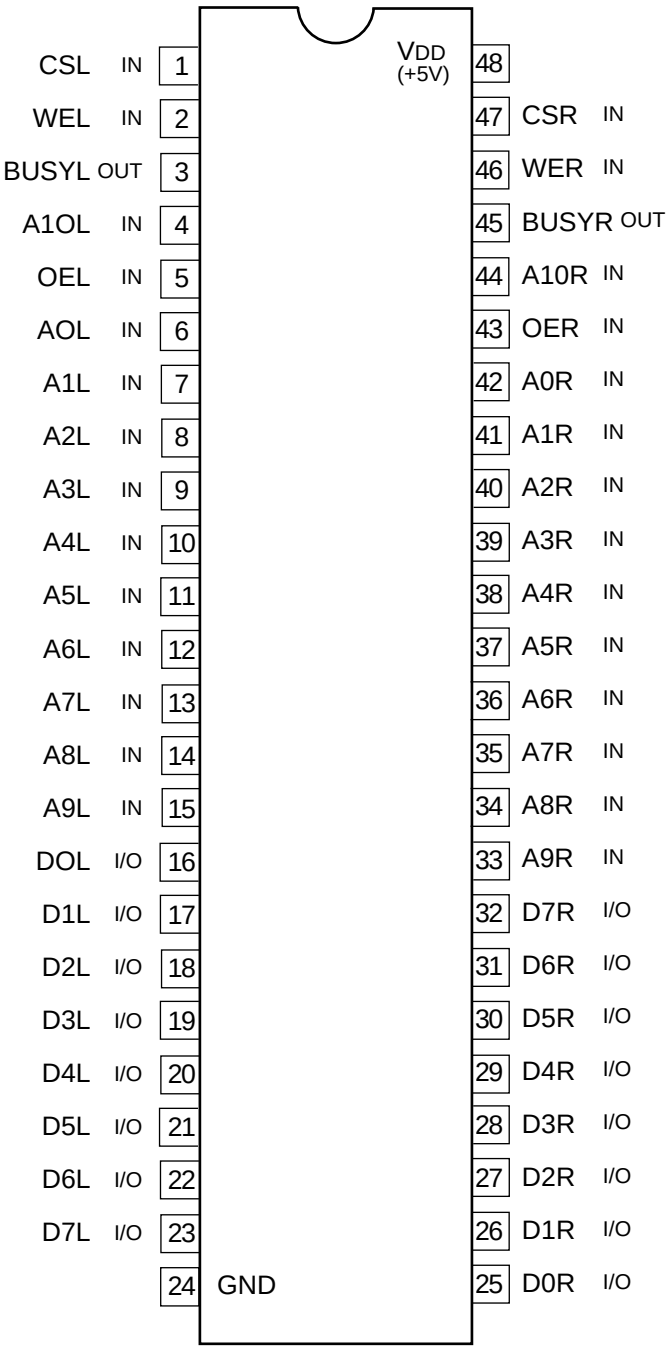
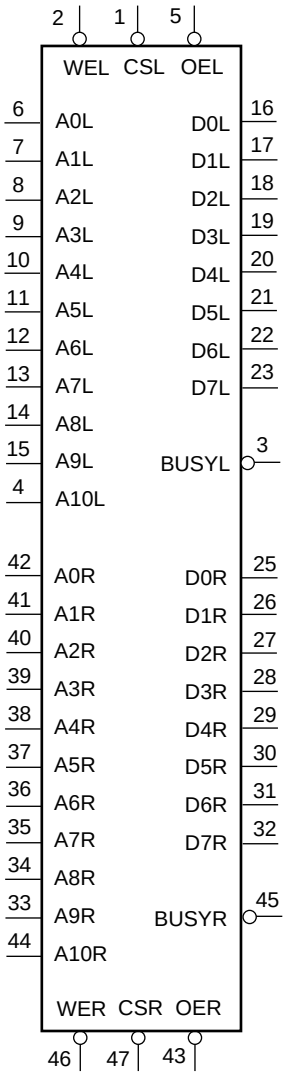
C-MOS 16K (2048×8)-BIT DUAL PORT STATIC RAM

-TOP VIEW-



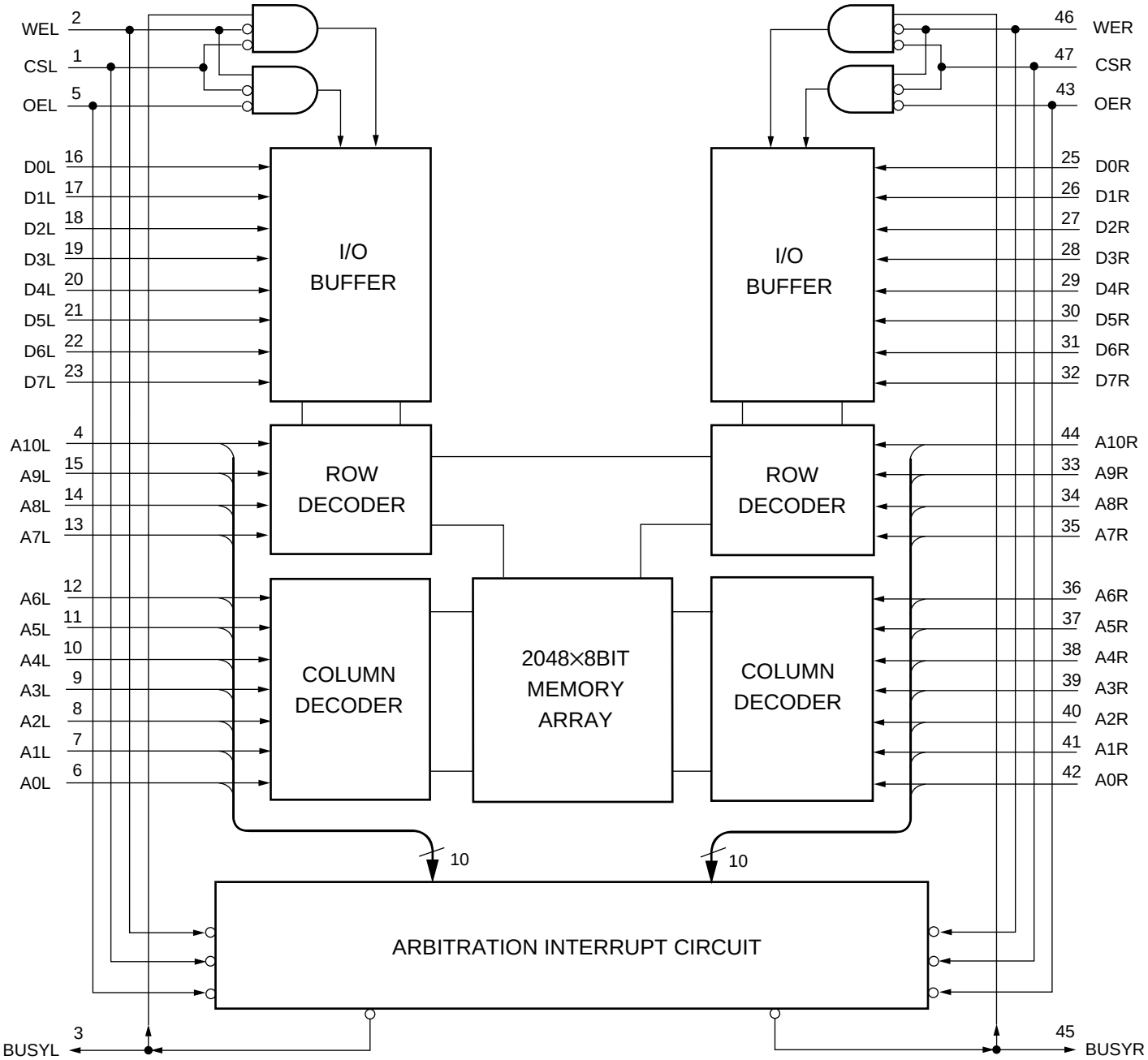


LEFT PORT

AOL–A10L ; ADDRESS INPUTS
BUSYL ; BUSY OUTPUT
CSL ; CHIP SELECT INPUT
DOL–D7L ; DATA INPUTS/OUTPUTS
OEL ; OUTPUT ENABLE INPUT
WEL ; WRITE ENABLE INPUT

RIGHT PORT

AOR–A10R ; ADDRESS INPUTS
BUSYR ; BUSY OUTPUT
CSR ; CHIP SELECT INPUT
DOR–D7R ; DATA INPUTS/OUTPUTS
OER ; OUTPUT ENABLE INPUT
WER ; WRITE ENABLE INPUT


WEL 2
CSL 1
OEL 5
D0L 16
D1L 17
D2L 18
D3L 19
D4L 20
D5L 21
D6L 22
D7L 23
A10L 4
A9L 15
A8L 14
A7L 13
A6L 12
A5L 11
A4L 10
A3L 9
A2L 8
A1L 7
A0L 6
BUSYL 3
I/O BUFFER
ROW DECODER
COLUMN DECODER
2048×8BIT MEMORY ARRAY
I/O BUFFER
ROW DECODER
COLUMN DECODER
10
10
ARBITRATION INTERRUPT CIRCUIT
46 WER
47 CSR
43 OER
25 D0R
26 D1R
27 D2R
28 D3R
29 D4R
30 D5R
31 D6R
32 D7R
44 A10R
33 A9R
34 A8R
35 A7R
36 A6R
37 A5R
38 A4R
39 A3R
40 A2R
41 A1R
42 A0R
45 BUSYR