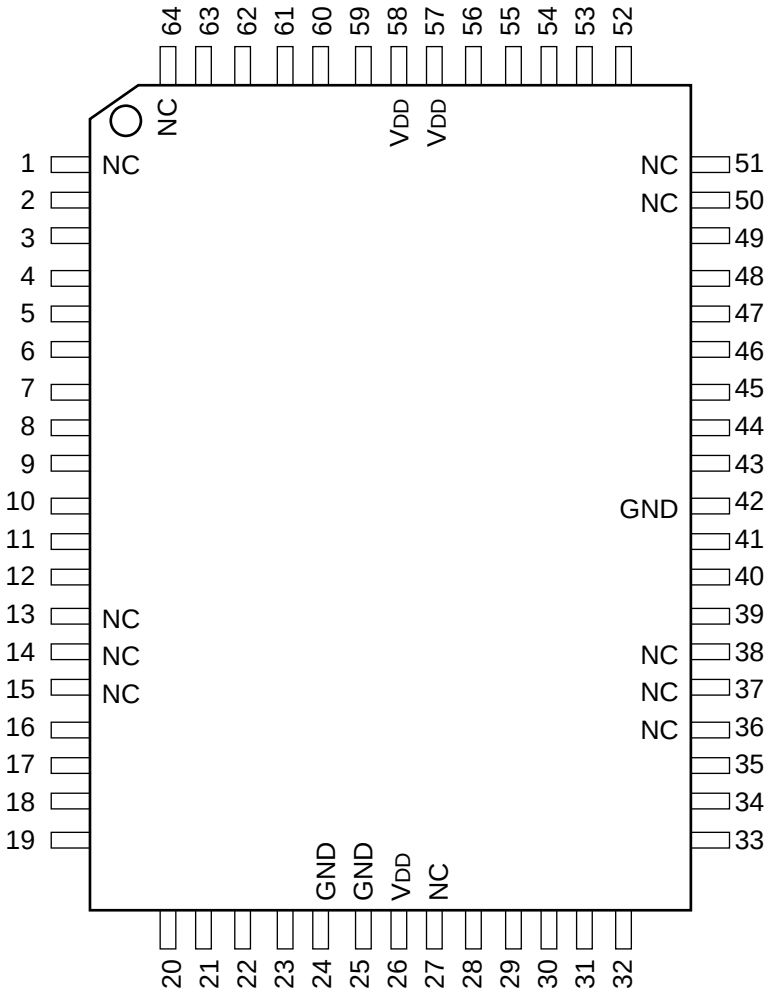
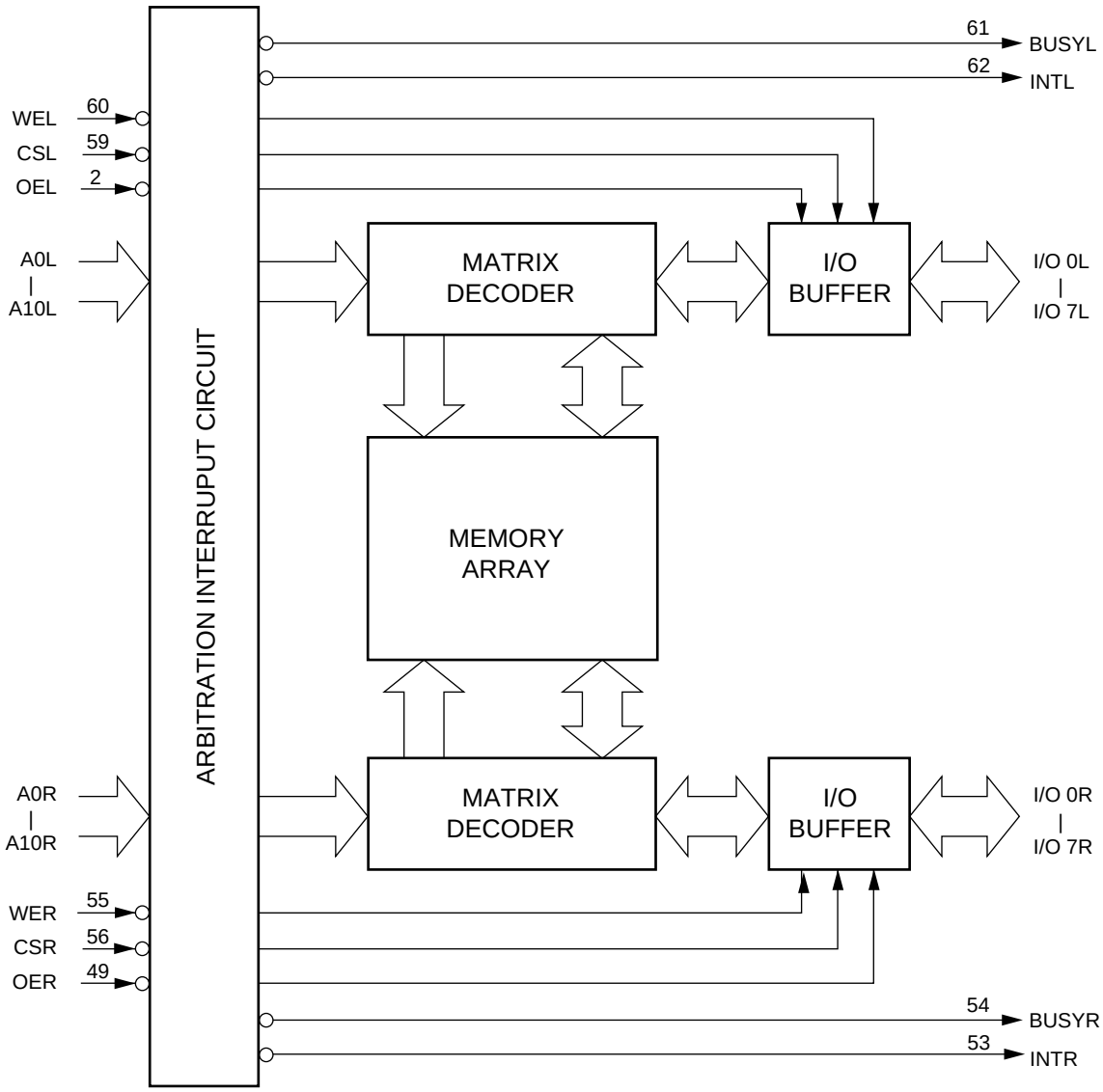
C-MOS 16,384 (2 K × 8)-BIT DUAL PORT SRAM

—TOP VIEW—



A0L - A10L, A0R - A10R	:	ADDRESS INPUTS
I/O0L - I/O7L, I/O0R - I/O7R	:	DATA INPUTS/OUTPUTS
$\overline{CSL}$, $\overline{CSR}$	:	CHIP SELECT INPUT
$\overline{WEL}$, $\overline{WER}$	:	WRITE ENABLE INPUT
$\overline{OEL}$, $\overline{OER}$	:	OUTPUT ENABLE INPUT
$\overline{BUSYL}$, $\overline{BUSYR}$	:	BUSY OUTPUT
$\overline{INTL}$, $\overline{INTR}$	:	INTERRUPT OUTPUT


61
BUSYL
62
INTL
WEL
60
CSL
59
OEL
2
A0L
|
A10L
MATRIX
DECODER
I/O
BUFFER
I/O 0L
|
I/O 7L
ARBITRATION INTERRUPUT CIRCUIT
MEMORY
ARRAY
A0R
|
A10R
MATRIX
DECODER
I/O
BUFFER
I/O 0R
|
I/O 7R
WER
55
CSR
56
OER
49
54
BUSYR
53
INTR