Dual 9-bit D-type flip-flop with reset and enable (3-State)

MB2823

FEATURES

- Two sets of high speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan–in are required with MOS microprocessors
- Live insertation/extraction permitted
- Power-up 3-State
- Power-up Reset
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The MB2823 dual bus interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The MB2823 has two 9-bit wide buffered registers with Clock Enable ($n\overline{CE}$) and Master Reset ($n\overline{MR}$) which are ideal for parity bus interfacing in high microprogrammed systems.

The registers are fully edge-triggered. The state of each D input, one set–up time before the Low-to-High clock transition is transferred to the corresponding flip–flop's Q output.

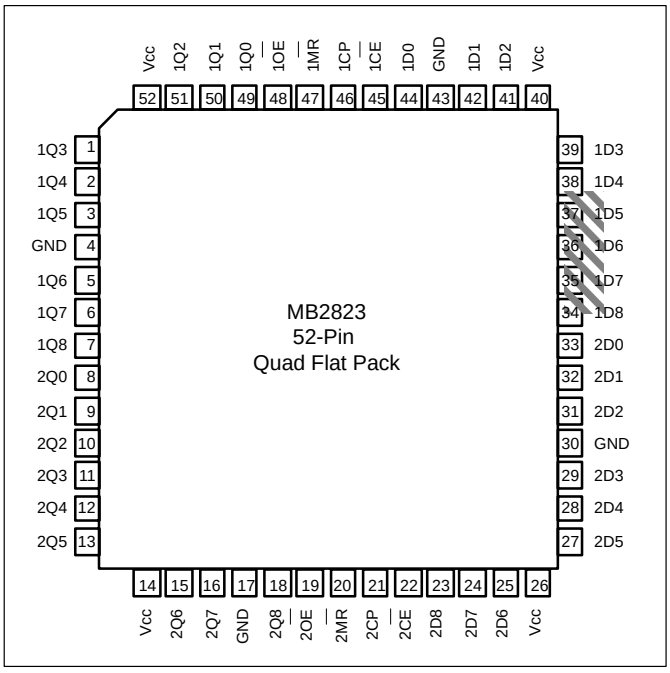
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF; V_{CC} = 5V	4.6	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-state	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	nA

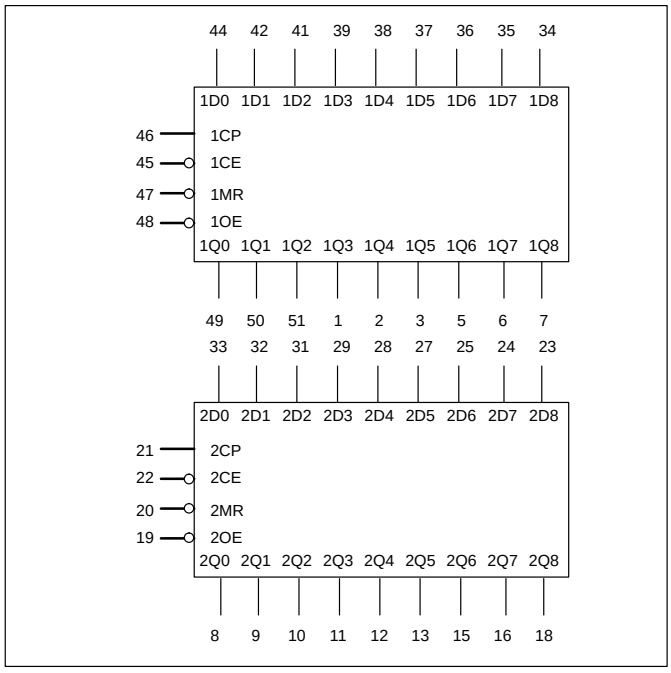
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
52-Pin Plastic Quad Flat Pack	–40°C to +85°C	MB2823BB	1418B

PIN CONFIGURATION



LOGIC SYMBOL



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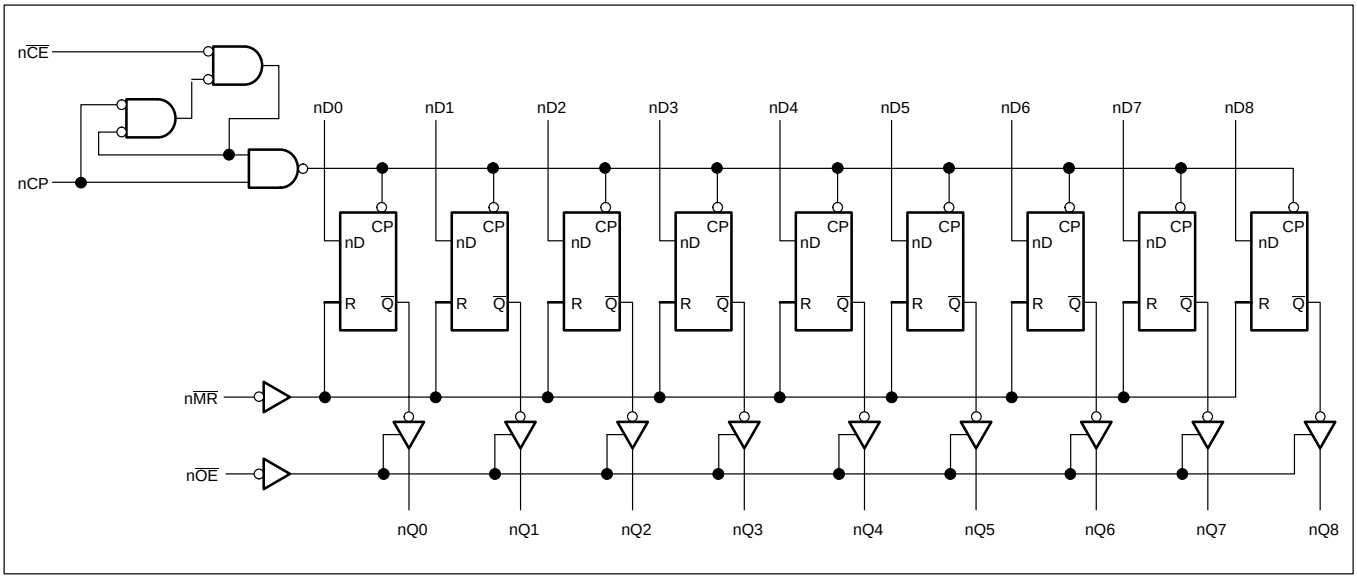
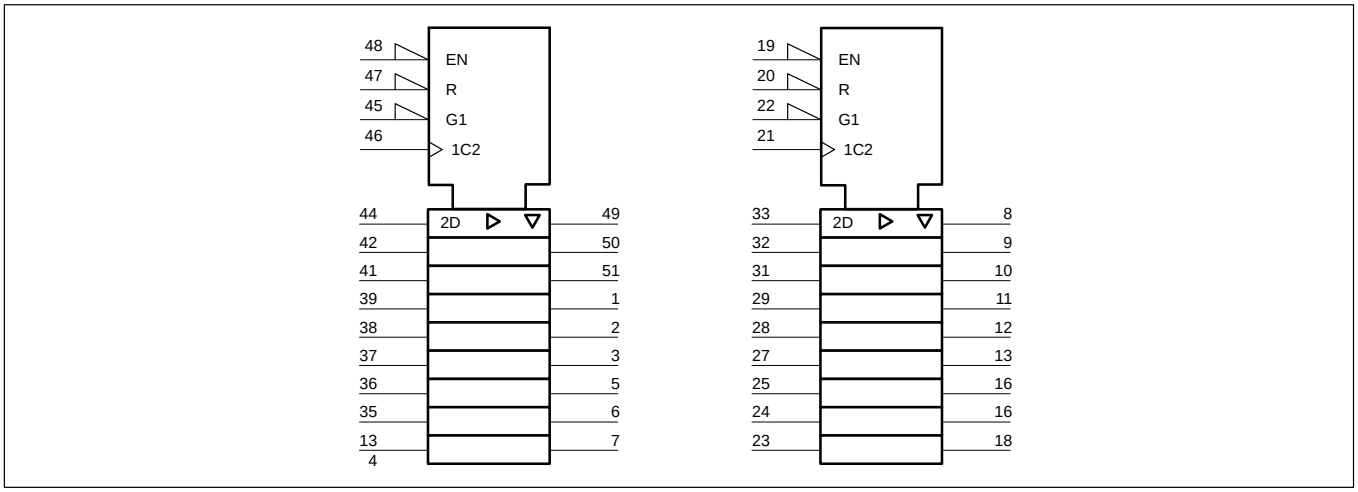
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
48, 19	$1\overline{OE}$, $2\overline{OE}$	Output enable input (active–Low)
44, 42, 41, 39, 38, 37, 36, 35, 34, 33, 32, 31, 29, 28, 27, 25, 24, 23	1D0-1D8 2D0-2D8	Data inputs
49, 50, 51, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16, 18	1Q0-1Q8 2Q0-2Q8	Data outputs
46, 21	1CP, 2CP	Clock pulse input (active rising edge)
45, 22	$1\overline{CE}$, $2\overline{CE}$	Clock enable input (active–Low)
47, 20	$1\overline{MR}$, $2\overline{MR}$	Master reset input (active–Low)
4, 17, 30, 43	GND	Ground (0V)
14, 26, 40, 52	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$n\overline{OE}$	$n\overline{MR}$	$n\overline{CE}$	nCP	nDx	nQ0 – nQ8	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	H	↥	X	NC	Hold
H	X	X	X	X	Z	High impedance

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
↥ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High–level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low–level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_{OL} = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}, V_{OE} = Don't care		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		120	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		45	68		68	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		120	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transistion time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

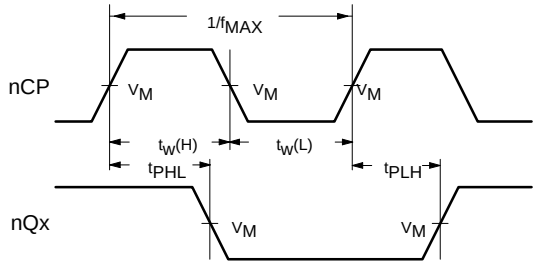
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	140	190		140		MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	2.0 2.5	3.8 4.2	5.1 5.6	2.0 2.5	5.7 6.1	ns
t_{PHL}	Propagation delay $n\overline{MR}$ to nQx	2	3.2	5.3	6.6	3.2	7.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.3 2.2	3.2 4.0	4.4 5.3	1.3 2.2	5.1 5.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	1.3 1.5	3.3 3.1	4.6 4.4	1.3 1.5	5.1 5.9	ns

AC SETUP REQUIREMENTS

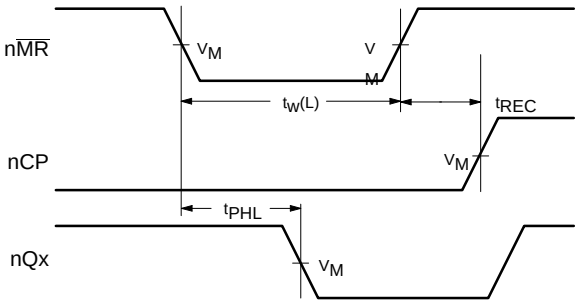
GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time, High or Low nDx to nCP	3	2.0 1.5	0.6 0.2	2.0 1.5	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low nDx to nCP	3	1.5 1.5	–0.2 –0.5	1.5 1.5	
$t_w(H)$ $t_w(L)$	nCP pulse width High or Low	1	3.0 3.5	1.0 2.3	3.0 3.5	ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low n$\overline{CE}$ to nCP	3	1.5 2.0	–0.2 1.0	1.5 2.0	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low n$\overline{CE}$ to nCP	3	1.5 1.5	–1.2 0.3	1.5 1.5	ns
$t_w(L)$	n$\overline{MR}$ pulse width, Low	2	3.0	1.6	3.0	ns
t_{rec}	Recovery time n$\overline{MR}$ to nCP	2	2.5	0.6	2.5	ns

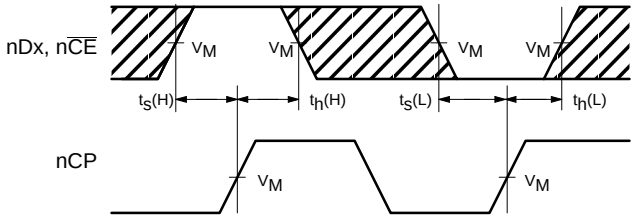
AC WAVEFORMS



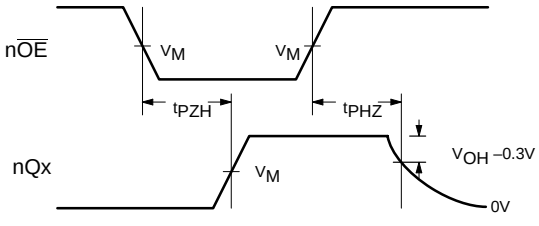
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



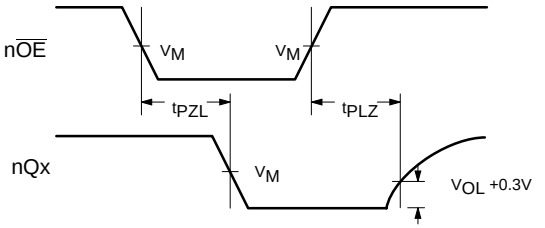
Waveform 2. Master Reset Pulse WIdth, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. Data Setup and Hold Times



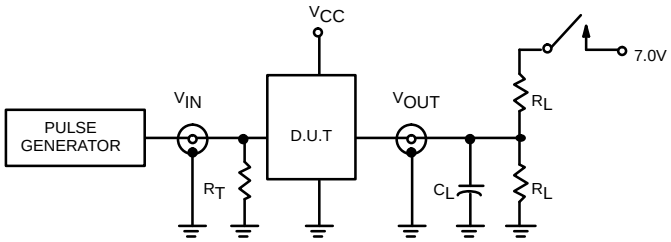
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



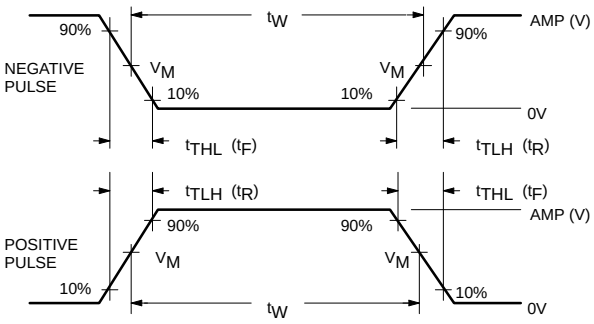
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

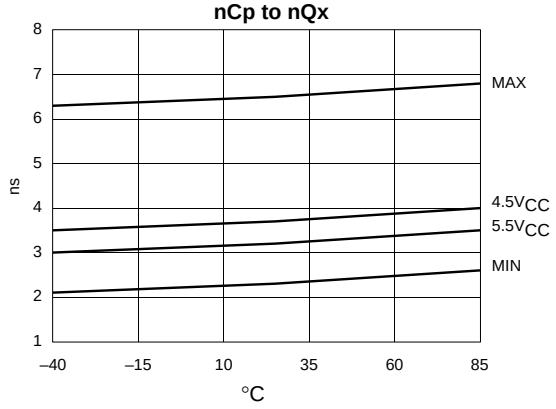
R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

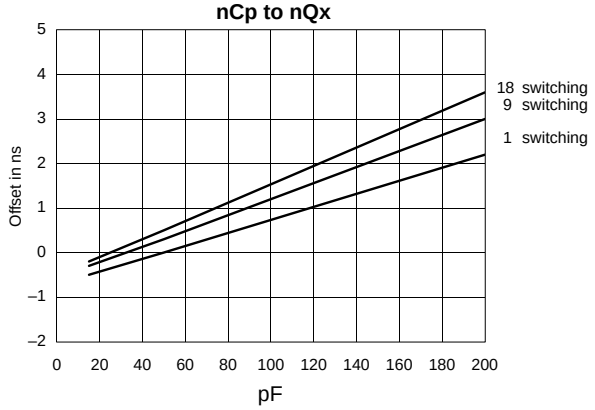
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

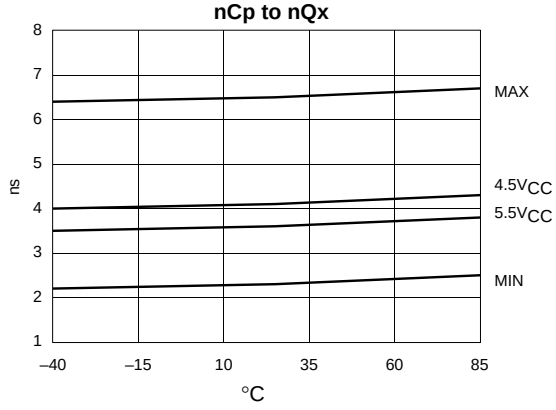
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nCp to nQx



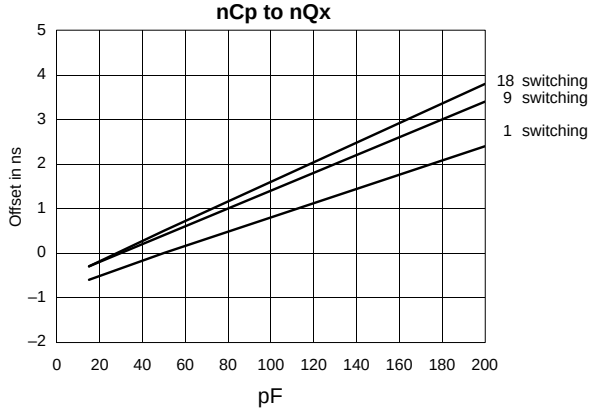
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nCp to nQx



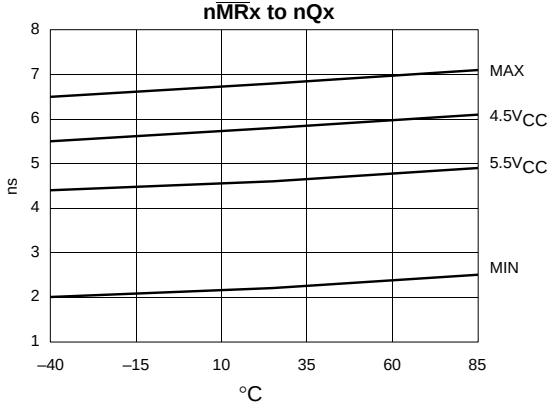
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nCp to nQx



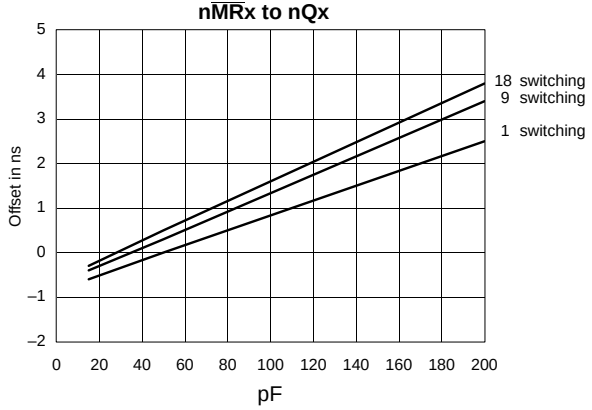
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nCp to nQx



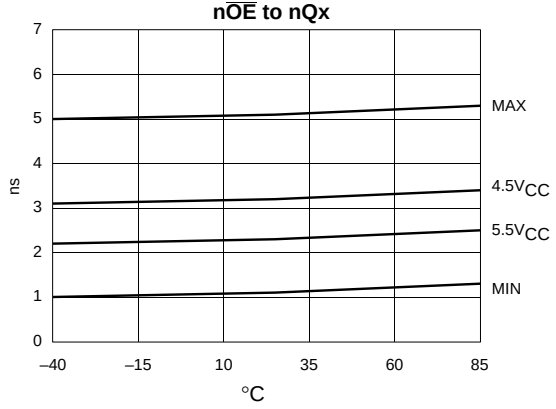
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{MR}$x to nQx



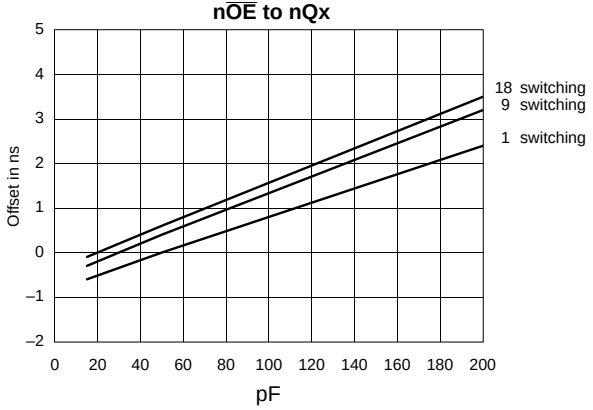
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
n$\overline{MR}$x to nQx



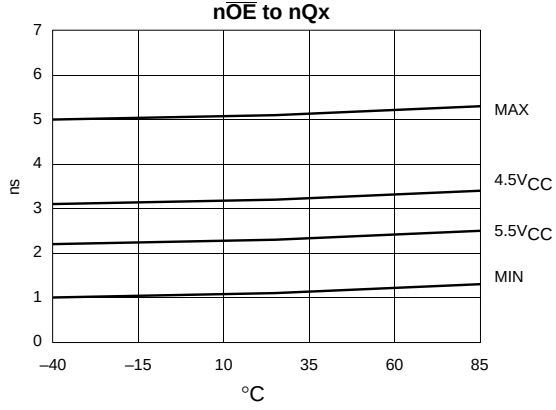
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to nQx



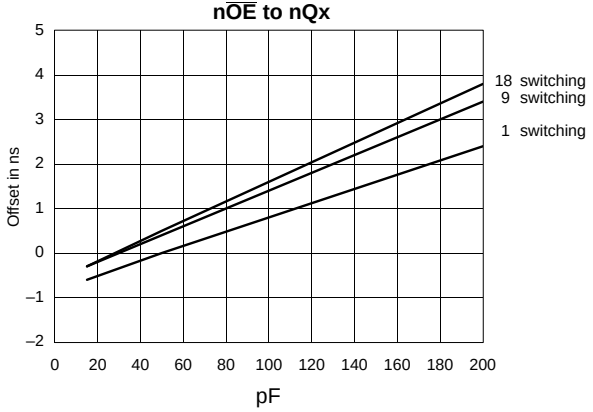
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to nQx



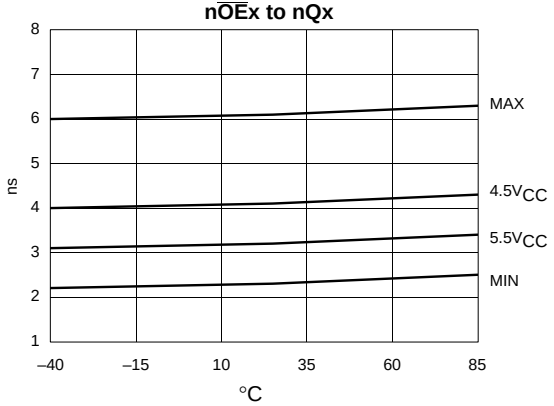
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to nQx



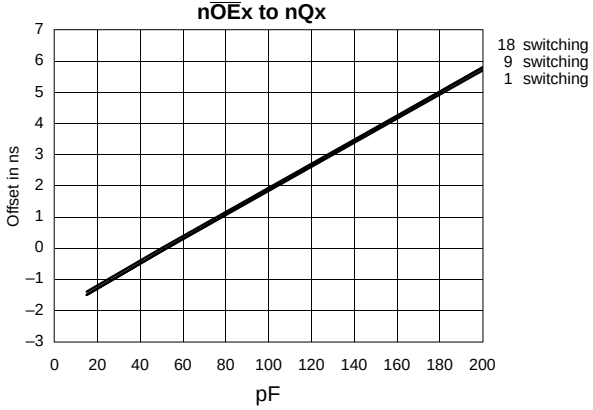
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to nQx



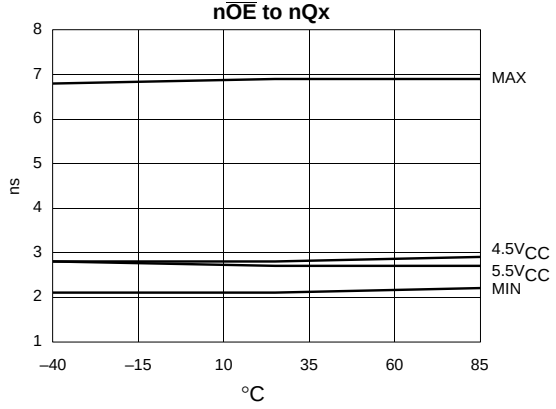
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$x to nQx



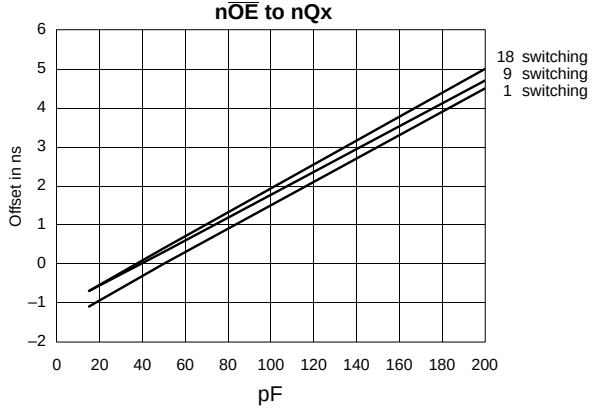
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$x to nQx



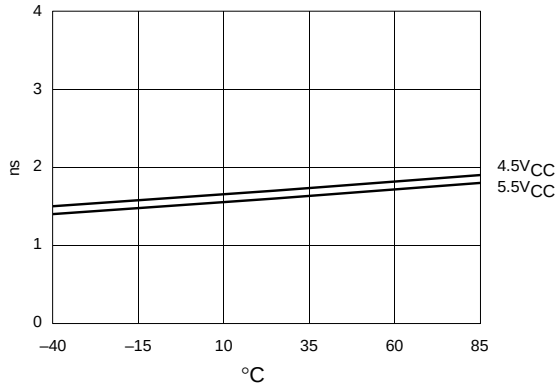
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to nQx



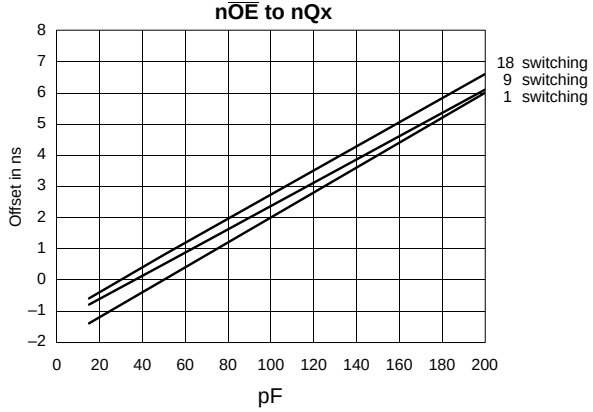
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to nQx



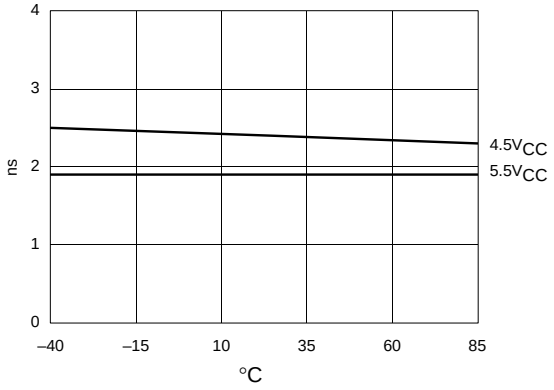
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



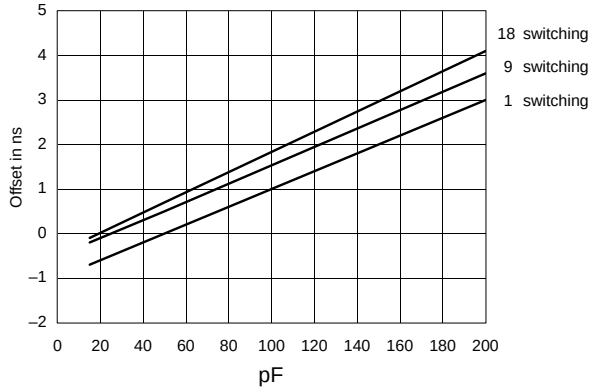
Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to nQx



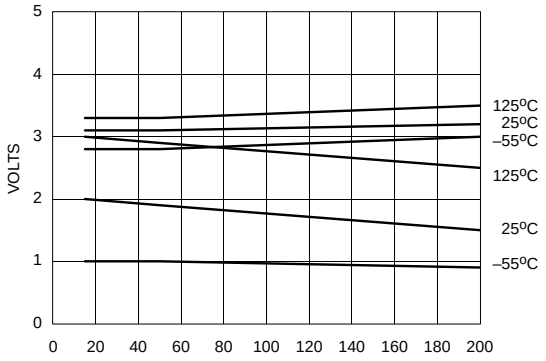
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching



V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0V to 3V



V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0V to 3V