Dual octal transparent latch (3-State) MB2373

FEATURES

- 16-bit transparent latch
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-State
- Live insertion/extraction permitted
- Power-up reset
- 3-State output buffers
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The MB2373 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2373 device is a dual octal transparent latch coupled to two sets of eight 3-State output buffers. The two sections of the device are controlled independently by Enable (nE) and Output Enable ($n\overline{OE}$) control gates.

The data on each set of D inputs are transferred to the latch outputs when the Latch Enable (nE) input is High. The latch remains transparent to the data inputs while nE is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. Each active-Low Output Enable ($n\overline{OE}$) controls eight 3-State buffers independent of the latch operation.

When $n\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $n\overline{OE}$ is High, the outputs are in the High–impedance "OFF" state, which means they will neither drive nor load the bus.

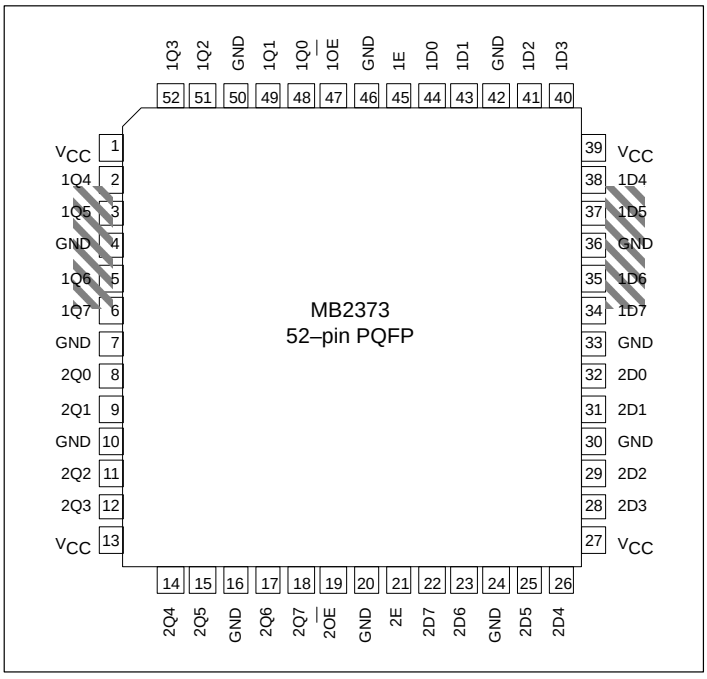
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	nA

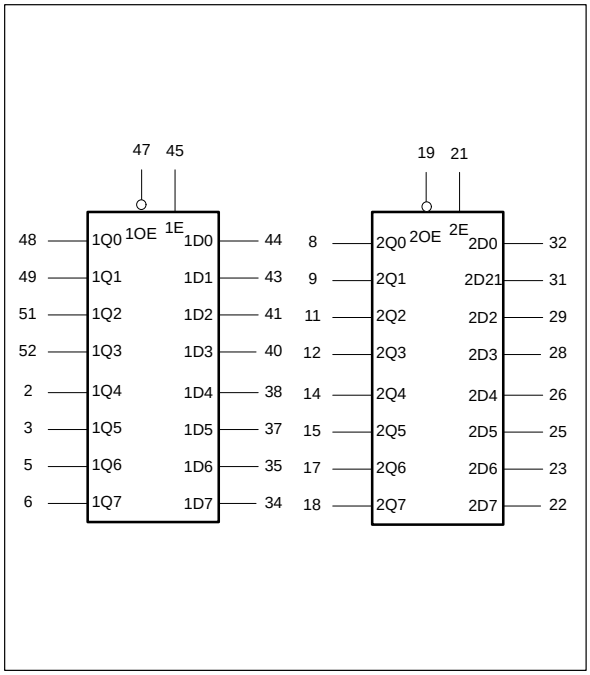
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
52–pin plastic Quad Flat Pack	–40°C to +85°C	MB2373BB	1418B

PIN CONFIGURATION



LOGIC SYMBOL



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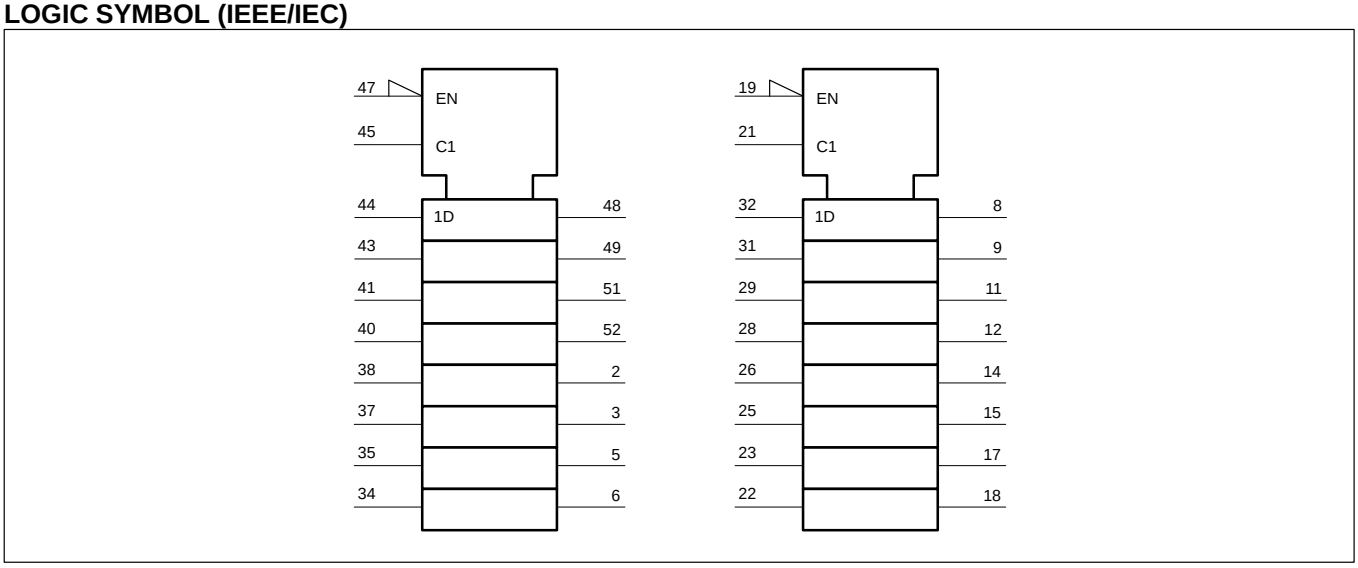
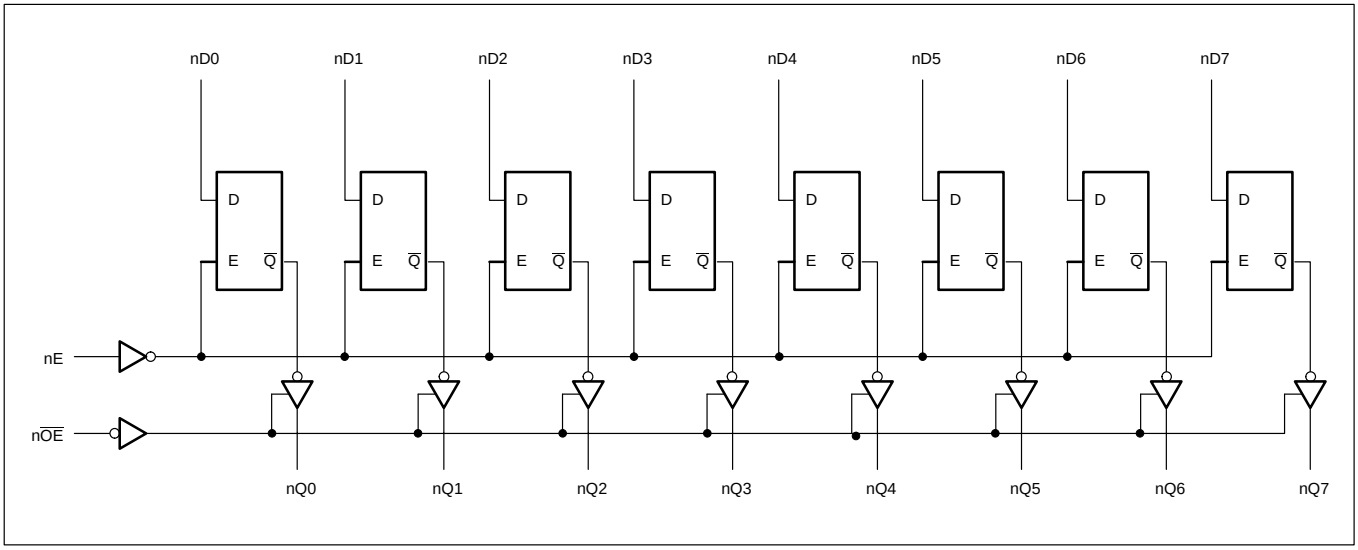
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
44, 43, 41, 40,38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	1D0 – 1D7 2D0 – 2D7	Data inputs
48, 49, 51, 52, 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
47, 19	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active–Low)
45, 21	1E, 2E	Enable inputs (active–High)
4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	GND	Ground (0V)
1, 13, 27, 39	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nE	nDx	REGISTER	nQ0 – nQ7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	i h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = GND		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–70	–180	–50	–180	mA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		120	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		44	60		60	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		120	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

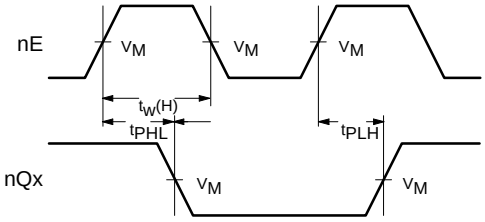
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	1.3 1.3	2.8 2.9	4.1 4.1	1.3 1.3	4.8 4.8	ns
t_{PLH} t_{PHL}	Propagation delay nE to nQx	1	1.8 2.0	3.5 3.5	4.9 4.9	1.8 2.0	5.7 5.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.2 2.1	2.9 3.8	4.1 5.3	1.2 2.1	5.1 6.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	1.4 2.0	3.7 3.6	5.0 4.6	1.4 2.0	5.5 5.1	ns

AC SETUP REQUIREMENTS

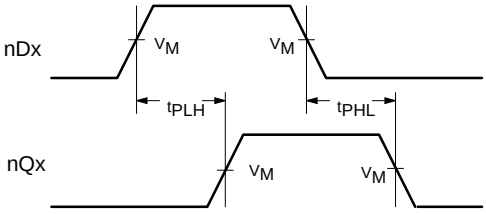
GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time, High or Low nDx to nE	3	1.0 1.0	0.0 0.3	1.0 1.0	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low nDx to nE	3	0.5 0.5	–0.2 0.0	0.5 0.5	ns
$t_w(H)$	Enable pulse width High	1	2.5	1.0	2.5	ns

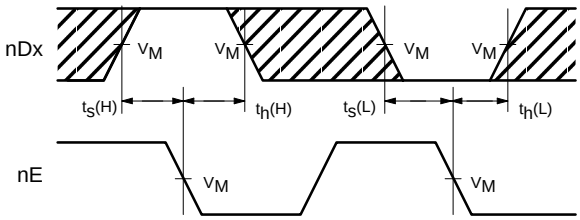
AC WAVEFORMS



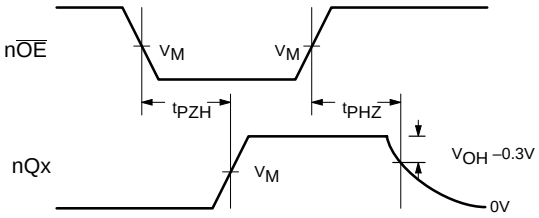
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



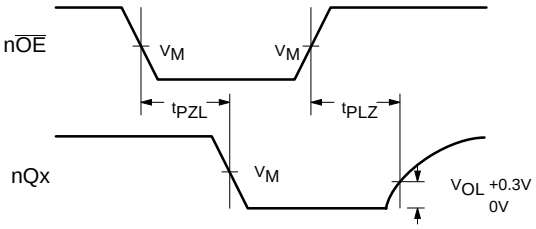
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Setup and Hold Times



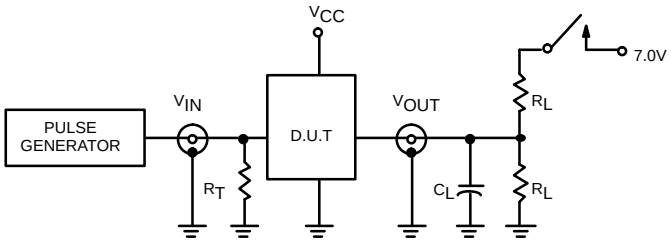
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



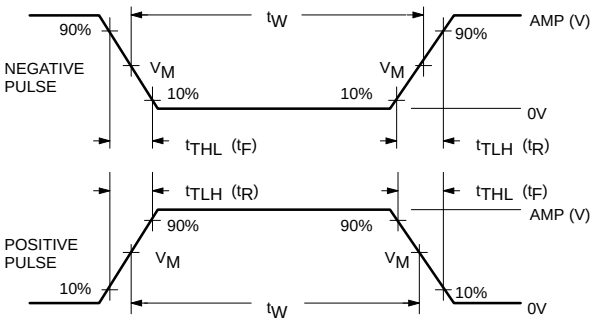
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

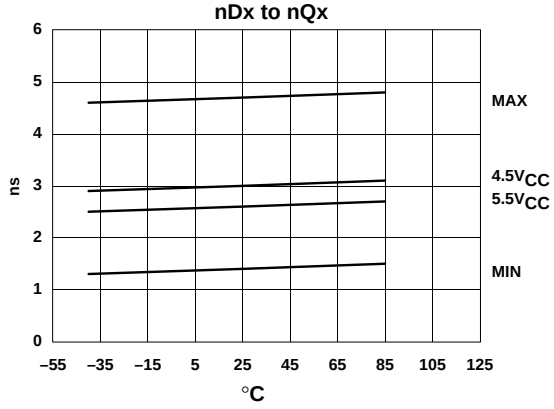
R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

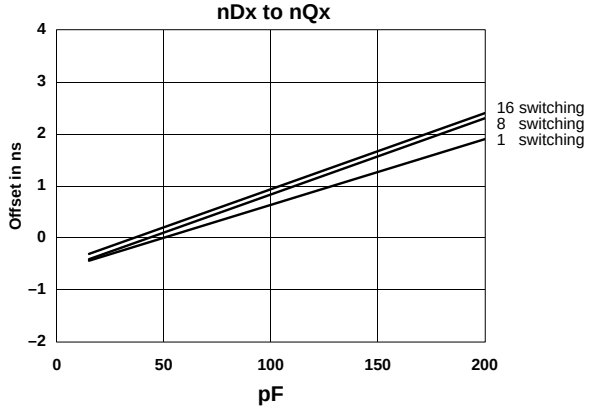
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

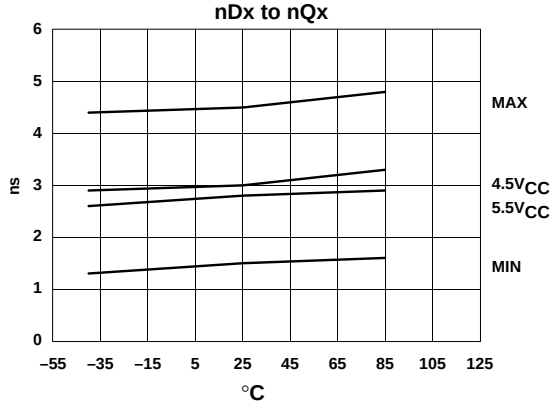
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nDx to nQx



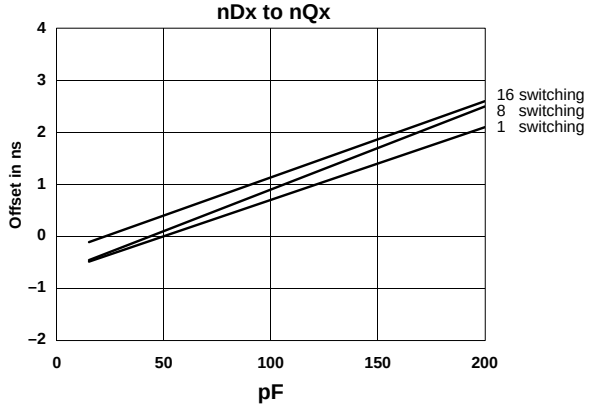
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nDx to nQx



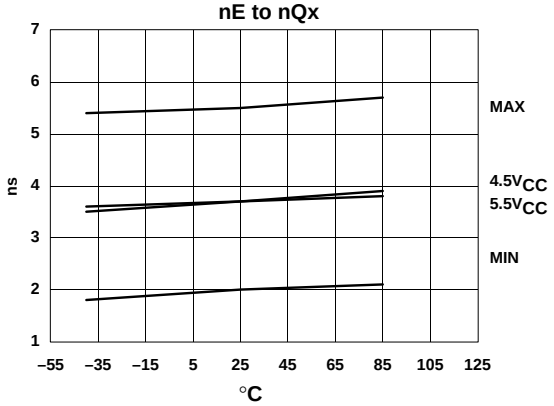
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nDx to nQx



Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nDx to nQx



t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nE to nQx



Adjustment of t_{PLH} for
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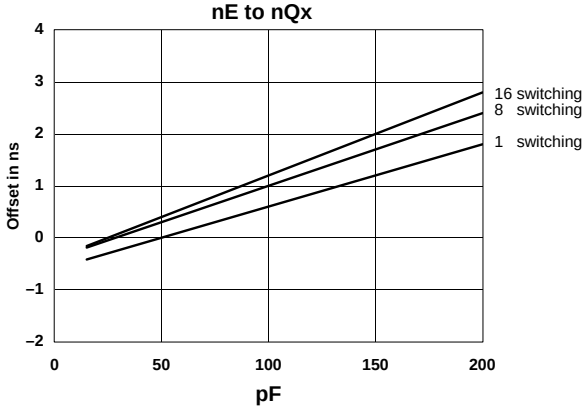
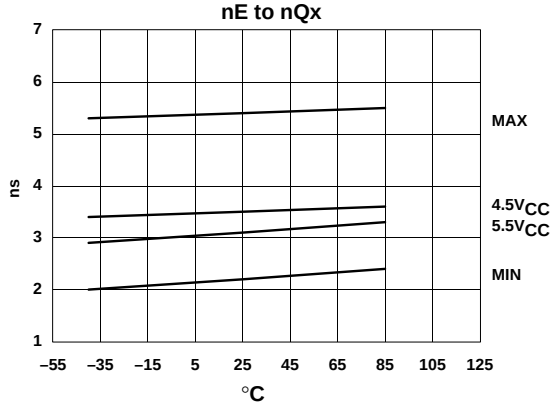
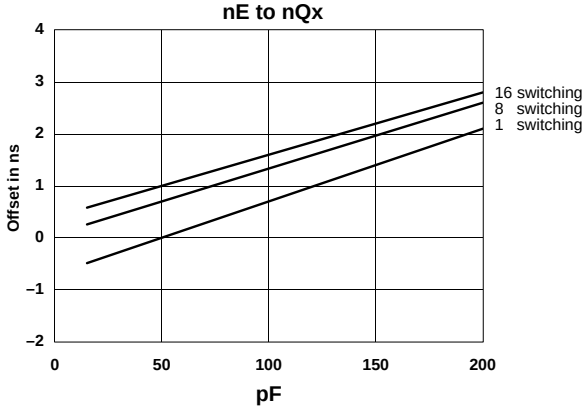
nE to nQx



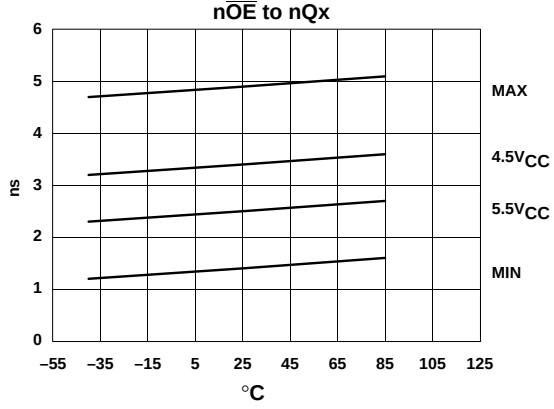
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nE to nQx



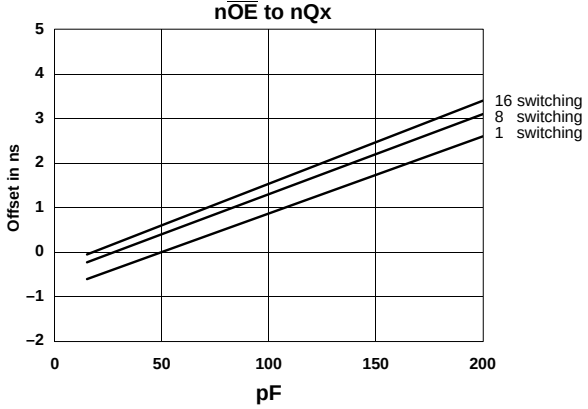
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nE to nQx



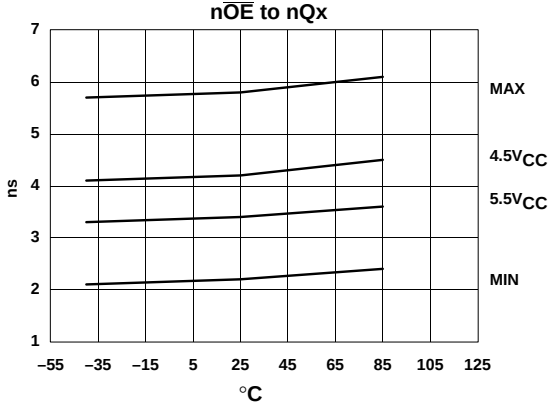
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to nQx



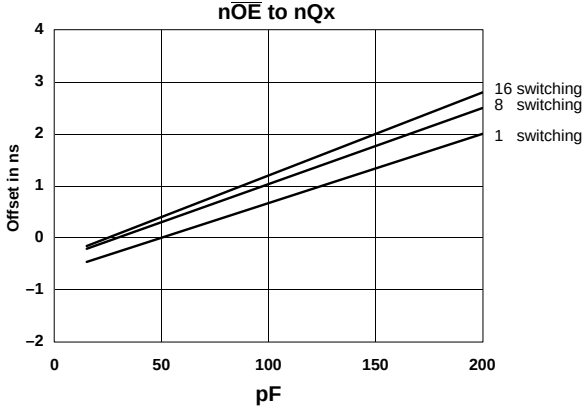
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to nQx



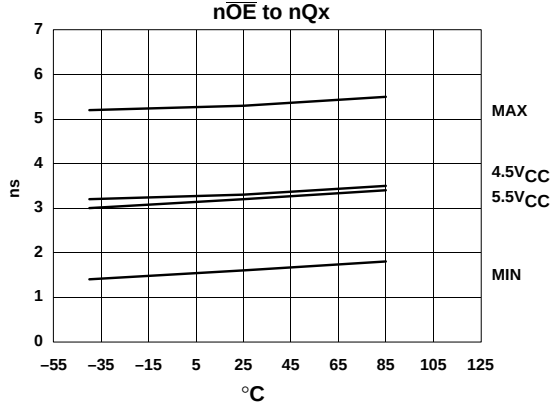
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to nQx



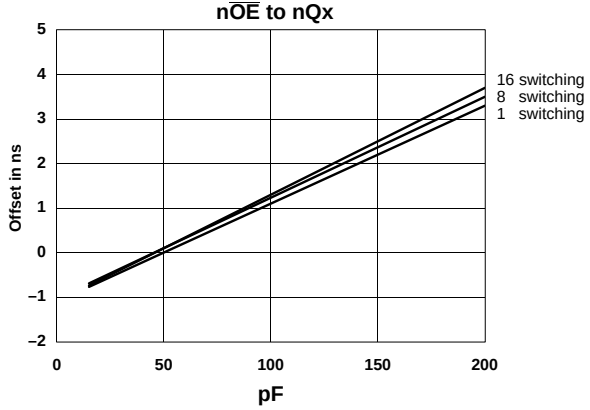
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to nQx



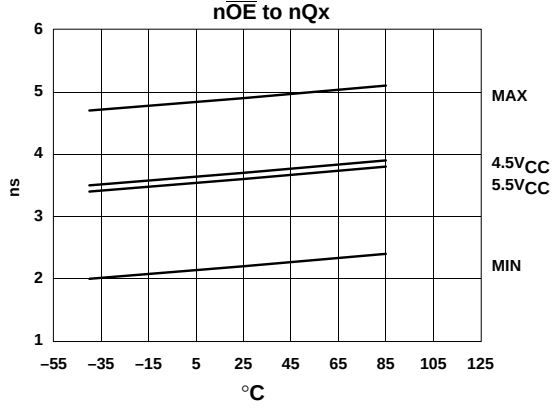
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to nQx



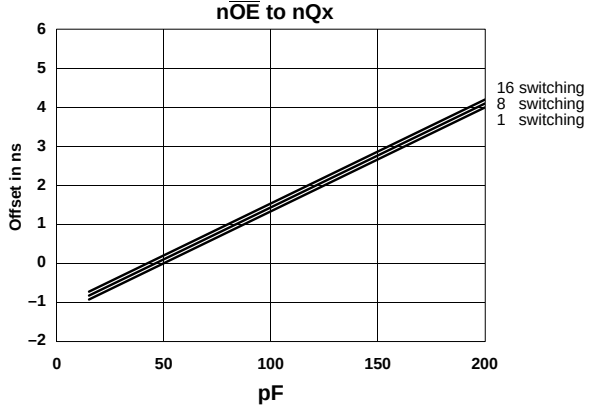
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to nQx



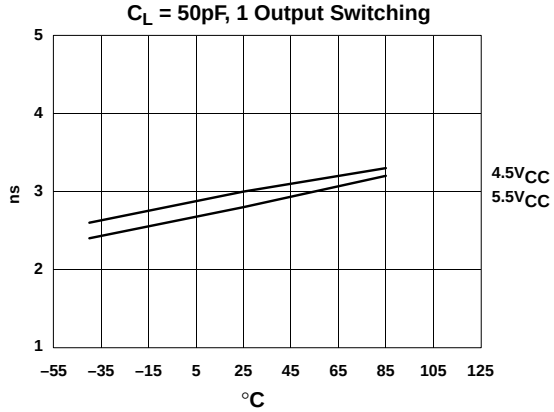
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to nQx



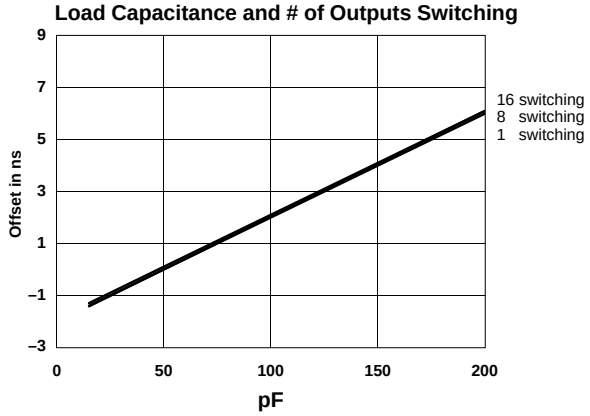
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to nQx



t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching

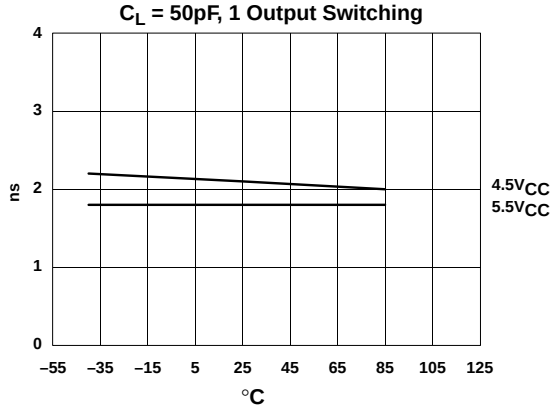


Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching

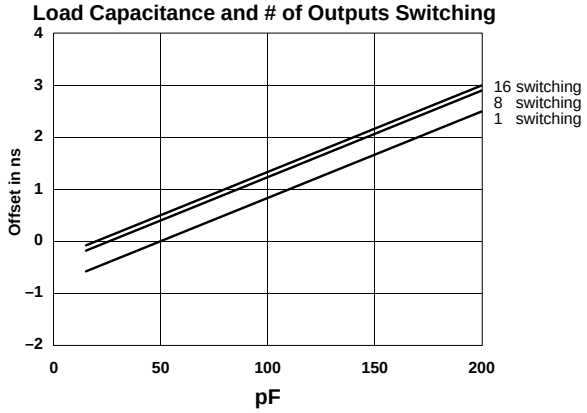


Dual octal transparent latch (3-State) MB2373

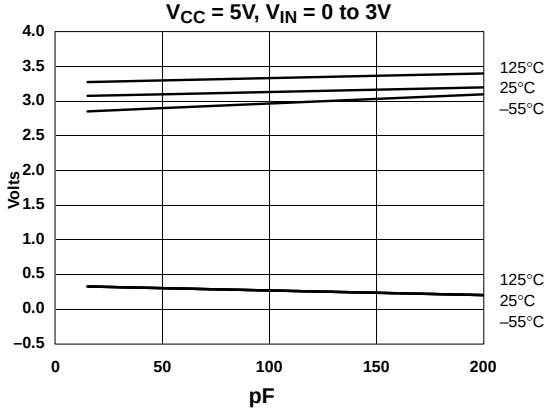
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching



V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V