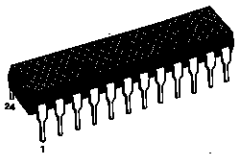
SGS-THOMSON MICROELECTRONICS

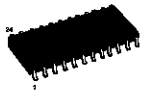
M74HC181

ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

- HIGH SPEED
  t_{PD} = 13 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS181



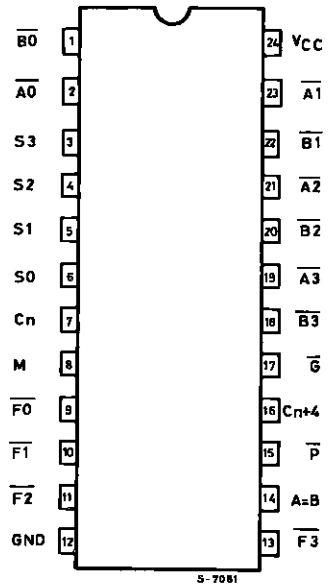
B1R
(Plastic Package)



M1R
(Micro Package)

ORDER CODES :
M74HC181M1R M74HC181B1R

PIN CONNECTIONS (top view)



* Open drain Output Structure

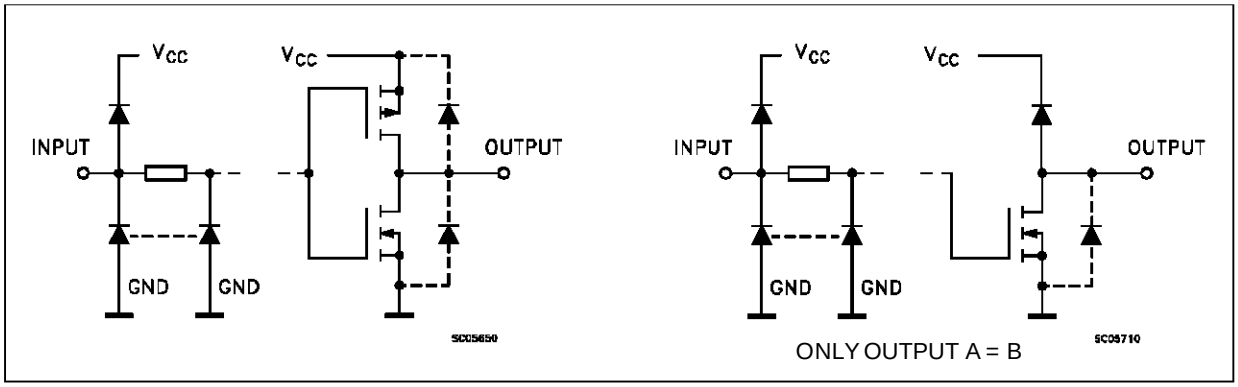
DESCRIPTION

The 74HC181 is a high speed CMOS ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR fabricated with silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the M54HC182 or M74HC182, full carry look-ahead circuits, high-speed arithmetic operations can be performed. These circuits will accomodate active-high or active-low data, if the pin designations are interpreted as shown below. Subtraction is accomplished by 1,s complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is 1–B–1, which requires an end-around or forced carry to produce A–B. The 181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs ($\overline{F0}$, $\overline{F1}$, $\overline{F2}$, $\overline{F3}$) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicated equality (A = B). The ALU should be

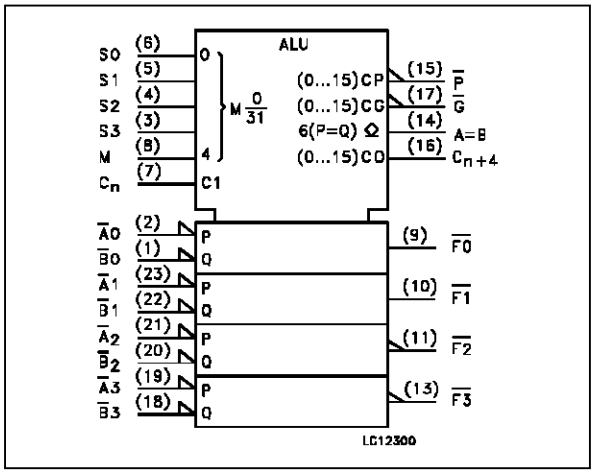
DESCRIPTION (continued)

in the subtract mode with C_n = H when performing this comparison. The A = B output is open-drain so that it can be wire-AND connected to give a comparison for more that four bits. The carry output (Cn + 4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively. These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUITS



IEC LOGIC SYMBOLS



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
2, 23, 21, 19	$\overline{A0}$ to $\overline{A3}$	Word A Inputs
1, 22, 20, 18	$\overline{B0}$ to $\overline{B3}$	Word B Inputs
6, 5, 4, 3	S0 to S3	Function Select Inputs
7	Cn	Inv. Carry Input
8	M	Mode Control Input
9, 10, 11, 13	$\overline{F0}$ to $\overline{F3}$	Function Outputs
14	A = B	Comparator Output
15	$\overline{P}$	Carry Propagate Output
16	Cn + 4	Inv. Carry Output
17	$\overline{G}$	Carry Generate Output
12	GND	Ground (0V)
24	V_{CC}	Positive Supply Voltage

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
ACTIVE LOW DATA (Table 1)	$\overline{A0}$	$\overline{B0}$	$\overline{A1}$	$\overline{B1}$	$\overline{A2}$	$\overline{B2}$	$\overline{A3}$	$\overline{B3}$	$\overline{F0}$	$\overline{F1}$	$\overline{F2}$	$\overline{F3}$	Cn	Cn + 4	$\overline{P}$	$\overline{G}$
ACTIVE HIGH DATA (Table 1)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	Cn	Cn + 4	X	Y

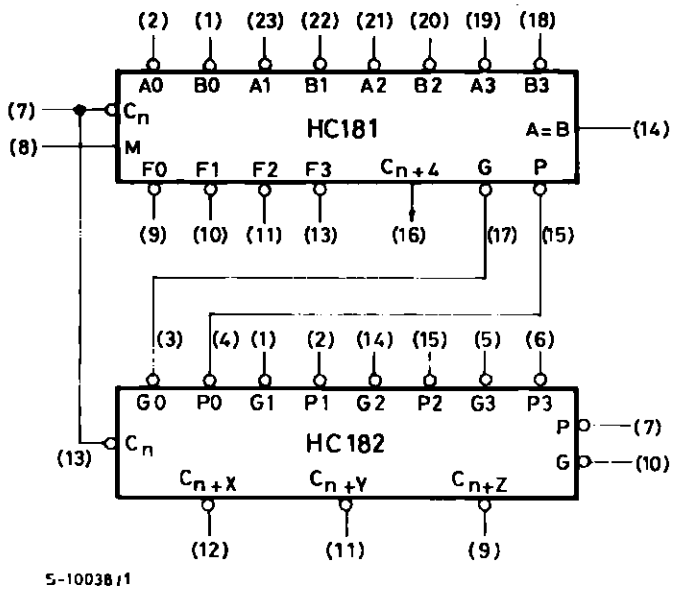
Input Cn	Output Cn + 4	Active LOW Data (Figure 1)	Active HIGH Data (Figure 2)
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

TRUTH TABLE 1

Selection				ACTIVE LOW DATA		
				M = H Logic Functions	M = L: Arithmetic Operations	
S3	S2	S1	S0		Cn = L (no carry)	Cn = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A Minus 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = (A$\overline{B}$)
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	F = $\overline{B}$	F = AB Plus (A + B)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
H	L	L	L	F = $\overline{A}$B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	F = A $\oplus$ B	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A *	F = A Plus A Plus 1
H	H	L	H	F = A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

* Each bit is shifted to the next more significant position.

FIGURE 1

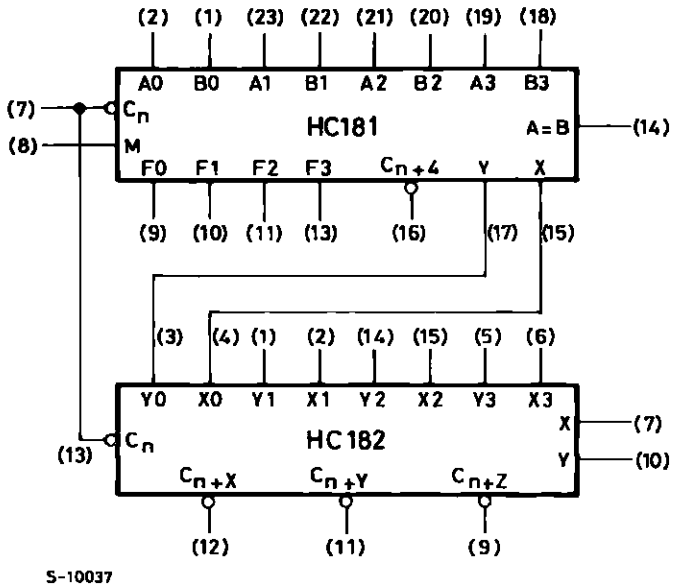


TRUTH TABLE 2

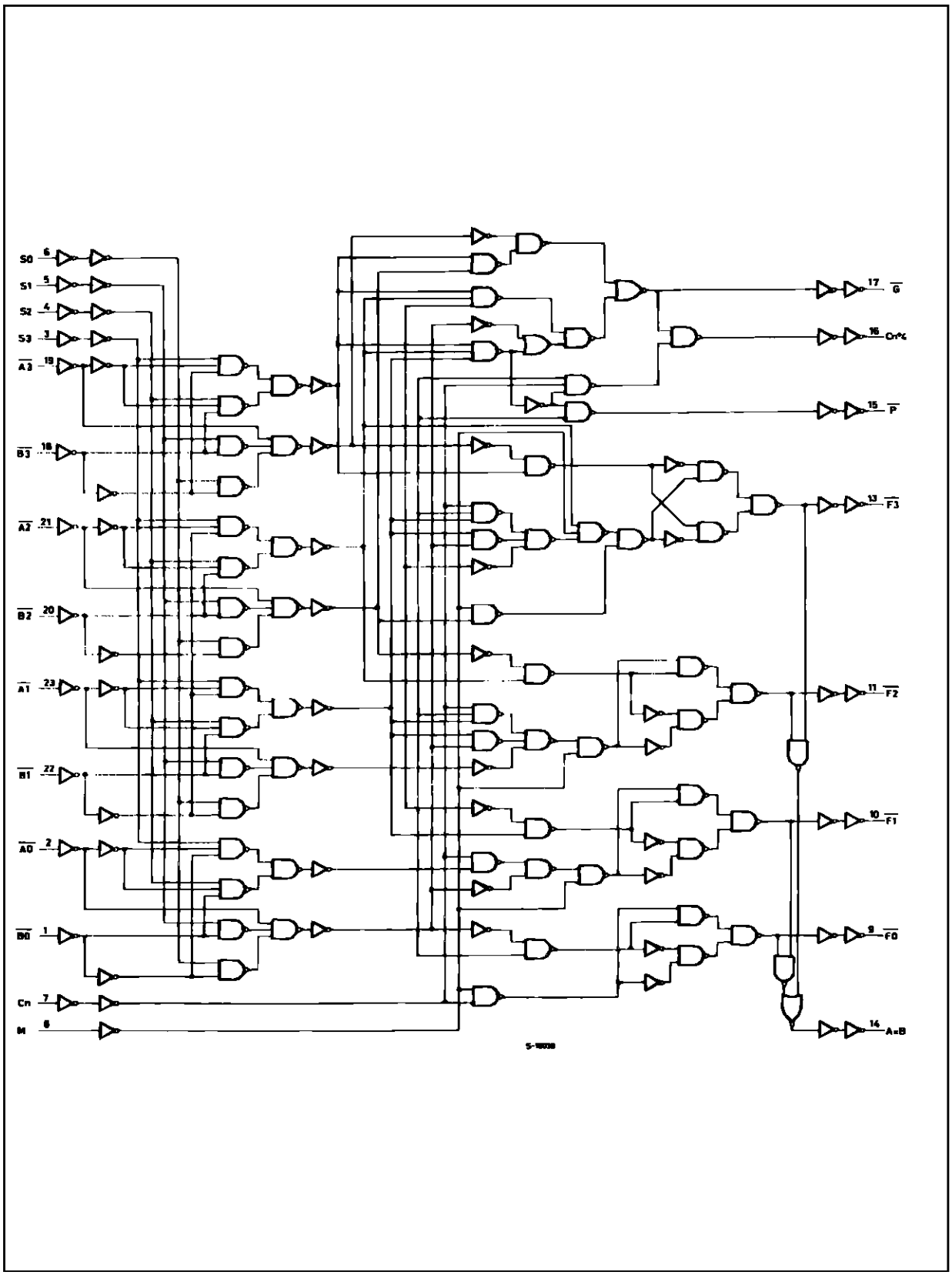
Selection				ACTIVE HIGH DATA		
				M = H Logic Functions	M = L: Arithmetic Operations	
S3	S2	S1	S0		Cn = H (no carry)	Cn = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A Plus 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + $\overline{B}$) Plus 1
L	L	H	L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L	L	H	H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{AB}$	F = A Plus (A$\overline{B}$)	F = A Plus A$\overline{B}$ Plus 1
L	H	L	H	F = $\overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus (A$\overline{B}$) Plus 1
L	H	H	L	F = A ⊕ B	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A *	F = A Plus A Plus 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

* Each bit is shifted to the next more significant position.

FIGURE 2



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)			T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		V
		4.5			3.15			3.15		
		6.0			4.2			4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5	V
		4.5					1.35		1.35	
		6.0					1.8		1.8	
V_{OH}	High Level Output Voltage (except A = B output)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		V
		4.5			4.4	4.5		4.4		
		6.0			5.9	6.0		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1	V
		4.5				0.0	0.1		0.1	
		6.0				0.0	0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

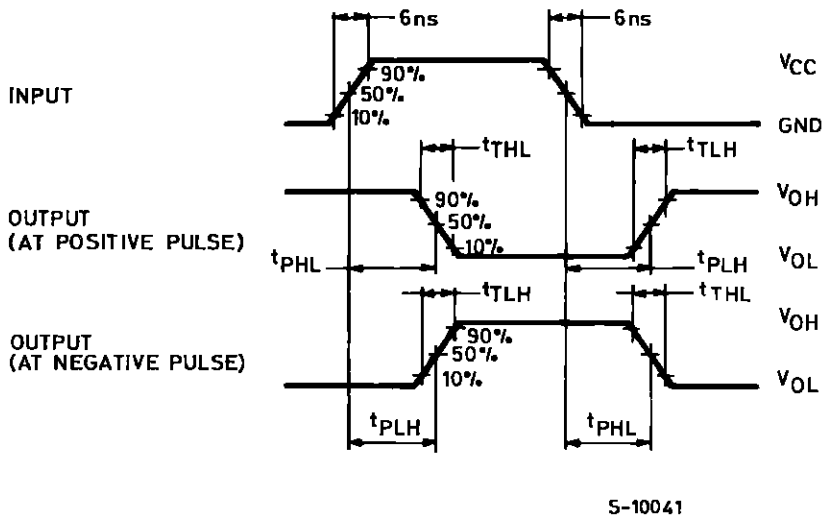
Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		
				Min.	Typ.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
t_{PLH} t_{PHL}	Propagation Delay Time (1)	2.0			54	120		150	ns
		4.5			16	24		30	
		6.0			13	20		26	
t_{PLH} t_{PHL}	Propagation Delay Time (2)	2.0			90	215		270	ns
		4.5			26	43		54	
		6.0			20	37		46	
t_{PLH} t_{PHL}	Propagation Delay Time (3)	2.0			97	215		270	ns
		4.5			27	43		54	
		6.0			21	37		46	
t_{PLH} t_{PHL}	Propagation Delay Time (4)	2.0			80	180		225	ns
		4.5			23	36		45	
		6.0			18	31		38	
t_{PLH} t_{PHL}	Propagation Delay Time (5)	2.0			81	190		240	ns
		4.5			24	38		48	
		6.0			19	32		41	
t_{PLH} t_{PHL}	Propagation Delay Time (6)	2.0			80	180		225	ns
		4.5			23	36		45	
		6.0			18	31		38	
t_{PLH} t_{PHL}	Propagation Delay Time (7)	2.0			80	170		215	ns
		4.5			23	34		43	
		6.0			18	29		37	
t_{PLH} t_{PHL}	Propagation Delay Time (8)	2.0			80	170		215	ns
		4.5			23	34		43	
		6.0			18	29		37	
t_{PLH} t_{PHL}	Propagation Delay Time (9)	2.0			95	220		275	ns
		4.5			27	44		55	
		6.0			21	37		47	
t_{PLH} t_{PHL}	Propagation Delay Time (10)	2.0			95	220		275	ns
		4.5			27	44		55	
		6.0			21	37		47	
t_{PLH} t_{PHL}	Propagation Delay Time (11)	2.0			86	200		250	ns
		4.5			24	40		50	
		6.0			18	34		43	
t_{PLZ} t_{PZL}	Propagation Delay Time (12)	2.0	R_L = 1kΩ		92	210		265	ns
		4.5			27	42		53	
		6.0			27	36		45	
C_{IN}	Input Capacitance				5	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				195				pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$

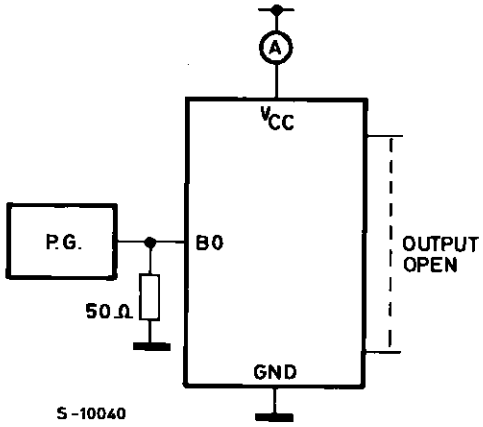
PROPAGATION DELAY TIME TEST CONDITIONS

Test No	INPUT	OUTPUT	Test Conditions
(1)	Cn	Cn + 4	
(2)	Any $\overline{A}$ or $\overline{B}$	Cn + 4	M = GND, S0 = S3 = V_{CC}, S1 = S2 GND ($\overline{SUM}$ mode)
(3)	Any $\overline{A}$ or $\overline{B}$	Cn + 4	M = GND, S0 = S3 = GND, S1 = S2 V_{CC} ($\overline{DIFF}$ mode)
(4)	$\overline{Cn}$	Any $\overline{F}$	M = GND ($\overline{SUM}$ or $\overline{DIFF}$ mode)
(5)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = GND, S0 = S3 = V_{CC}, S1 = S2 GND ($\overline{SUM}$ mode)
(6)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = GND, S0 = S3 = GND, S1 = S2 V_{CC} ($\overline{DIFF}$ mode)
(7)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M = GND, S0 = S3 = V_{CC}, S1 = S2 GND ($\overline{SUM}$ mode)
(8)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M = GND, S0 = S3 = GND, S1 = S2 V_{CC} ($\overline{DIFF}$ mode)
(9)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M = GND, S0 = S3 = V_{CC}, S1 = S2 GND ($\overline{SUM}$ mode)
(10)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M = GND, S0 = S3 = GND, S1 = S2 V_{CC} ($\overline{DIFF}$ mode)
(11)	$\overline{Ai}$ or $\overline{Bi}$	Fi	M = V_{CC} (Logic mode)
(12)	Any $\overline{A}$ or $\overline{B}$	A = B	M = GND, S0 = S3 = GND, S1 = S2 V_{CC} ($\overline{DIFF}$ mode)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



Input Condition :

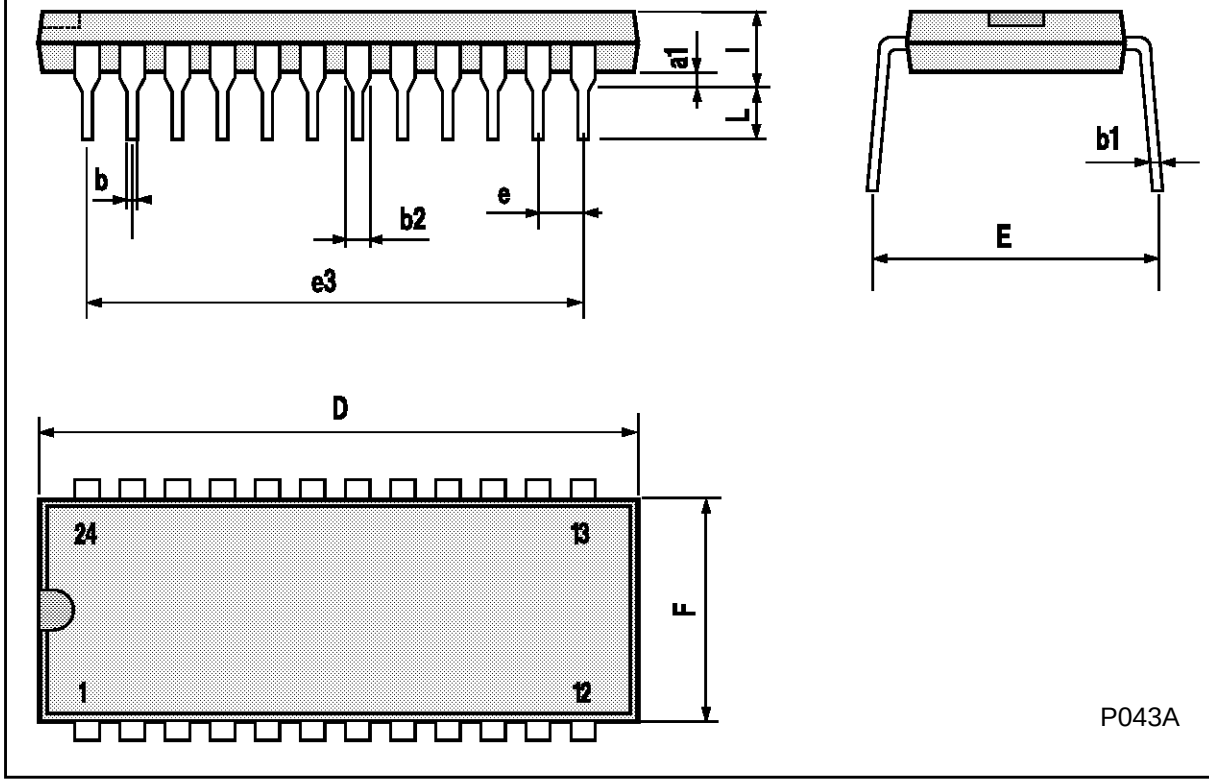
$\overline{A0}$, $\overline{A1}$, $\overline{A2}$, $\overline{A3}$, S0, S3, Cn = V_{DD}

$\overline{B1}$, $\overline{B2}$, $\overline{B3}$, S1, S2, M = GND

INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

Plastic DIP24 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	



P043A

SO24 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45° (typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.420
e		1.27			0.05	
e3		13.97			0.55	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
S	8° (max.)