MOTOROLA

FACT SHEET

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MCM69T618

100 MHz Cache Tag/Data RAM (64K x 18)

The MCM69T618 64K x 18 cache tag/data RAM can be used in a variety of applications. These include MIPS R5000, PentiumPro™, and graphics accelerator applications.

GENERAL PART DESCRIPTION

The MCM69T618 is a 1M bit synchronous fast static RAM with integrated tag compare function. It is designed to to be used as tag RAM for 512KB, 1MB, or 2MB secondary cache as well as to be used as a data RAM for 512KB caches. This device is organized as 64K words of 18 bits each, fabricated with Motorola's high performance silicon gate BiCMOS technology. It integrates input registers, output registers, tag comparator, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache tag RAM applications.

Compare cycles begin as read cycles with output disabled so compare data can be loaded into the input register. The comparator compares the data read from the array with the registered input data, and a match signal is generated. The match output is also stored by an output register and released to the match output buffer at the next rising edge of clock (K).

The MCM69T618 operates from a single 3.3 V power supply and all inputs and outputs are LVTTL compatible.

Features:

- MCM69T618–5 = 5 ns Clock–to–Match/10 ns cycle
  MCM69T618–6 = 6 ns Clock–to–Match/12 ns cycle
  MCM69T618–7 = 7 ns Clock–to–Match/13.3 ns cycle
- Single 3.3 V +10%, –5% Power Supply
- Pipelined Data Comparator
- Pipelined Chip Enable and Write Enable for Data (DQ) Output Enable Path
- 64K x 18 Organization Supports Up to 2MB Cache
- Synchronous Data Input Register Load Enable ($\overline{DE}$)
- Internally Self–Timed Write Cycle
- Asynchronous Data I/O Output Enable ($\overline{G}$)
- Asynchronous Match Output Enable ($\overline{MG}$)
- 119 Bump, 50 mil (1.27 mm) Pitch, 7 x 17 Plastic Ball Grid Array (PBGA) and 100 Pin TQFP Packages.

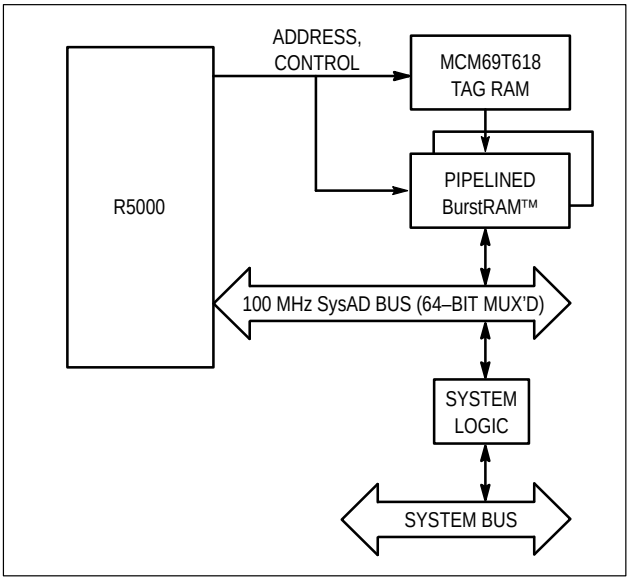
APPLICATION EXAMPLES

MIPS R5000

- L2 Cache Tag RAM
- L2 Cache Data RAM

The MCM69T618 provides very fast tag look–up and achieves as little as two–cycle latency for cache hits on the processor's 100 MHz SysAD Bus. The RAM has an integrated comparator and delivers fast MATCH output timing. Because the R5000 integrates the L2 cache controller, only tag and data store are needed to complete the L2 cache design.

This RAM can also be used as the data store for the L2 cache. Four chips complete a 512KB cache. Chip expansion pins are provided to easily build 128K x 72 data storage.



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BurstRAM is a trademark of Motorola, Inc.

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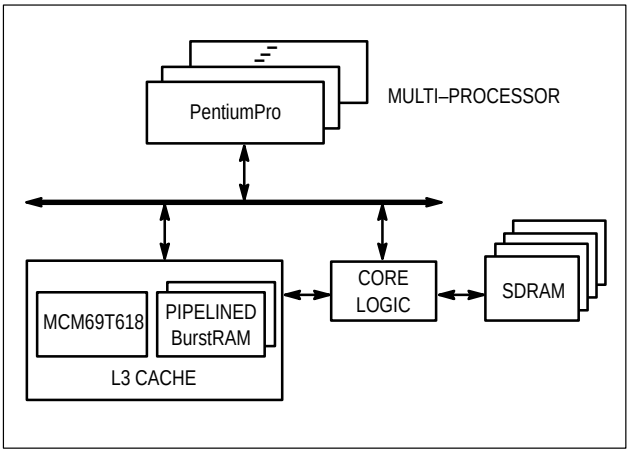
PentiumPro

- L3 Cache Tag RAM

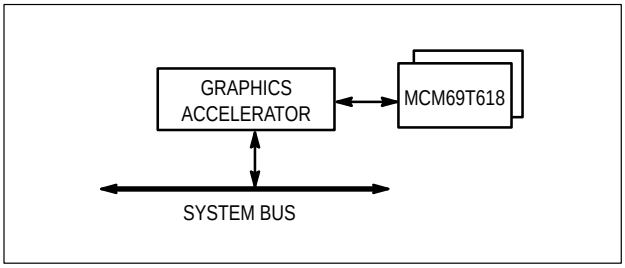
The MCM69T618 is used as an L3 tag RAM for PentiumPro L3 cache designs. An external L3 controller designed with this tag RAM and popular pipelined BurstRAMs provide a higher level of performance for PentiumPro systems.



Graphics Accelerator

- 100 MHz Data Storage

High speed graphics rendering engines use the MCM69T618 for fast local data storage. Accelerators that perform 3D animation, virtual reality, or mechanical design graphics can take advantage of this fast SRAM's simple interface, low latency, and high bandwidth for these applications.



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