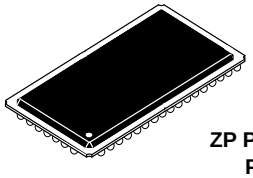
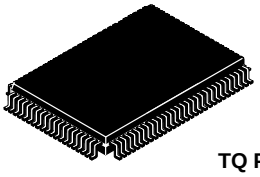
MCM69T618

Product Preview

64K x 18 Bit Synchronous Pipelined Cache Tag RAM



ZP PACKAGE
PBGA
CASE 999–01



TQ PACKAGE
TQFP
CASE 983A–01

The MCM69T618 is a 1M bit synchronous fast static RAM with integrated tag compare function. It is designed to address tag RAM for 512KB, 1MB, or 2MB secondary cache as well as to be used as a data RAM for 512KB caches. This device is organized as 64K words of 18 bits each, fabricated with Motorola's high performance silicon gate BiCMOS technology. It integrates input registers, output registers, tag comparators, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache tag RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQ), write enable ($\overline{SW}$) and chip enable (SE0 and $\overline{SE1}$) are all controlled through positive–edge–triggered noninverting registers. Data enable ($\overline{DE}$) is sampled on the rising clock edge while output enable ($\overline{G}$) and match output enable ($\overline{MG}$) are asynchronous.

Write cycles are internally self–timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

For read cycles, pipelined SRAM output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (K).

Compare cycles begin as read cycles with output disabled so compare data can be loaded into the input register. The comparator compares the read data with the registered input data, and a match signal is generated. The match output is also stored by an output register and released to the match output buffer at the next rising edge of clock (K).

The MCM69T618 operates from a single 3.3 V power supply and all inputs and outputs are LVTTL compatible.

- MCM69T618–5 = 5 ns Clock–to–Match / 10 ns cycle
  MCM69T618–6 = 6 ns Clock–to–Match / 12 ns cycle
  MCM69T618–7 = 7 ns Clock–to–Match / 13.3 ns cycle
- Single 3.3 V +10%, –5% Power Supply
- Pipelined Data Comparator
- Pipelined Chip Enable and Write Enable for Data (DQ) Output Enable Path
- 64K x 18 Organization Supports Up to 2MB Cache
- Synchronous Data Input Register Load Enable ($\overline{DE}$)
- Internally Self–Timed Write Cycle
- Asynchronous Data I/O Output Enable ($\overline{G}$)
- Asynchronous Match Output Enable ($\overline{MG}$)
- 119 Bump, 50 mil (1.27 mm) Pitch, 7 x 17 Plastic Ball Grid Array (PBGA) and 100 Pin TQFP Packages.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 1
3/18/96

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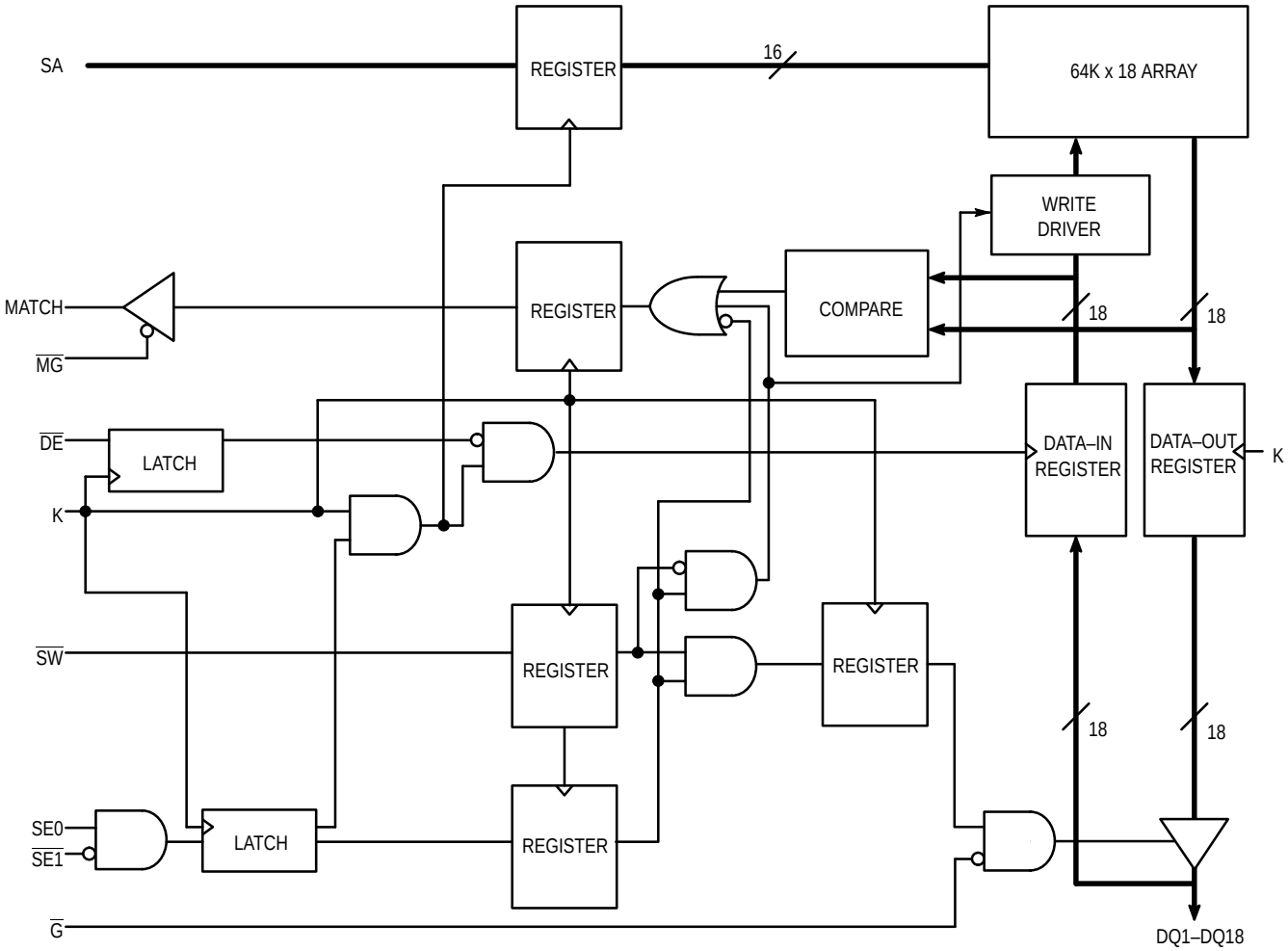
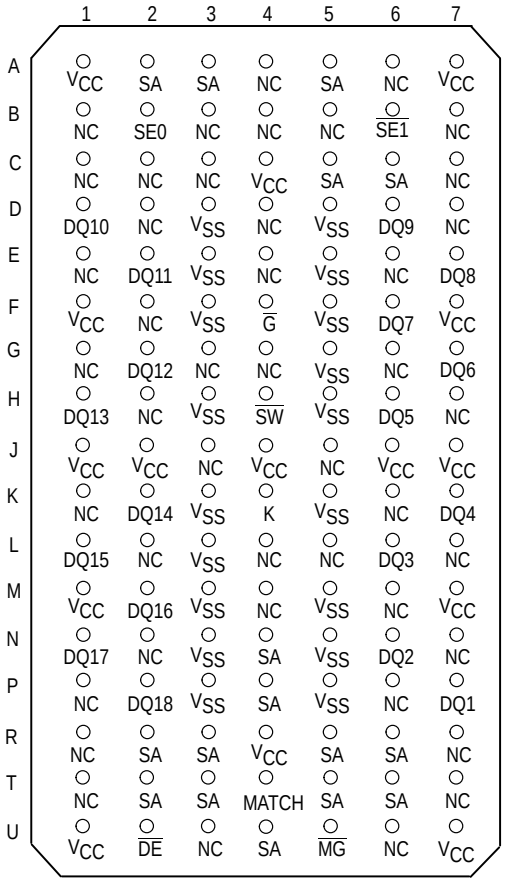
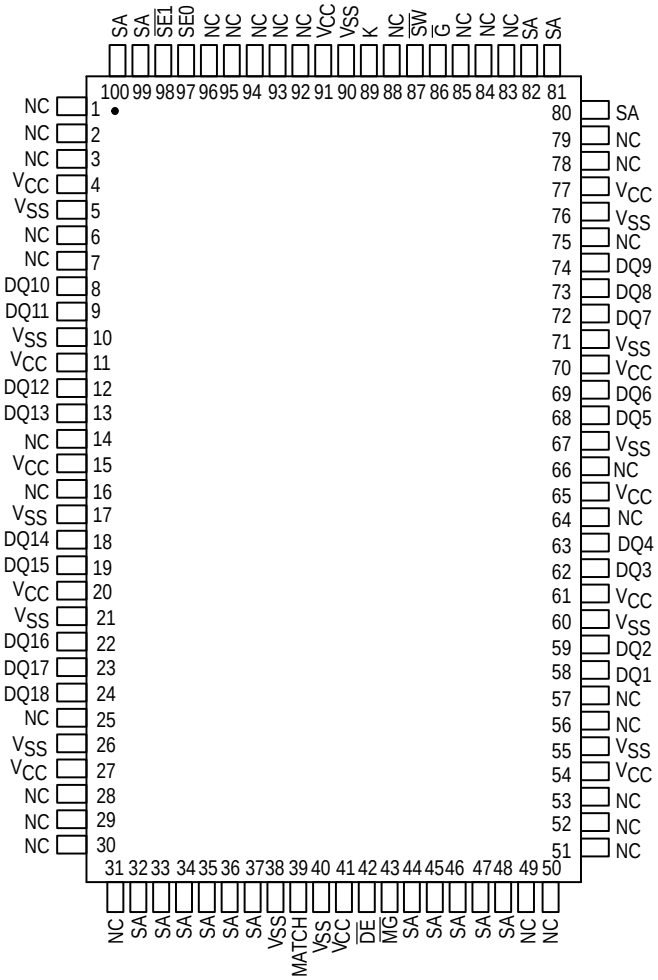
FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS



TOP VIEW 119 BUMP PBGA



TOP VIEW 100 PIN TQFP

Not to Scale

PIN DESCRIPTIONS

PBGA Pin Locations	TQFP Pin Locations	Symbol	Type	Description
2A, 3A, 5A, 5C, 6C, 4N, 4P, 2R, 3R, 5R, 6R, 2T, 3T, 5T, 6T, 4U	32, 33, 34, 35, 36, 37, 44, 45, 46, 47, 48, 80, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge. The address pins select one of the 64K tag entries.
4K	89	K	Input	Clock: All the signals except $\overline{G}$ and $\overline{MG}$ are controlled by the clock.
4H	87	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. The $\overline{SW}$ input specifies whether a read or write cycle is to occur when the chip is enabled. A write command should not be issued within three cycles of a read command unless $\overline{G}$ is high or output drive contention may occur.
2B	97	SE0	Input	Synchronous Chip Enable: Registered on the rising clock edge, active high.
6B	98	$\overline{SE1}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4F	86	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low. $\overline{G}$ must be low for read data to be output two cycles after a read command. If $\overline{G}$ is high, the data output DQ will remain in high impedance even if a read command occurs internally.
1D, 6D, 2E, 7E, 6F, 2G, 7G, 1H, 6H, 2K, 7K, 1L, 6L, 2M, 1N, 6N, 2P, 7P	8, 9, 12, 13, 18, 19, 22, 23, 24, 58, 59, 62, 63, 68, 69, 72, 73, 74	DQ1 – DQ18	I/O	Synchronous Data I/O: For write cycles, registered on the rising clock edge. Two cycles after a read command, the read data is output on the DQ pins provided that $\overline{G}$ is low. On the same cycle of a write command, the write data is input on the DQ signals.
2U	42	$\overline{DE}$	Input	Data Enable Input: Latched on the rising clock edge, active low. The data input register is only updated when $\overline{DE}$ is low.
5U	43	$\overline{MG}$	Input	Match Output Enable: Asynchronous pin, active low. When $\overline{MG}$ is low, the MATCH output driver is on, otherwise the MATCH output driver is in high impedance.
4T	39	MATCH	Output	Two cycles after a compare cycle and if $\overline{MG}$ is low, MATCH will be high if the data presented to the DQ inputs matches the data stored in the RAM. MATCH will be low if the data does not match.
1A, 7A, 4C, 1F, 7F, 1J, 2J, 4J, 6J, 7J, 1M, 7M, 4R, 1U, 7U	4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{CC}	Supply	Power Supply: 3.3 V +10%, –5%. These pins act as thermal vias to pcb power plane for the PBGA package.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P	5, 10, 17, 21, 26, 38, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground: These pins act as thermal vias to pcb ground plane for the PBGA package.
4A, 6A, 1B, 3B, 4B, 5B, 7B, 1C, 2C, 3C, 7C, 2D, 4D, 7D, 1E, 4E, 6E, 2F, 1G, 3G, 4G, 6G, 2H, 7H, 3J, 5J, 1K, 6K, 2L, 4L, 5L, 7L, 4M, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 7T, 3U, 6U	1, 2, 3, 6, 7, 14, 16, 25, 28, 29, 30, 31, 49, 50, 51, 52, 53, 56, 57, 64, 66, 75, 78, 79, 83, 84, 85, 88, 92, 93, 94, 95, 96	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	$\overline{SE}$	$\overline{SW}$	$\overline{DE}$	$\overline{MG}$	$\overline{G}$	Match	DQ
Read	0	1	X	X	0	—	Data Out
Write	0	0	0	X	1	—	Data In
Compare	0	1	0	0	1	Data Out	Data In
Fill Write	0	0	1	X	1	—	High–Z
Deselected (Match Out)	1	X	X	0	X	Data High	High–Z
Deselected	1	X	X	1	X	High–Z	High–Z

NOTES: 1. X = Don't Care. 1 = logic high. 0 = logic low.
2. $\overline{SE}$ low is defined as $\overline{SE1}$ = 0 and SE0 = 1. $\overline{SE}$ high is defined as $\overline{SE1}$ = 1 or SE0 = 0.
3. $\overline{G}$ and $\overline{MG}$ are asynchronous signals and are not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) when $\overline{G}$ goes low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}		V_{in}, V_{out}	V_{CC} + 0.5	V
Output Current (per I/O)		I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	PBGA TQFP	P_D	2.1 1.6	W
Temperature Under Bias		T_{bias}	– 10 to 85	°C
Storage Temperature		T_{stg}	– 55 to 125	°C

NOTES: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	PBGA	TQFP	Unit	Notes
Thermal Resistance (Still Air)			**Max**	**Max**		1
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	41 19	40 25	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	11	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V +10%, –5%, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.135	3.3	3.6	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.5**	V

* $V_{IL} \geq$ – 1.5 V for $t \leq t_{KHKH}/2$.
** $V_{IH} \leq V_{CC}$ + 1.0 V for $t \leq t_{KHKH}/2$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (0 V ≤ V_{in} ≤ V_{CC})		$I_{lkg(I)}$	—	—	± 1	µA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{CC})		$I_{lkg(O)}$	—	—	± 1	µA
AC Supply Current (Device Selected, All Outputs Open, All Inputs Toggling at $V_{in} \leq V_{IL}$ or $\geq V_{IH}$, Cycle Time ≥ t_{KHKH} min)	MCM69T618–5 MCM69T618–6 MCM69T618–7	I_{CCA}	— — —	— — —	240 225 220	mA
CMOS Standby Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{CC} – 0.2 V)	MCM69T618–5 MCM69T618–6 MCM69T618–7	I_{SB1}	—	—	130 110 105	mA
Clock Running Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{CC} – 0.2 V)	MCM69T618–5 MCM69T618–6 MCM69T618–7	I_{SB2}	— — —	— — —	45 40 40	mA
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = –4 mA)		V_{OH}	2.4	—	—	V

NOTE: 1. Device in Deselected mode as defined by the Truth Table.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	3	5	pF
Input/Output Capacitance	$C_{I/O}$	—	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V +10%, –5%, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM69T618–5		MCM69T618–6		MCM69T618–7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12	—	13.3	—	ns	
Clock High Pulse Width	t_{KHKL}	3.5	—	4	—	4.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	3.5	—	4	—	4.5	—	ns	
Clock High to Match Valid	t_{KHMV}	—	5	—	6	—	7	ns	
Clock Access Time	t_{KHQV}	—	5	—	6	—	7	ns	4
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	5	ns	4
Match Output Enable to Match Valid	t_{MGLMV}	—	5	—	5	—	5	ns	4
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	4. 6
Clock High to Output Change	t_{KHQX2}	1.5	—	1.5	—	1.5	—	ns	4
Clock High to Match Output Change	t_{KHMX}	1.5	—	1.5	—	1.5	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 6
Match Output Enable to Match Active	t_{MGLMX}	0	—	0	—	0	—	ns	4, 6
Output Disable to Q High–Z	t_{GHQZ}	—	5	—	5	—	5	ns	5, 6
Match Output Disable to Match High–Z	t_{MGHMZ}	—	5	—	5	—	5	ns	6
Clock High to Q High–Z	t_{KHQZ}	1.5	5	1.5	5	1.5	5	ns	5, 6
Setup Times: Address, Data In, Write, Enable	t_{AVKH}, t_{DVKH}, t_{WVKH}, t_{EVKH}	2.5	—	2.5	—	2.5	—	ns	
Hold Times: Address, Data In, Write, Enable	t_{KHAX}, t_{KHDX}, t_{KHWX}, t_{KHEX}	0.5	—	0.5	—	0.5	—	ns	

NOTES:
1. “Write” applies to the $\overline{SW}$ signal. “Enable” applies to SE0, $\overline{SE1}$, and $\overline{DE}$ signals.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don’t care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
4. Tested per AC Test Load.
5. Measured at ± 200 mV from steady state. Tested per High–Z test load.
6. This parameter is sampled and not 100% tested.

AC TEST LOADS

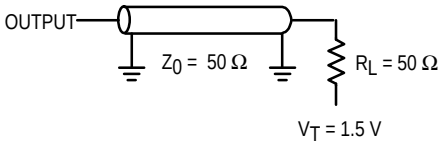


Figure 1A. AC Test Load

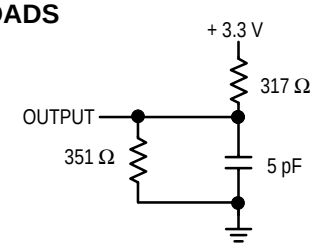
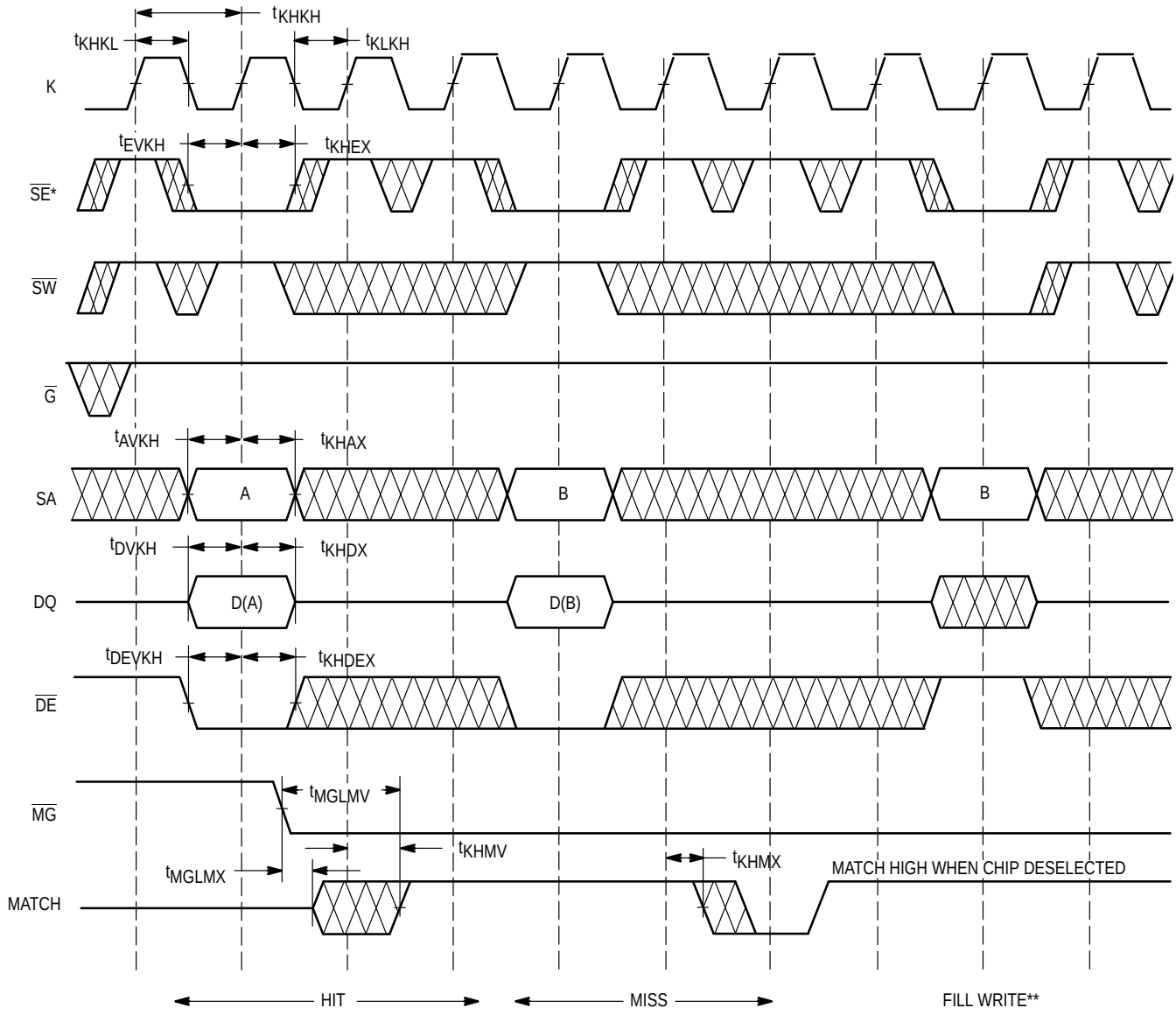


Figure 1B. High–Z Test Load

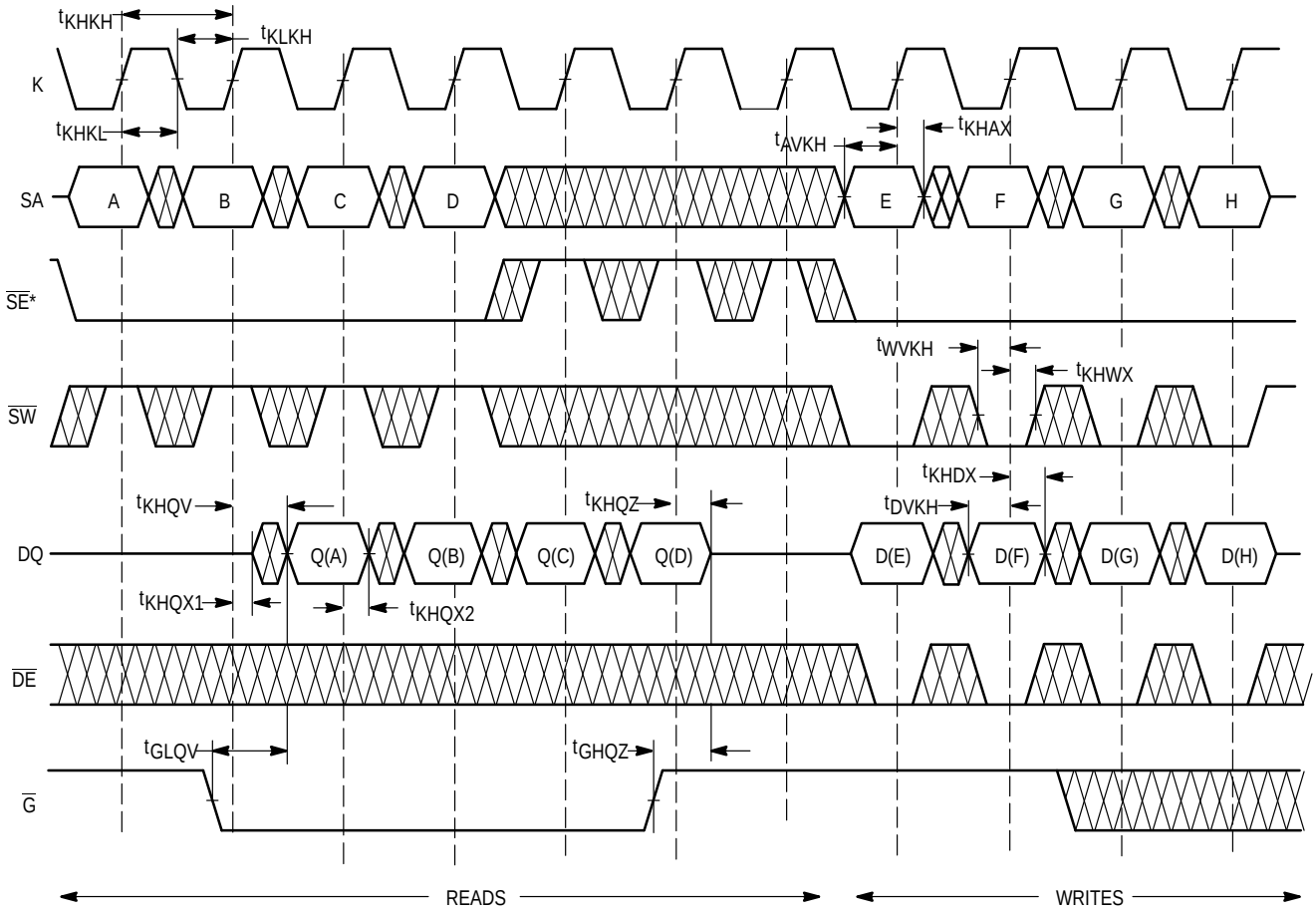
COMPARE/FILL WRITE CYCLES



* $\overline{SE}$ low = SE0 high and $\overline{SE1}$ low.

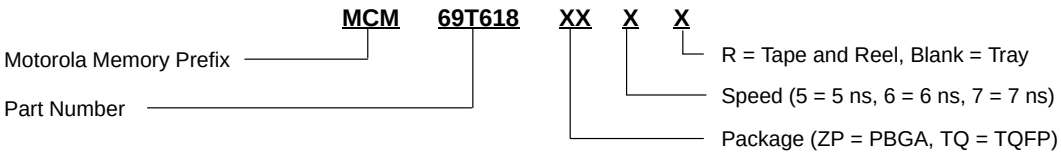
** During fill write sequence, tag entry is written with tag value retained in the data input register from the previous compare cycle.

READ/WRITE CYCLES



* $\overline{SE}$ low = SE0 high and $\overline{SE1}$ low.

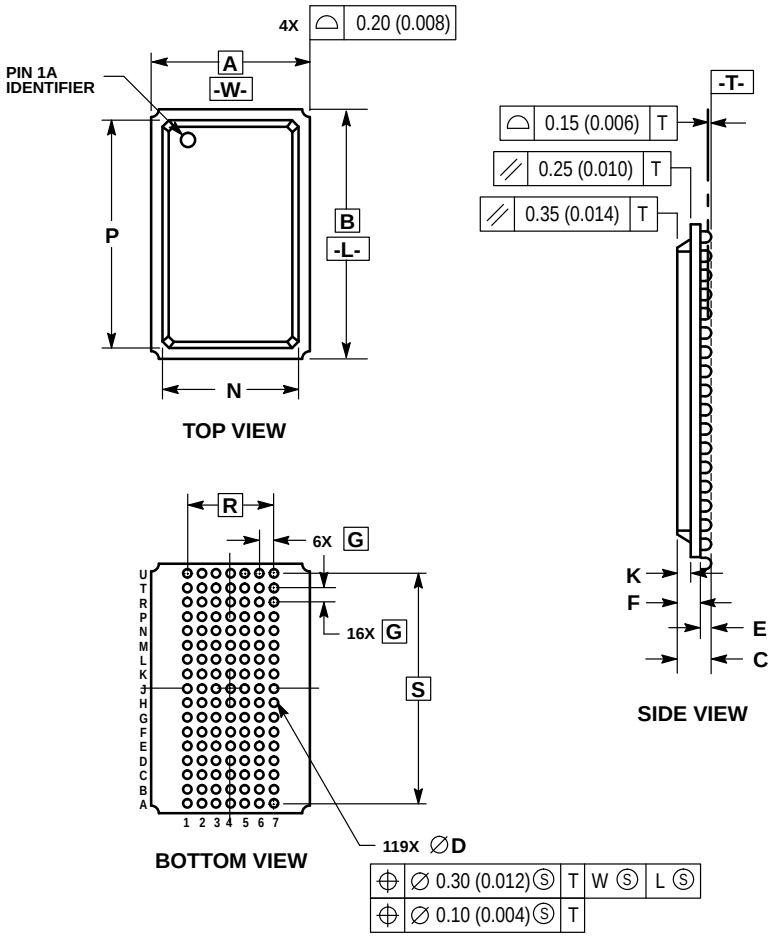
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers —	MCM69T618ZP5	MCM69T618ZP6	MCM69T618ZP7
	MCM69T618ZP5R	MCM69T618ZP6R	MCM69T618ZP7R
	MCM69T618TQ5	MCM69T618TQ6	MCM69T618TQ7
	MCM69T618TQ5R	MCM69T618TQ6R	MCM69T618TQ7R

PACKAGE DIMENSIONS

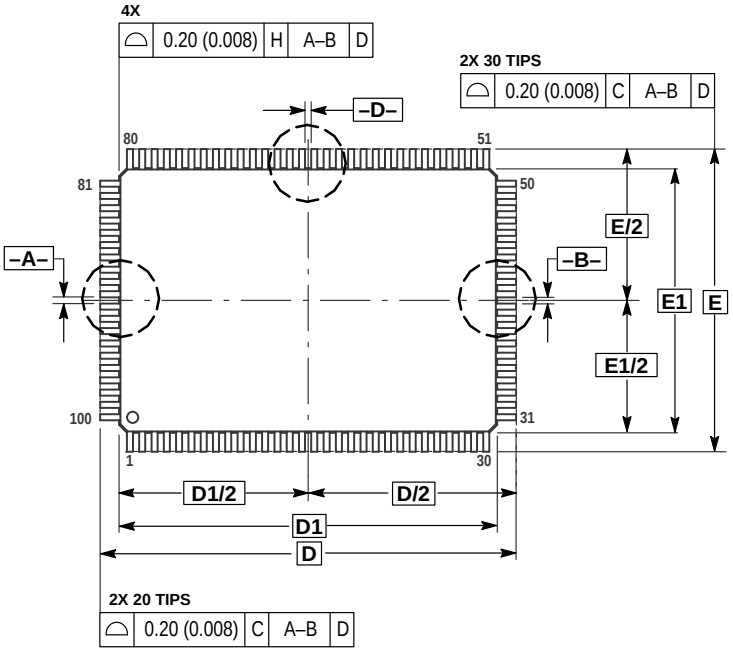
ZP PACKAGE
7 X 17 BUMP PBGA
CASE 999–01

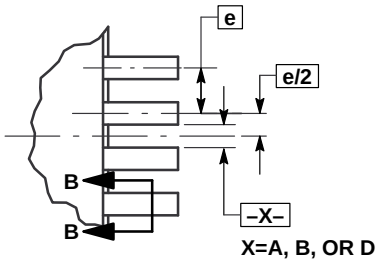


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

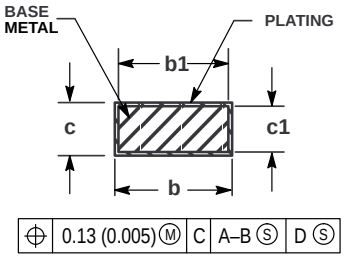
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.00 BSC		0.551 BSC	
B	22.00 BSC		0.866 BSC	
C	—	2.40	—	0.094
D	0.60	0.90	0.024	0.035
E	0.50	0.70	0.020	0.028
F	1.30	1.70	0.051	0.067
G	1.27 BSC		0.050 BSC	
K	0.80	1.00	0.031	0.039
N	11.90	12.10	0.469	0.476
P	19.40	19.60	0.764	0.772
R	7.62 BSC		0.300 BSC	
S	20.32 BSC		0.800 BSC	

TQ PACKAGE
TQFP
CASE 983A–01

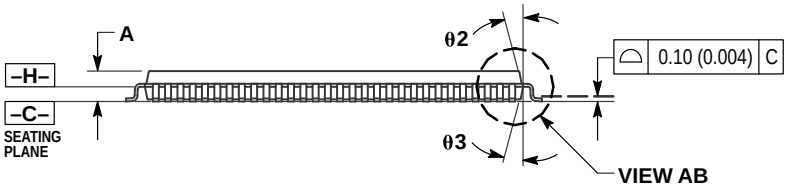




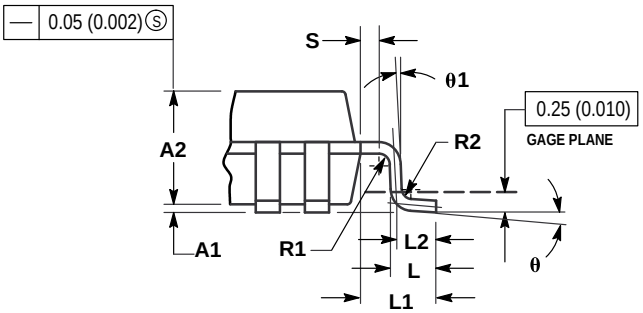
VIEW Y



SECTION B–B



VIEW AB



VIEW AB

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS D1 AND B1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.45 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015
b1	0.22	0.33	0.009	0.013
c	0.09	0.20	0.004	0.008
c1	0.09	0.16	0.004	0.006
D	22.00 BSC		0.866 BSC	
D1	20.00 BSC		0.787 BSC	
E	16.00 BSC		0.630 BSC	
E1	14.00 BSC		0.551 BSC	
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
L1	1.00 REF		0.039 REF	
L2	0.50 REF		0.020 REF	
S	0.20	—	0.008	—
R1	0.08	—	0.003	—
R2	0.08	0.20	0.003	0.008
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	11°	13°	11°	13°
θ3	11°	13°	11°	13°

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