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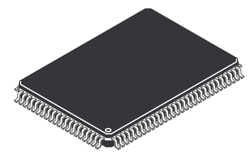
MCM69F737



TQ PACKAGE
TQFP
CASE 983A–01

Product Preview

128K x 36 Bit Flow–Through BurstRAM™ Synchronous Fast Static RAM

The MCM69F737 is a 4M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the PowerPC™ and other high performance microprocessors. It is organized as 128K words of 36 bits each. This device integrates input registers, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K).

Addresses (SA), data inputs (DQx), and all control signals except output enable (G) and Linear Burst Order (LBO) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either ADSP or ADSC input pins. Subsequent burst addresses can be generated internally by the MCM69F737 (burst sequence operates in linear or interleaved mode dependent upon state of LBO) and controlled by the burst address advance (ADV) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write (SBx), synchronous global write (SGW), and synchronous write enable (SW) are provided to allow writes to either individual bytes or to all bytes. The four bytes are designated as “a”, “b”, “c”, and “d”. SBa controls DQa, SBb controls DQb, etc. Individual bytes are written if the selected byte writes SBx are asserted with SW. All bytes are written if either SGW is asserted or if all SBx and SW are asserted.

For read cycles, a flow–through SRAM allows output data to simply flow freely from the memory array.

The MCM69F737 operates from a 3.3 V core power supply and all outputs operate on a 2.5 V power supply. All inputs and outputs are JEDEC standard JESD8–5 compatible.

- MCM69F737 Speed Options

Speed	t_{KHKH}	Flow–Through t_{KHQV}	Setup	Hold	I_{DD}
117 MHz	8.5 ns	7.5 ns	2 ns	0.5 ns	350 mA
100 MHz	10 ns	8 ns	2 ns	0.5 ns	325 mA
90 MHz	11 ns	8.5 ns	2 ns	0.5 ns	300 mA

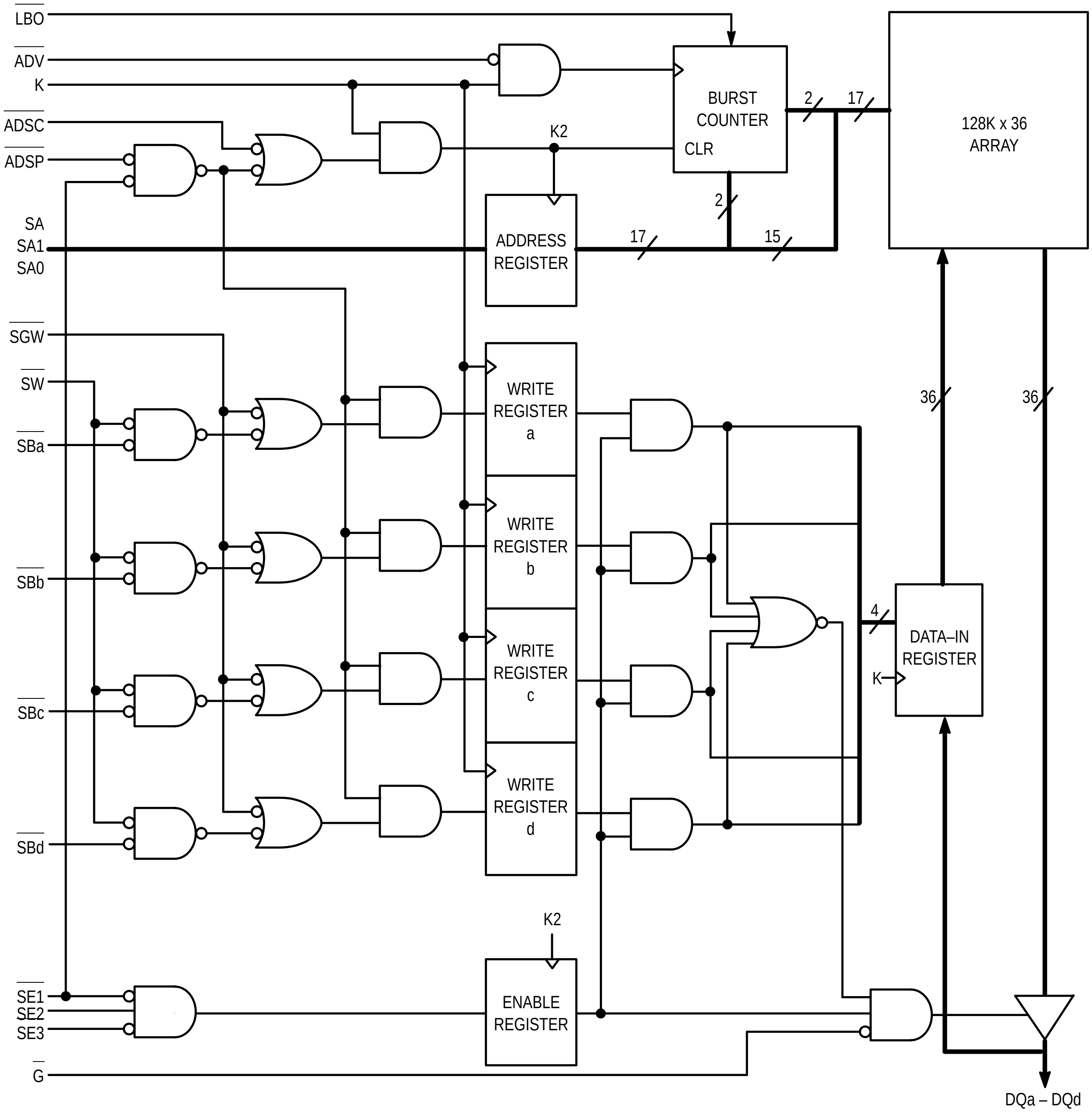
- 3.3 V + 10%, – 5% Core Power Supply, 2.5 V I/O Supply
- ADSP, ADSC, and ADV Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Single–Cycle Deselect Timing
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- JEDEC Standard 100 Pin TQFP Package

BurstRAM is a trademark of Motorola, Inc.
PowerPC is a trademark of IBM Corp.

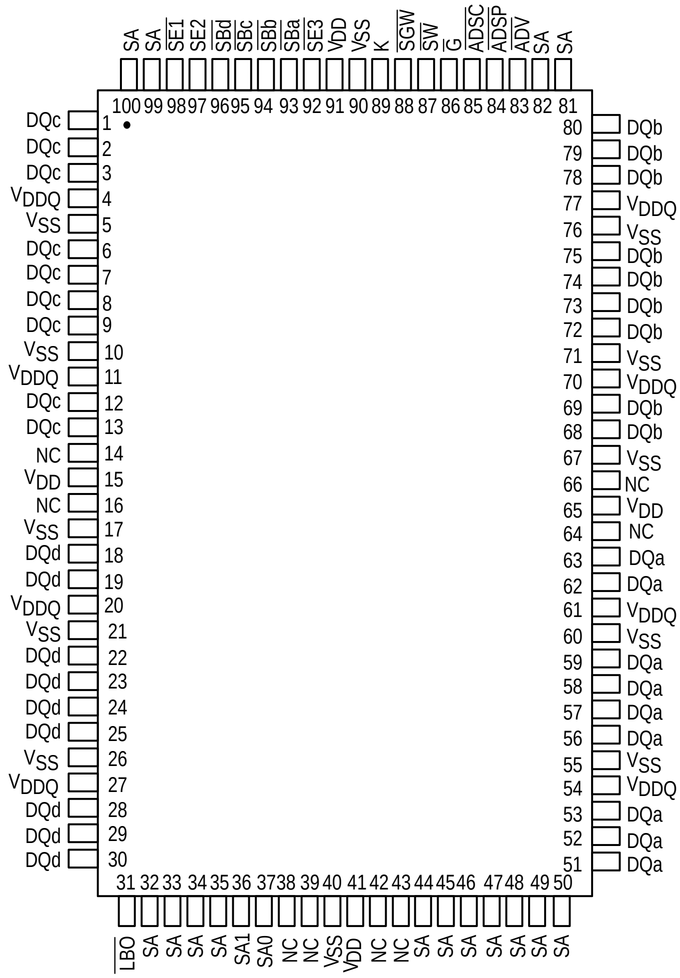
This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

8/7/96

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS



TOP VIEW

Not to Scale

PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Initiates READ, WRITE, or chip deselect cycle.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ, WRITE, or chip deselect cycle (exception — chip deselect does not occur when ADSP is asserted and SE1 is high).
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 51, 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79, 80 (c) 1, 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29, 30	DQx	I/O	Synchronous Data I/O: “x” refers to the byte being read or written (byte a, b, c, d).
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except G and LBO.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1,SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94, 95, 96 (a) (b) (c) (d)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: “x” refers to the byte being written (byte a, b, c, d). SGW overrides SBx.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks ADSP or deselects chip when ADSC is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the SBx and SW signals. If only byte write signals SBx are being used, tie this pin high.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write SBx pins. If only byte write signals SBx are being used, tie this pin low.
15, 41, 65, 91	V_{DD}	Supply	Core Power Supply.
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	Supply	I/O Power Supply.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
14, 16, 38, 39, 42, 43, 64, 66	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 5)

Next Cycle	Address Used	$\overline{\text{SE1}}$	SE2	$\overline{\text{SE3}}$	$\overline{\text{ADSP}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	$\overline{\text{G}}$ 3	DQx	Write 2, 4
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	X	High–Z	X5
Begin Read	External	0	1	0	1	0	X	X	High–Z	READ5
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES:
1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{\text{SBx}}$ and $\overline{\text{SW}}$ low or 2) $\overline{\text{SGW}}$ is low.
3. $\overline{\text{G}}$ is an asynchronous signal and is not sampled by the clock K. $\overline{\text{G}}$ drives the bus immediately (t_{GLQX}) following $\overline{\text{G}}$ going low.
4. On write cycles that follow read cycles, $\overline{\text{G}}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{\text{G}}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.
5. This read assumes the RAM was previously deselected.

LINEAR BURST ADDRESS TABLE ($\overline{\text{LBO}}$ = V_{SS})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{\text{LBO}}$ = V_{DD})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	SGW	SW	SBa	SBb	SBc	SBd
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte a	H	L	L	H	H	H
Write Byte b	H	L	H	L	H	H
Write Byte c	H	L	L	H	L	H
Write Byte d	H	L	H	L	H	L
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} – 0.5 to + 4.6	V
I/O Supply Voltage (See Note 3)	V_{DDQ}	V_{SS} – 0.5 to V_{DD}	V
Input Voltage Relative to V_{SS} for Any Pin Except V_{DD} (See Note 3)	V_{in}, V_{out}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Input Voltage (Three–State I/O) (See Note 3)	V_{IT}	V_{SS} – 0.5 to V_{DDQ}+ 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.
3. This is a steady–state DC parameter that is in effect after the power supply has achieved its nominal operating level. Power sequencing cannot be controlled, and is not allowed.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS (See Note 1)

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

($3.6\ V \geq V_{DD} \geq 3.135\ V$, $110°C \geq T_J \geq 20°C$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = 0\ V$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.3	—	0.7	V
Input High Voltage	V_{IH}	1.7	—	V_{DD} + 0.3	V
I/O Supply Voltage	V_{DDQ}	2.375	2.5	V_{DD}	V

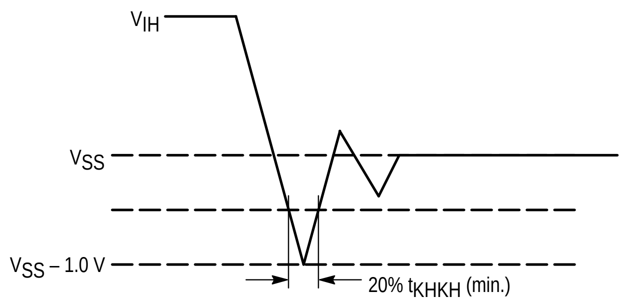


Figure 1. Undershoot Voltage

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input Leakage Current ($0\ V \leq V_{in} \leq V_{DD}$)	$I_{lkg(I)}$	—	—	± 1	µA	
Output Leakage Current ($0\ V \leq V_{in} \leq V_{DDQ}$)	$I_{lkg(O)}$	—	—	± 1	µA	
AC Supply Current (Device Selected, All Outputs Open, Cycle Time ≥ t_{KHKH} min) MCM69F737–7.5 MCM69F737–8 MCM69F737–8.5	I_{DDA}	—	—	350 325 300	mA	2, 3, 4
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH})	I_{SB1}	—	—	130	mA	1, 2, 3, 4
Clock Running Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS} + 0.2\ V$ or $\geq V_{DD} - 0.2\ V$)	I_{SB2}	—	—	30	mA	1
Output Low Voltage (I_{OL} = 2 mA). Refer to Figure 4.	V_{OL}	—	—	0.7	V	
Output High Voltage (I_{OL} = –2 mA). Refer to Figure 4.	V_{OH}	1.7	—	—	V	
Desk Top Suspend Current (Selected, All Inputs ≤ 0.2 V, freq. = max, V_{DD} = max, ADSP and ADSC = Logic High, Outputs Disabled)	I_{DS1}	—	—	TBD	mA	
Desk Top Idle Current (Selected, All Inputs ≤ 0.2 V, freq. = 0, V_{DD} = max, ADSP and ADSC = Logic High, Outputs Disabled)	I_{DS1A}	—	—	TBD	mA	
Desk Top Standby Current (Deselected, All Inputs ≤ 0.2 V, freq. = 0, V_{DDQ} = max, Outputs Disabled)	I_{DS2}	—	—	TBD	mA	

NOTES:
1. Device is deselected as defined by the Truth Table.
2. Reference AC Operating Conditions and Characteristics for input and timing.
3. All addresses transition simultaneously low (LSB) then high (MSB).
4. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $110°C \geq T_J \geq 20°C$, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	5	pF
Input/Output Capacitance	$C_{I/O}$	—	7	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(3.6 V ≥ V_{DD} ≥ 3.135 V, 110°C ≥ T_J ≥ 20°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . 1.25 V
Input Pulse Levels . . . . 0 to 2.5 V
Input Slew Rate (See Note 1) . . . . 1.0 V/ns

Output Timing Reference Level . . . . 1.25 V
Output Load . . . . See Figure 2 Unless Otherwise Noted
Output Rise/Fall Times (max) . . . . 1.8 ns

READ/WRITE CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM69F737–7.5 117 MHz		MCM69F737–8 100 MHz		MCM69F737–8.5 90 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	8.5	—	10	—	11	—	ns	
Clock High Pulse Width	t_{KHKL}	3	—	4	—	4.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	3	—	4	—	4.5	—	ns	
Clock Access Time	t_{KHQV}	—	7.5	—	8	—	8.5	ns	3
Output Enable to Output Valid	t_{GLQV}	—	3.5	—	3.5	—	3.5	ns	3
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	3, 4, 5
Clock High to Output Change	t_{KHQX2}	2	—	2	—	2	—	ns	4, 5
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	3, 4, 5
Output Disable to Q High–Z	t_{GHQZ}	—	3.5	—	3.5	—	3.5	ns	3, 4, 5
Clock High to Q High–Z	t_{KHQZ}	2	3.5	2	3.5	2	3.5	ns	3, 4, 5
Setup Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{ADKH} t_{ADSKH} t_{DVKH} t_{WVKH} t_{EVKH}	2.0	—	2.0	—	2.0	—	ns	3
Hold Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	ns	3

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. Tested per AC Test Load, Figure 2.
4. Measured at ± 200 mV from steady state.
5. This parameter is sampled and not 100% tested.

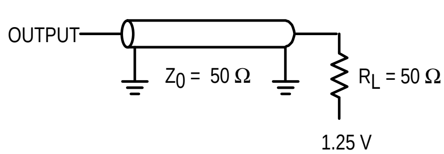
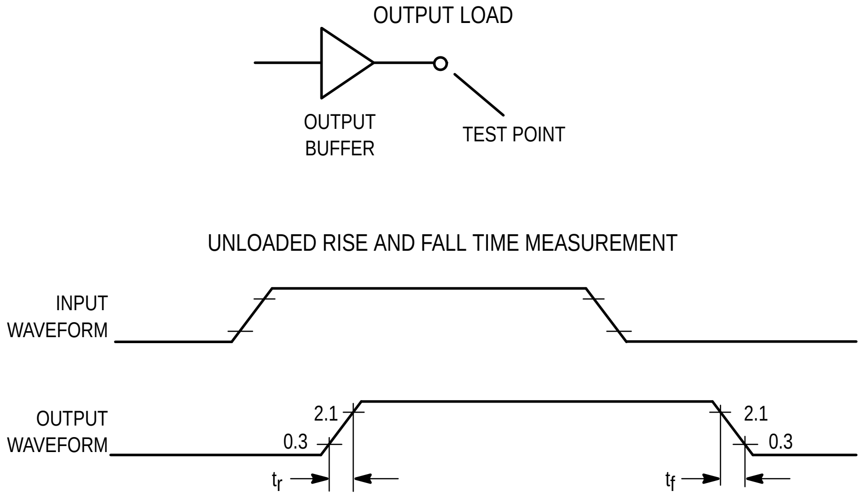


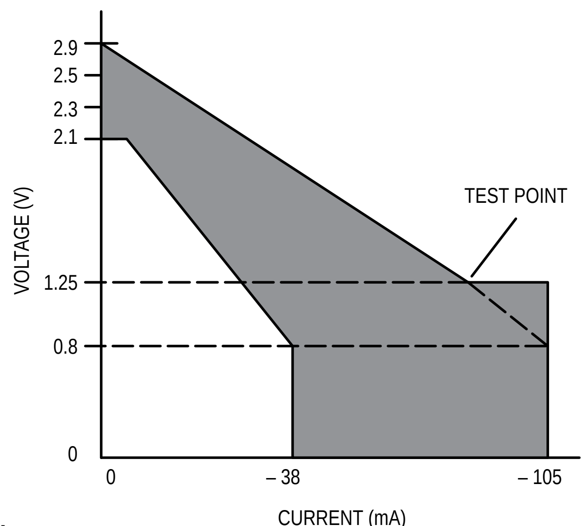
Figure 2. AC Test Load



NOTES:
1. Input waveform has a slew rate of 1 V/ns.
2. Rise time is measured from 0.3 V to 2.1 V unloaded.
3. Fall time is measured from 2.1 V to 0.3 V unloaded.

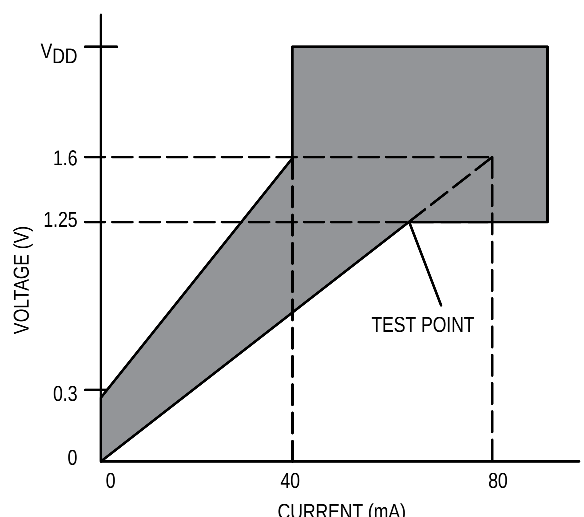
Figure 3. Unloaded Rise and Fall Time Characterization

PULL–UP		
VOLTAGE (V)	I (mA) Min	I (mA) Max
– 0.5	– 38	– 105
0	– 38	– 105
0.8	– 38	– 105
1.25	– 26	– 83
1.5	– 20	– 70
2.3	0	– 30
2.7	0	– 10
2.9	0	0
3.4	0	0



(a) Pull–Up

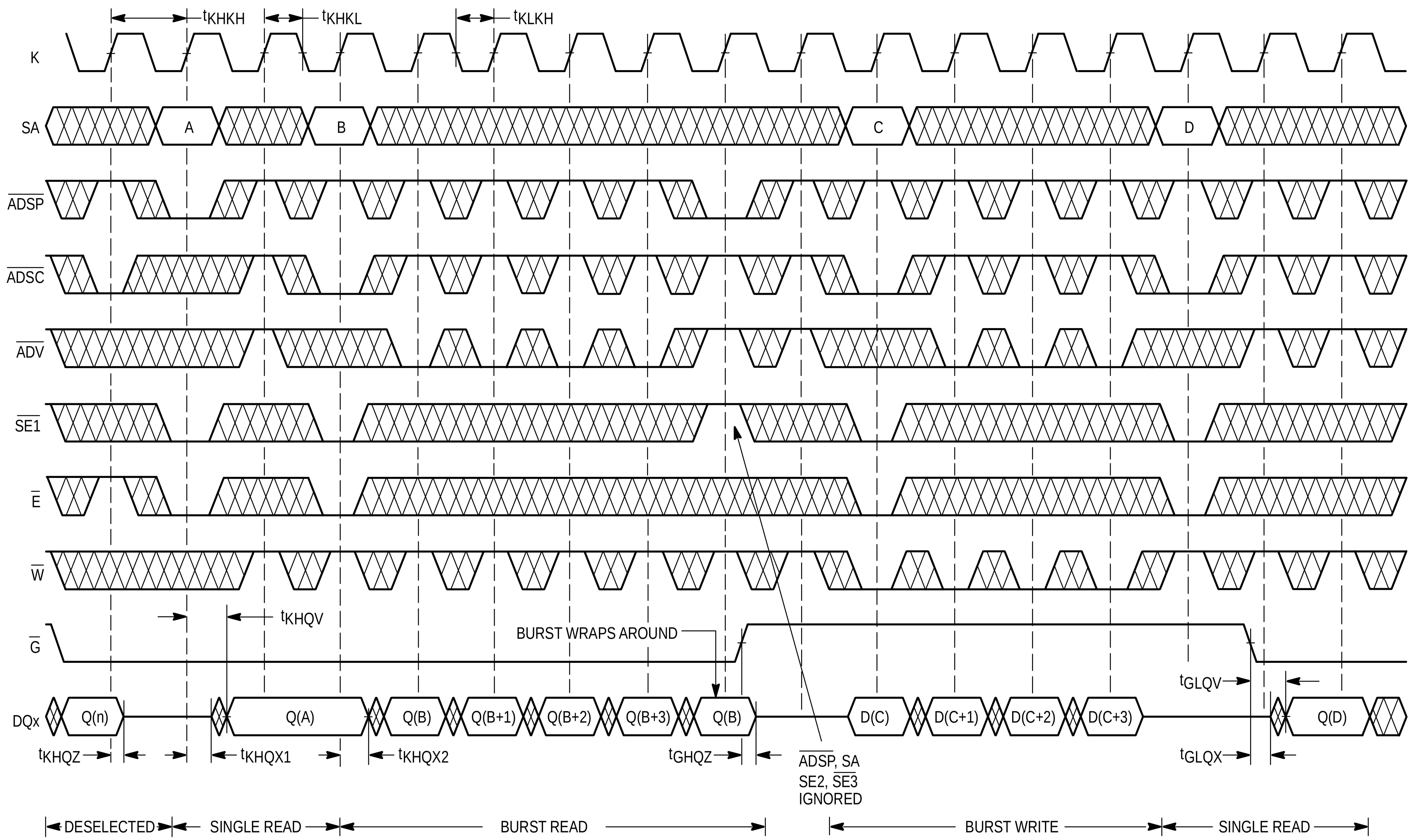
PULL–DOWN		
VOLTAGE (V)	I (mA) Min	I (mA) Max
– 0.5	0	0
0	0	0
0.4	10	20
0.8	20	40
1.25	31	63
1.6	40	80
2.8	40	80
3.2	40	80
3.4	40	80



(b) Pull–Down

Figure 4. Typical Output Buffer Characteristics

READ/WRITE CYCLES



Note: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and/or $\overline{SW}$ and $\overline{SBx}$ low.

APPLICATION INFORMATION

STOP CLOCK OPERATION

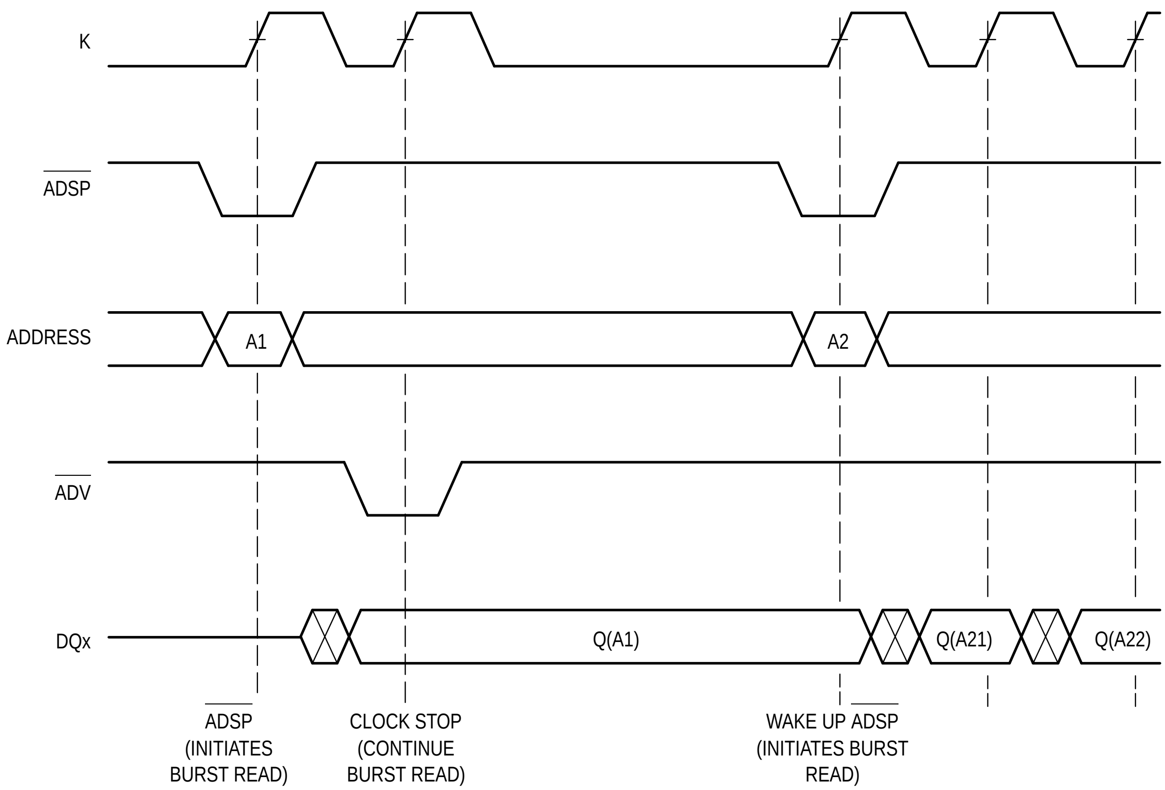
In the stop clock mode of operation, the SRAM will hold all state and data values even though the clock is not running (full static operation). The SRAM design allows the clock to start with ADSP and ADSC, and stops the clock after the last write data is latched, or the last read data is driven out.

When starting and stopping the clock, the AC clock timing and parametrics must be strictly maintained. For example, clock pulse width and edge rates must be guaranteed when starting and stopping the clocks.

To achieve the lowest power operation for all three stop clock modes, stop read, stop write, and stop deselect:

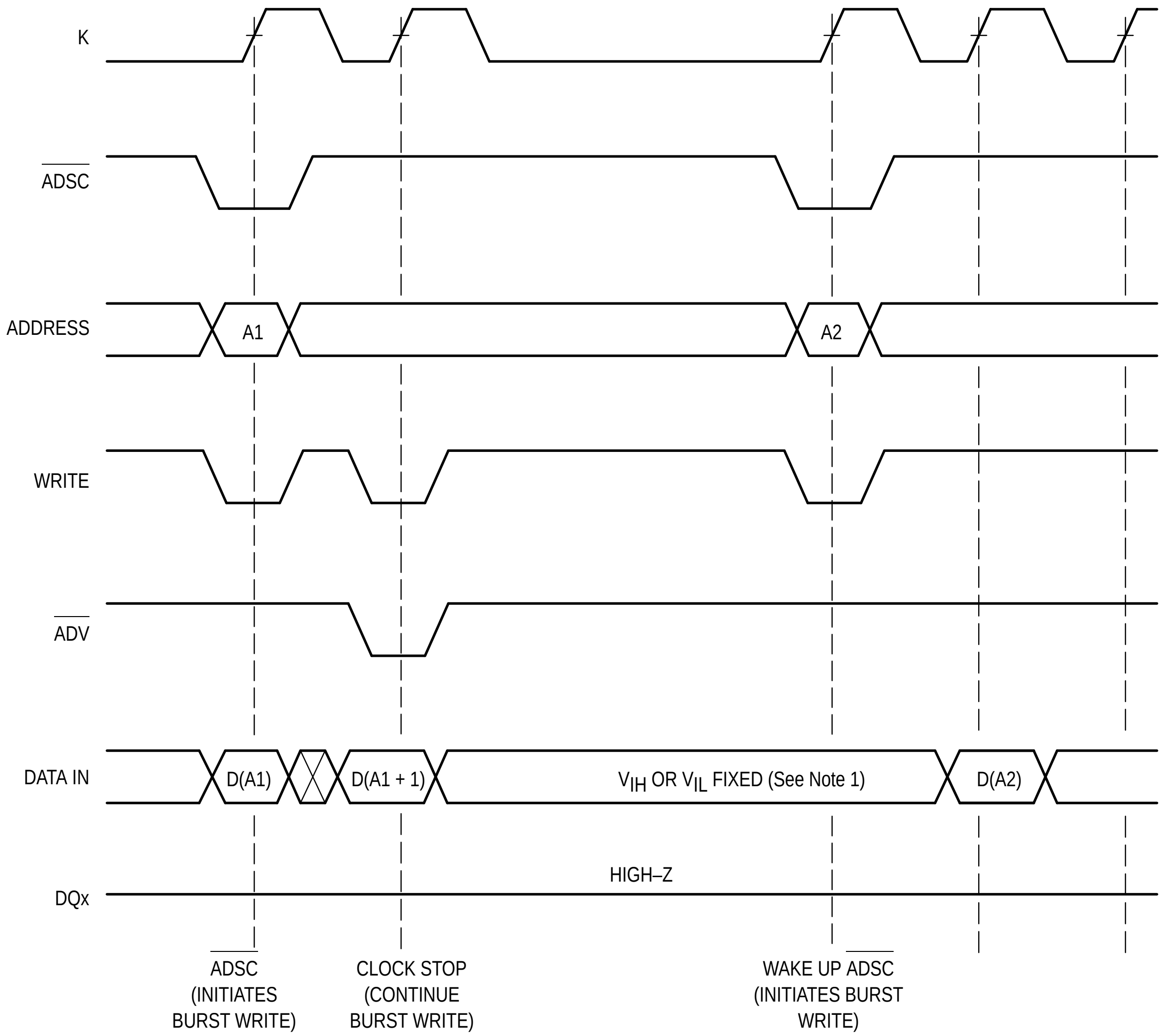
1. Force the clock to a low state.
2. Force the control signals to an inactive state (this guarantees any potential source of noise on the clock input will not start an unplanned on activity).
3. Force the address inputs to a low state (V_{IL}), preferable < 0.2 V.

STOP CLOCK WITH READ TIMING



NOTES:
1. For lowest possible power consumption during stop clock, the addresses should be driven to a low state (V_{IL}). Best results are obtained if V_{IL} < 0.2 V.

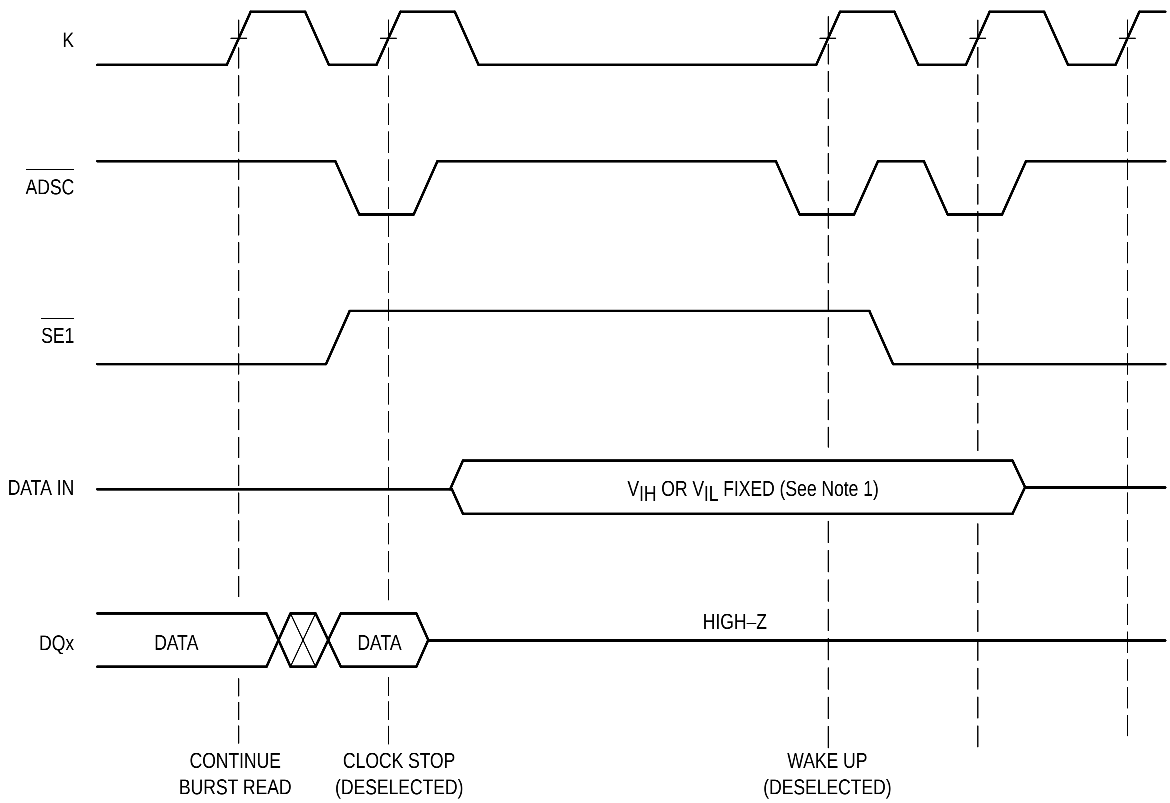
STOP CLOCK WITH WRITE TIMING



NOTES:

1. While the clock is stopped, DATA IN must be fixed in a high (V_{IH}) or low (V_{IL}) state to reduce DC current of the input buffers. For lowest power operation, all data and address lines should be held in a low (V_{IL}) state and control lines held in an inactive state.
2. For best possible power savings, the data–in should be driver low.

STOP CLOCK WITH DESELECT OPERATION TIMING



NOTES:

1. While the clock is stopped, DATA IN must be fixed in a high (V_{IH}) or low (V_{IL}) state to reduce DC current of the input buffers. For lowest power operation, all data and address lines should be held in a low (V_{IL}) state and control lines held in an inactive state.
2. For best possible power savings, the data–in should be driver low.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for PowerPC – and other high end MPU – based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69F737. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 5.

CONTROL PIN TIE VALUES (H ≥ V_{IH}, L ≤ V_{IL})

Non–Burst	ADSP	ADSC	ADV	SE1	LBO
Sync Non–Burst, Flow–through SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

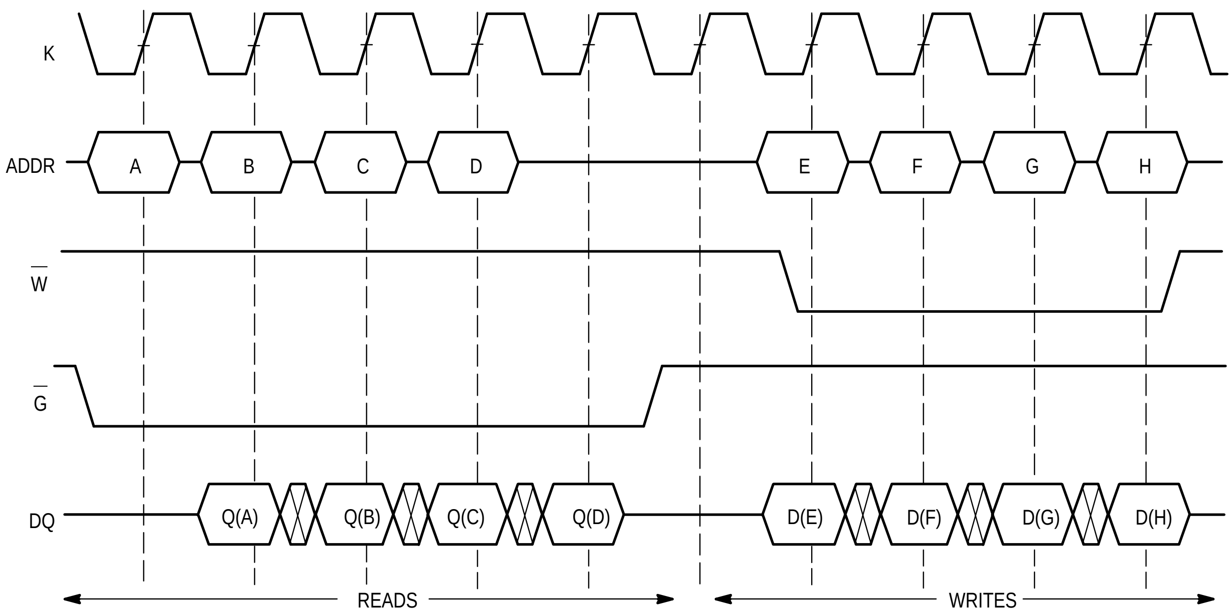


Figure 5. Configured as Non–Burst Synchronous SRAM

ORDERING INFORMATION
(Order by Full Part Number)

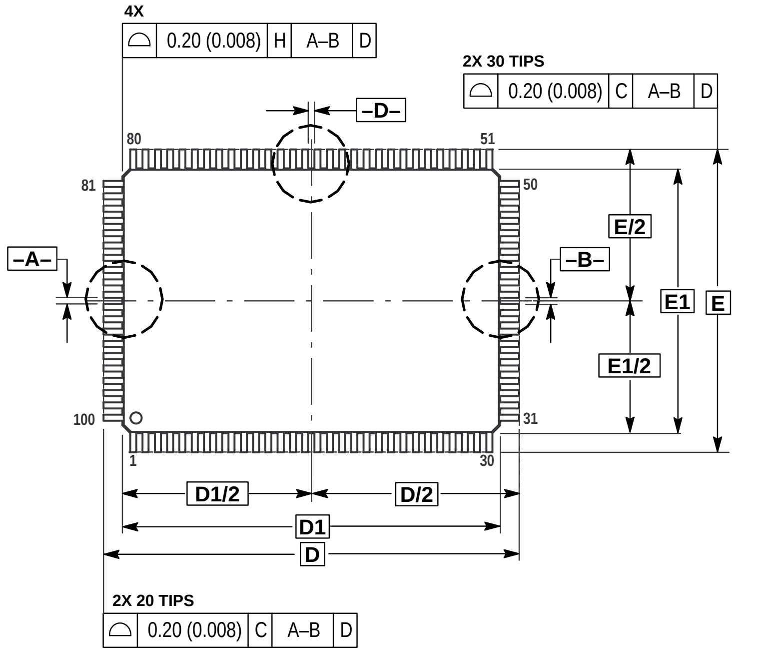
MCM 69F737 XX X X

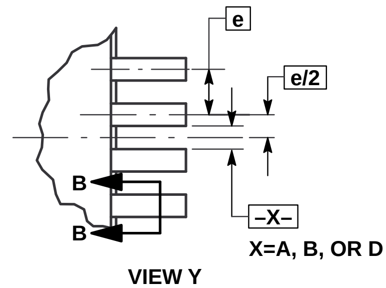
- MCM — Motorola Memory Prefix
- 69F737 — Part Number
- XX — Package (TQ = TQFP)
- X — Speed (7.5 = 7.5 ns, 8 = 8 ns, 8.5 = 8.5 ns)
- X — Blank = Trays, R = Tape and Reel

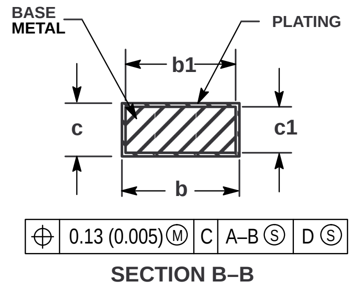
Full Part Numbers — MCM69F737TQ7.5 MCM69F737TQ8 MCM69F737TQ8.5
MCM69F737TQ7.5R MCM69F737TQ8R MCM69F737TQ8.5R

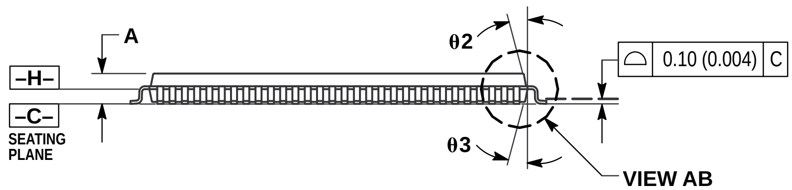
PACKAGE DIMENSIONS

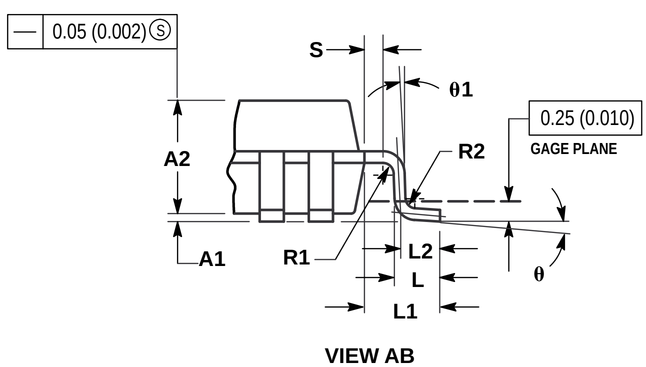
TQ PACKAGE
TQFP
CASE 983A–01











NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS D1 AND B1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.45 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015
b1	0.22	0.33	0.009	0.013
c	0.09	0.20	0.004	0.008
c1	0.09	0.16	0.004	0.006
D	22.00 BSC		0.866 BSC	
D1	20.00 BSC		0.787 BSC	
E	16.00 BSC		0.630 BSC	
E1	14.00 BSC		0.551 BSC	
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
L1	1.00 REF		0.039 REF	
L2	0.50 REF		0.020 REF	
S	0.20	—	0.008	—
R1	0.08	—	0.003	—
R2	0.08	0.20	0.003	0.008
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	11°	13°	11°	13°
θ3	11°	13°	11°	13°

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