

MCM69C232 MCM69C432

Content Addressable Memories for High Performance Internetworking Applications

4K x 64 CAM:

6/10/96

The MCM69C232 and the MCM69C432 are flexible content-addressable memories (CAM) that can contain 4096 and 16384 entries of 64 bits respectively. They are implemented with standard 4-transistor SRAM cells that provide a six to eight fold improvement in cost per bit, compared to existing CAMs. The widths of the match field and the output field are programmable, and the match time is designed to be 160 nanoseconds. As a result, the MCM69C232 and the MCM69C432 are well suited for datacom applications such as Virtual Path Identifier/Virtual Circuit Identifier (VPI/VCI) translation in ATM switches up to OC12 (622 Mbps) data rates and Media Access Control (MAC) address lookup in Ethernet/Fast Ethernet bridges. The match duty cycle of the MCM69C232 and the MCM69C432 is user defined, with a trade-off between the time between matches and the number of new entries added to the CAM per second.

LINE CARD BLOCK DIAGRAM



MCM69C232 AND MCM69C432 BLOCK DIAGRAM



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The Product:

MCM69C232 Features:

- 4096 Entries
- Programmable 12 to 64 Bit Wide Match Field
- Samples Available 4Q96
- Volume Pricing < \$20

MCM69C432 Features:

- 16,384 Entries
- Programmable 14 to 64 Bit Wide Match Field
- Samples Available 1Q97
- Volume Pricing < \$50

Common Features:

- 160 ns Match Time
- Mask Register to "Don't Care" Selected Bits
- Depth Expansion by Cascading Multiple Devices
- 50 MHz Maximum Clock Rate
- Programmable 0 to 32 Bit Output Value
- Separate Ports for Control and Match Operations
- 150 ns Insertion Time if One of 12 Entry Queue Locations is Empty
- 10 ms Initialization Time after Fast Insertion (at Power–Up Only)
- Single 3.3 V \pm 5% Supply
- IEEE Standard 1149.1 Test Port (JTAG)
- 100 Pin TQFP Package

For additional information call 512–933–SRAM, or your local Motorola sales representative. FAX (512) 933–6809

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