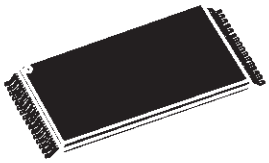
M68Z128

5V, 1 Mbit (128Kb x8) Low Power SRAM with Output Enable

DATA BRIEFING

- ULTRA LOW DATA RETENTION CURRENT
  - 10nA (typical)
  - 1.0µA (max)
- OPERATION VOLTAGE: 5V ±10%
- 128Kb x 8 VERY FAST SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIMES: 55ns
- LOW V_{CC} DATA RETENTION: 2V
- TRI-STATE COMMON I/O
- LOW ACTIVE and STANDBY POWER
- AUTOMATIC POWER-DOWN WHEN DESELECTED



TSOP32 (N)
(8 x 20mm)

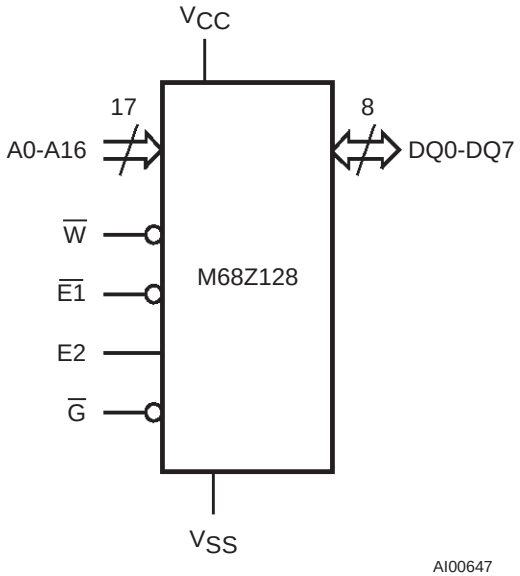
DESCRIPTION

The M68Z128 is a 1 Mbit (1,048,576 bit) CMOS SRAM, organized as 131,072 words by 8 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ±10% supply, and all inputs and outputs are TTL compatible.

This device has an automatic power-down feature, reducing the power consumption by over 99% when deselected.

The M68Z128 is available in TSOP32 (8 x 20mm) package.

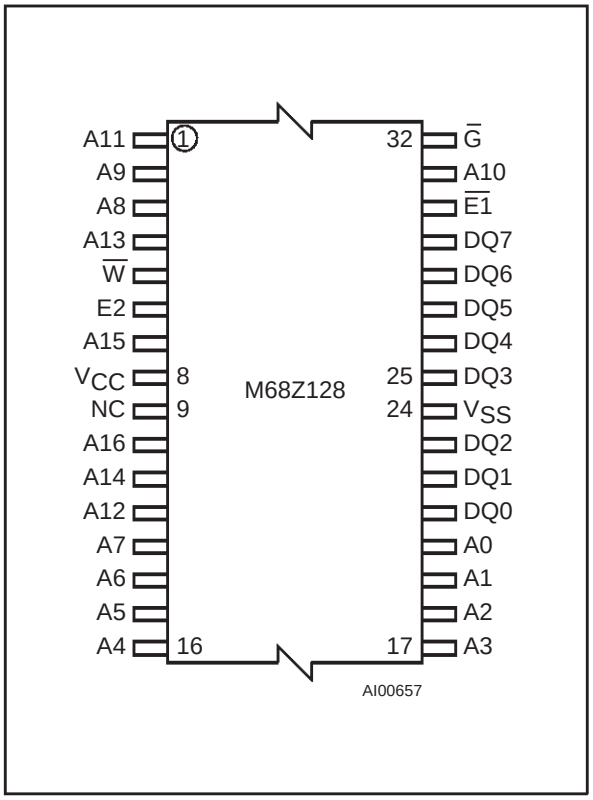
Logic Diagram



Signal Names

A0-A16	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage

TSOP Pin Connections



Ordering Information Scheme

For a list of available options or for further information on any aspect of this device, please contact the ST Microelectronics Sales Office nearest to you.

Example: M68Z128 -55 N 1

Speed

-55 55ns

Package

N TSOP32
(8 x 20mm)

Temp. Range

1 0 to 70 °C