MCM67T316

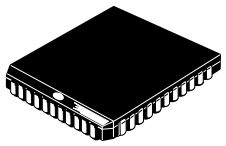
8K x 16 Bit Synchronous Cache Tag RAM

The MCM67T316 is a 131,072 bit synchronous static random access memory organized as 8,192 words of 16 bits, fabricated using Motorola's high–performance silicon–gate BiCMOS technology. Each word contains a 15–bit address tag and a valid bit.

The MCM67T316 compares the address tag stored in the RAM with the current input data. The result is either an active high MATCH level for a cache hit, or a low level for a cache miss. The valid bit is used to qualify a cache hit or miss. The entire tag memory can be invalidated by resetting all the valid bits. This is accomplished by holding the $\overline{\text{INVAL}}$ pin low for four consecutive cycles.

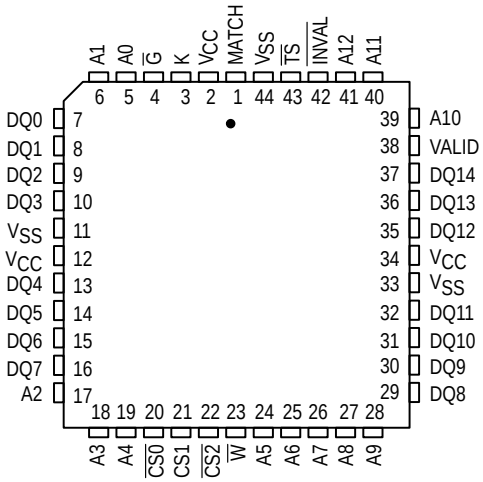
The MCM67T316 is available in a 44 pin PLCC package.

- 8K x 16 Fast Access Static Memory Array
- Single 5 V ± 10% Power Supply
- Fast Match Time: 10/12 ns Max
- Fast Clock Cycle Time: 15/25 ns Min
- Registered Address, Data, and Control Inputs
- Valid Bit on Each Word to Qualify a Cache Hit/Miss
- Four Cycles to Invalidate the Entire Tag Memory
- Cascadable to Two Cache Tags with No External Logic



FN PACKAGE
44–LEAD PLCC
CASE 777–02

PIN ASSIGNMENTS



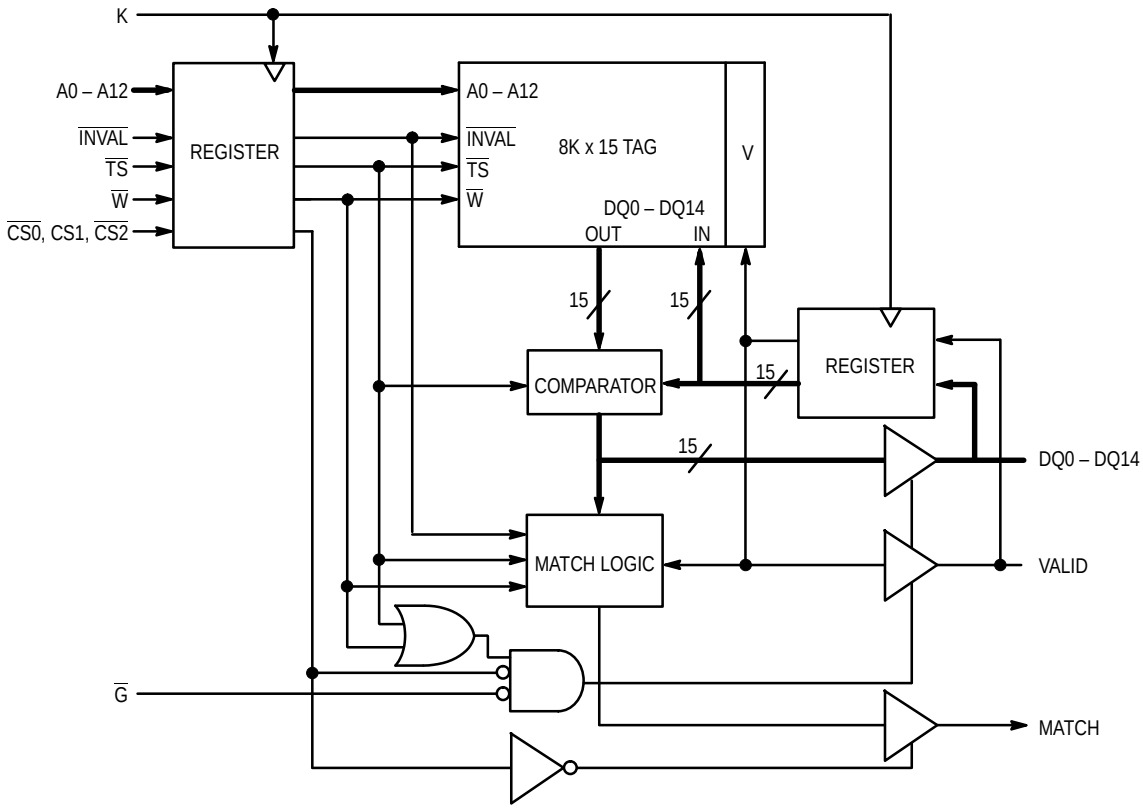
PIN NAMES

A0 – A12	Tag Address Inputs
K	Clock Input
$\overline{\text{TS}}$	Tag Select Input
$\overline{\text{W}}$	Tag Write Enable Input
VALID	Valid Bit Input/Output
$\overline{\text{INVAL}}$	Tag Invalidate Input
MATCH	Cache Match Output
$\overline{\text{G}}$	Output Enable Input
$\overline{\text{CS0}}$, CS1, $\overline{\text{CS2}}$	Chip Select Input
DQ0 – DQ14	Data Input/Outputs
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

REV 1
5/95

BLOCK DIAGRAM



TRUTH TABLE (See Notes)

W	TS	G	CS	INVAL	K	Mode	Supply Current	DQ0 – DQ14 Status	VALID Status	MATCH Status
X	H	L	T	H	L–H	Not Allowed	I_{CC}	Compare Out	Data Out	Data Out
X	H	H	T	H	L–H	Tag Compare	I_{CC}	Data In	High–Z	Data Out
H	L	L	T	H	L–H	Tag Read	I_{CC}	Data Out	Data Out	H
H	L	H	T	H	L–H	Tag Read	I_{CC}	High–Z	High–Z	H
L	L	L	T	H	L–H	Not Allowed	I_{CC}	High–Z	High–Z	H
L	L	H	T	H	L–H	Tag Write	I_{CC}	Data In	Data In	H
X	X	X	F	H	L–H	Chip Deselected	I_{SB}	High–Z	High–Z	High–Z
X	X	X	X	L	4 cycle	Invalidate Memory	I_{INV}	—	L	L

NOTES:
1. X means don't care, T means selected, F means deselected, and L–H means low to high transition.
2. All inputs except G must meet setup and hold times for low–to–high transition of clock (K).

PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
5, 6, 17, 18, 19, 24, 25, 26, 27, 28, 39, 40, 41	A0 – A12	Input	ADDRESS – Registered on the rising clock edge. The 13 address input pins are used to select one of the 8,192 tag entries.
3	K	Input	CLOCK – The clock input pin accepts a minimum 5 ns clock high or clock low pulse at a minimum 15 ns clock cycle. All inputs except Output Enable are synchronous and controlled by the clock.
43	$\overline{TS}$	Input	TAG SELECT – Registered on rising clock edge, $\overline{TS}$ is active low. When this pin is asserted, the device is in tag access mode, where the memory can be modified. When this pin is high, the device is in tag compare mode. In this mode, the tag memory is used for address comparison only and cannot be modified.
23	$\overline{W}$	Input	TAG WRITE ENABLE – Registered on the rising clock edge, $\overline{W}$ is active low. When this pin is asserted in tag access mode ($\overline{TS}$ = 0), the device will write the data on DQ0 – DQ14 to memory. Set $\overline{W}$ high in the tag access mode to read the contents of the memory. This input is ignored in tag compare mode ($\overline{TS}$ = 1).
38	VALID	I/O	VALID BIT – Registered on the rising clock edge. This pin reflects the valid bit in tag compare mode and tag read mode. In tag access write mode, data on this pin is stored in the valid bit. If $\overline{INVAL}$ is asserted, VALID will be forced low. This pin will be three–stated if either the output is disabled ($\overline{G}$ = 1) or the device is deselected.
42	$\overline{INVAL}$	Input	TAG INVALIDATE – Registered on the rising clock edge, $\overline{INVAL}$ is active low. Assert this pin to set all valid bits low, which invalidates the entire tag memory. The tag memory can be invalidated even when deselected. For invalidation to complete, the $\overline{INVAL}$ pin must be asserted for four rising clock edges. The $\overline{INVAL}$ pin must be asserted at power–up to ensure that the valid bits for all address tags are set low.
1	MATCH	Output	TAG MATCH – In the tag compare mode ($\overline{TS}$ = 1), a high at this output indicates a cache hit, and a low indicates a cache miss. In the tag access mode ($\overline{TS}$ = 0), this output remains high, except when $\overline{INVAL}$ is asserted, which drives the MATCH output low. MATCH can be three–stated by deselecting the part, but $\overline{G}$ has no effect on the MATCH output.
4	$\overline{G}$	Input	OUTPUT ENABLE – Asynchronous pin, active low. When this pin is set high, the data pin (DQ0 – DQ14) and the VALID pin will be three–stated. The $\overline{G}$ input must be asserted to use VALID pin and data pins (DQ0 – DQ14) as outputs.
20, 22	$\overline{CS0}$, $\overline{CS2}$	Input	CHIP SELECT – Registered on the rising clock edge, $\overline{CS0}$ and $\overline{CS2}$ are active low. To enable this device, $\overline{CS0}$, $\overline{CS2}$ must be set low and CS1 set high. Otherwise, the device will be disabled, and all outputs will be three–stated.
21	CS1	Input	CHIP SELECT – Registered on the rising clock edge, CS1 is active high. To enable this device, $\overline{CS0}$, $\overline{CS2}$ must be set low and CS1 set high. Otherwise, the device will be disabled, and all outputs will be three–stated.
7, 8, 9, 10, 13, 14, 15, 16, 29, 30, 31, 32, 35, 36, 37	DQ0 – DQ14	I/O	DQ pins are registered on the rising clock edge. In tag access mode ($\overline{TS}$ = 0), data in the tag memory can be modified using these pins. In tag compare mode ($\overline{TS}$ = 1), the data is compared to the tag word specified by the address. If $\overline{INVAL}$ is asserted these pins go into an unknown state. These pins will be three–stated if either the outputs are disabled ($\overline{G}$ = 1) or the device is deselected.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL}(min) = – 3.0 V ac (pulse width ≤ 10 ns).

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current (CS = Selected, $\overline{G}$ = V_{IH}, I_{out} = 0 mA, All inputs = V_{IL} or V_{IH}, V_{IL} = 0 V, and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min) MCM67T316–10 MCM67T316–12	I_{CCA}	 — —	 — —	 275 250	mA
AC Supply Current ($\overline{INVAL}$ = V_{IL} for four cycles, I_{out} = 0 mA, All inputs = V_{IL} or V_{IH},V_{IL} = 0 V, and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min) MCM67T316–10 MCM67T316–12	I_{INV}	 — —	 — —	 305 280	mA
AC Standby Current (CS = Deselected, All inputs = V_{IL} or V_{IH}, V_{IL} = 0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB}	—	—	50	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	8	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

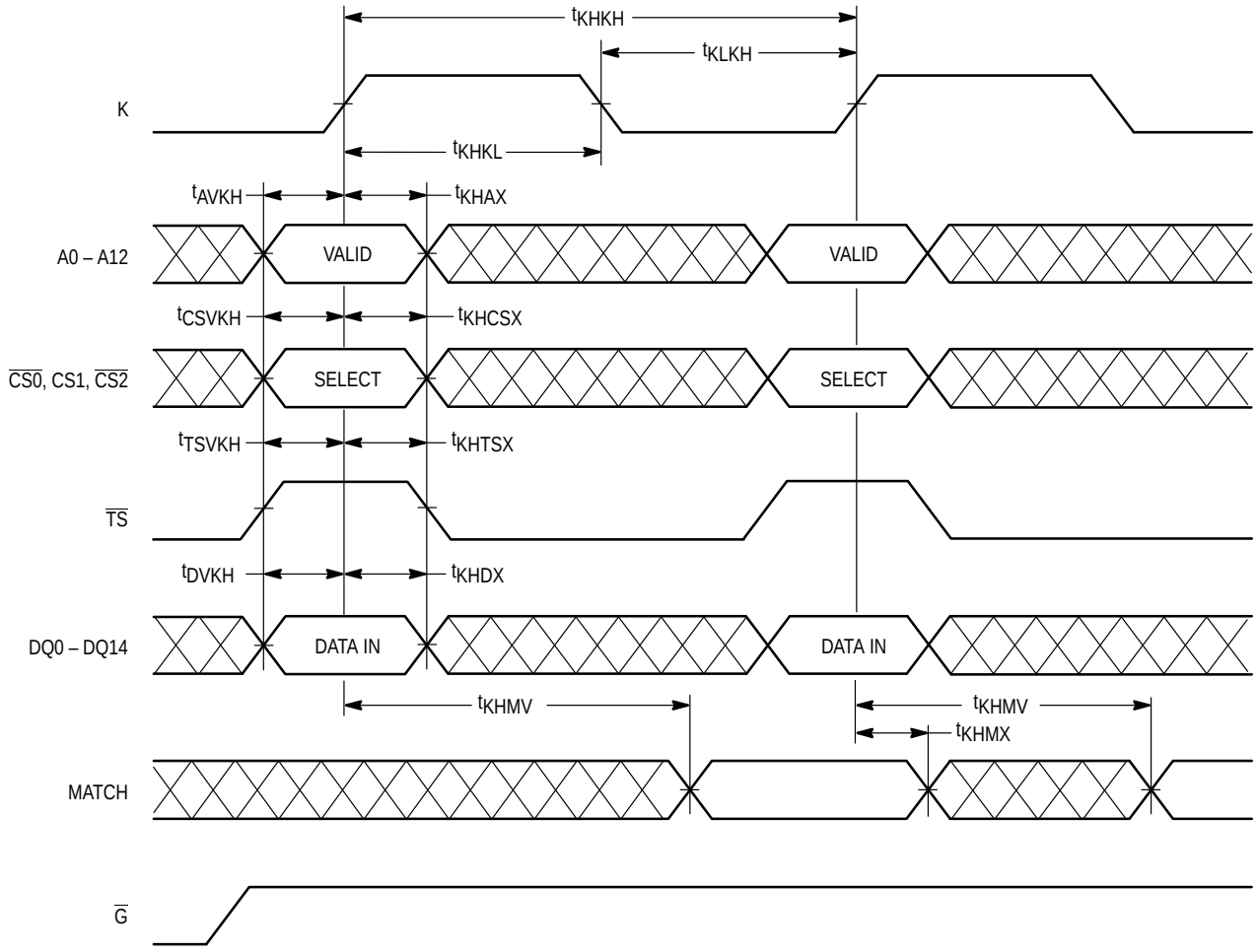
Output Measurement Timing Level . . . . . 1.5 V
Output Load . . . . . 50 Ohm Transmission Line

TAG COMPARE, READ, AND WRITE CYCLE TIMING (See Notes 1 and 2)

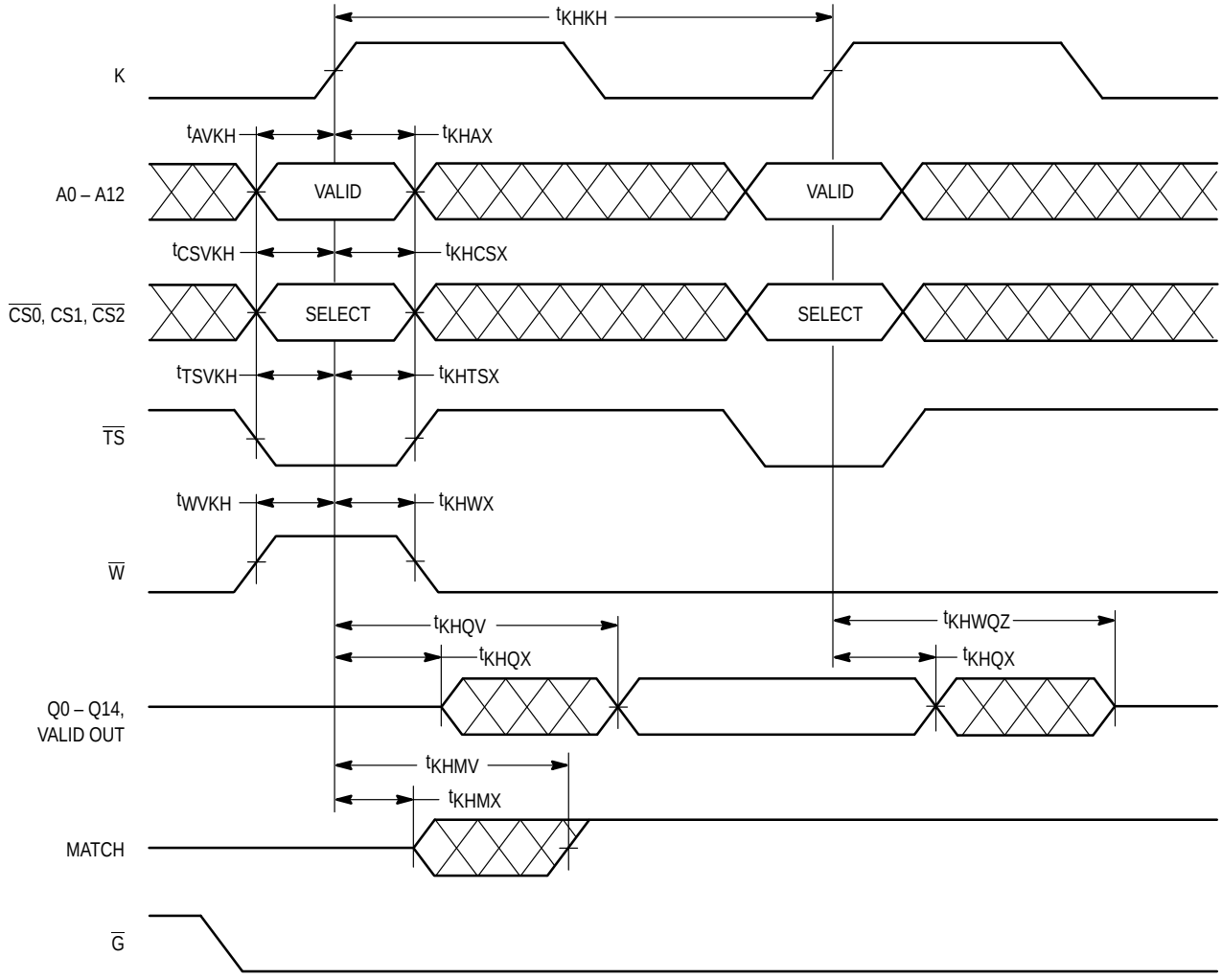
Parameter	Symbol	MCM67T316–10		MCM67T316–12		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	25	—	ns	
Clock High Time	t_{KHKL}	5	—	8	—	ns	
Clock Low Time	t_{KLKH}	5	—	8	—	ns	
Clock High to MATCH Valid	t_{KHMV}	—	10	—	12	ns	
Clock High to Output Valid	t_{KHQV}	—	10	—	12	ns	
Output High to Output High–Z Due to $\overline{W}$	t_{KHWQZ}	—	8	—	8	ns	
Output High to Output High–Z	t_{KHQZ}	—	8	—	8	ns	
Output High to Output Change	t_{KHQX}	3	—	3	—	ns	
Output Enable Low to Output Valid	t_{GLQV}	—	8	—	8	ns	
Output Enable Low to Output Active	t_{GLQX}	3	—	3	—	ns	
Output Enable High to Output High–Z	t_{GHQZ}	—	8	—	8	ns	
Setup Times: Address Write Tag Select Invalid Chip Select Data In	t_{AVKH} t_{WVKH} t_{TSVKH} t_{IVVKH} t_{CSVKH} t_{DVKH}	3	—	3	—	ns	3
Hold Times: Address Write Tag Select Invalid Chip Select Data In	t_{KHAX} t_{KHWX} t_{KHTSX} t_{KHIVX} t_{KHCSX} t_{KHDX}	1	—	3	—	ns	3
Clock High to MATCH Active	t_{KHMX}	3	—	3	—	ns	
Clock High to MATCH Low After $\overline{INVAL}$ Low	t_{KHML}	—	8	—	8	ns	
Clock High to VALID Low After $\overline{INVAL}$ Low	t_{KHVL}	—	8	—	8	ns	

NOTES:
1. All read and write cycles are referenced from K.
2. Valid data from Clock High will be the data stored at the address or the last valid read cycle.
3. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of clock when the chip is selected. Chip enable must be valid at each rising edge of clock for the device to remain enabled.

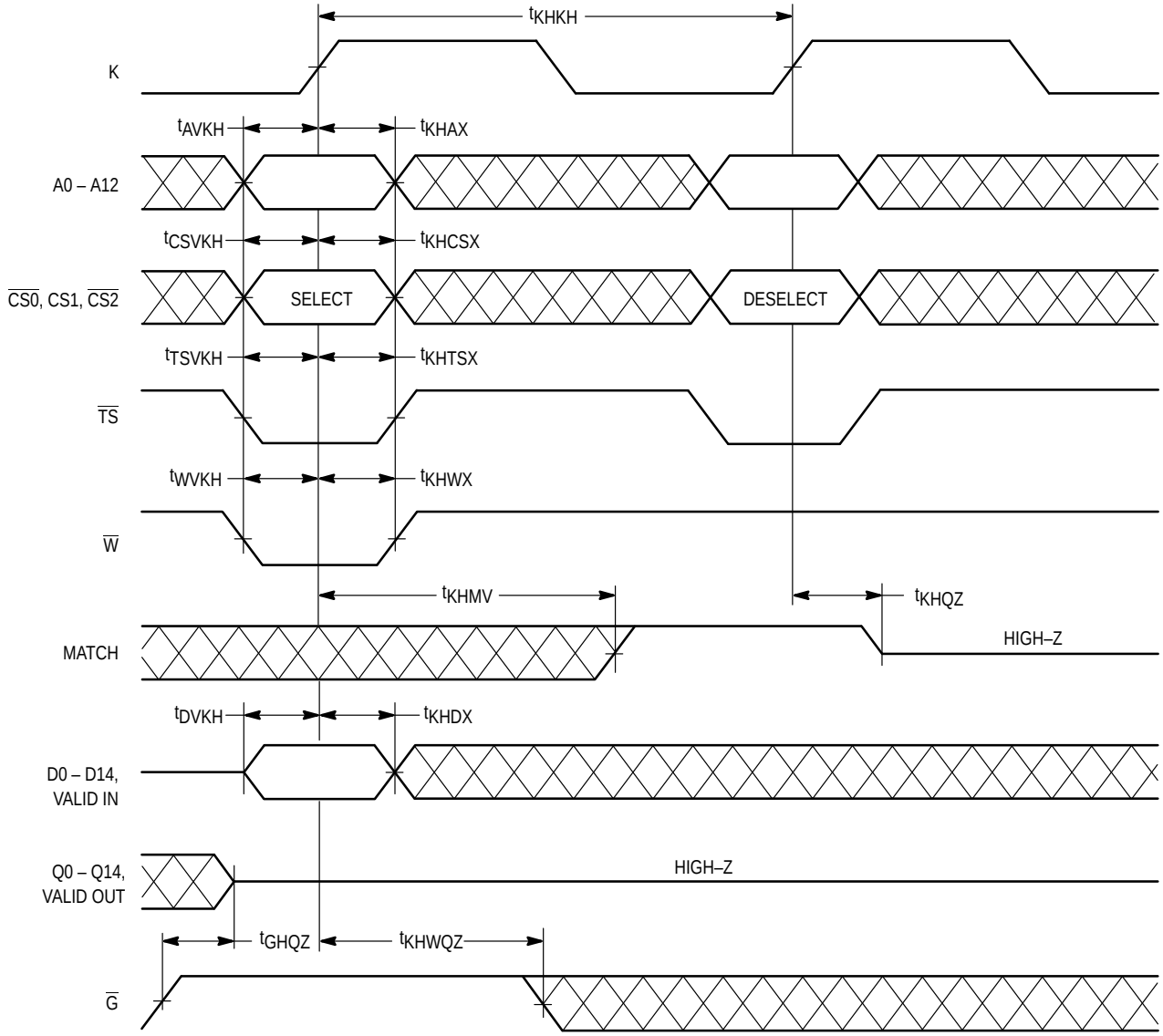
TAG COMPARE CYCLE



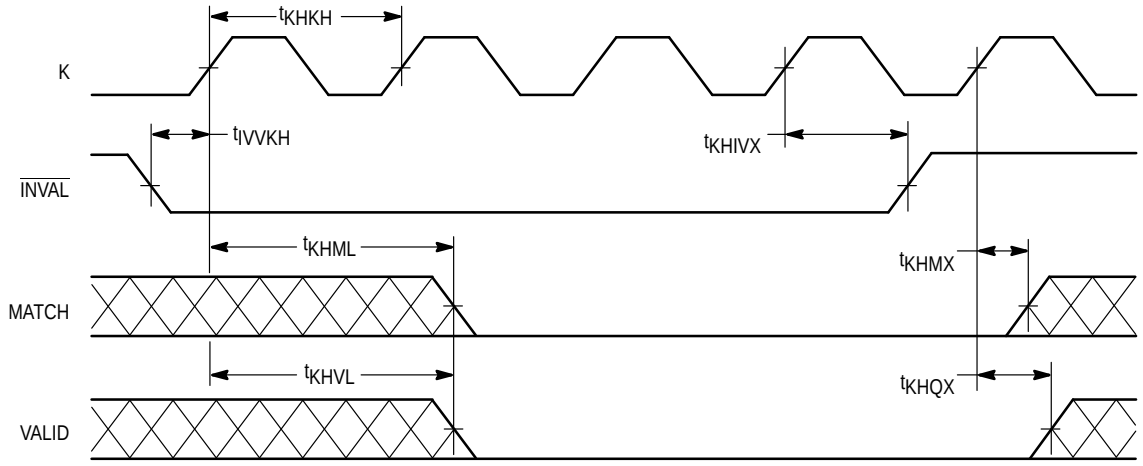
READ CYCLE


tKHKH
K
tAVKH
tKHAX
A0 – A12
VALID
VALID
tCSVKH
tKHCSX
CS0, CS1, CS2
SELECT
SELECT
tTSVKH
tKHTSX
TS
tWVKH
tKHWX
W
tKHQV
tKHQX
tKHWQZ
tKHQX
Q0 – Q14,
VALID OUT
tKHMV
tKHMX
MATCH
G

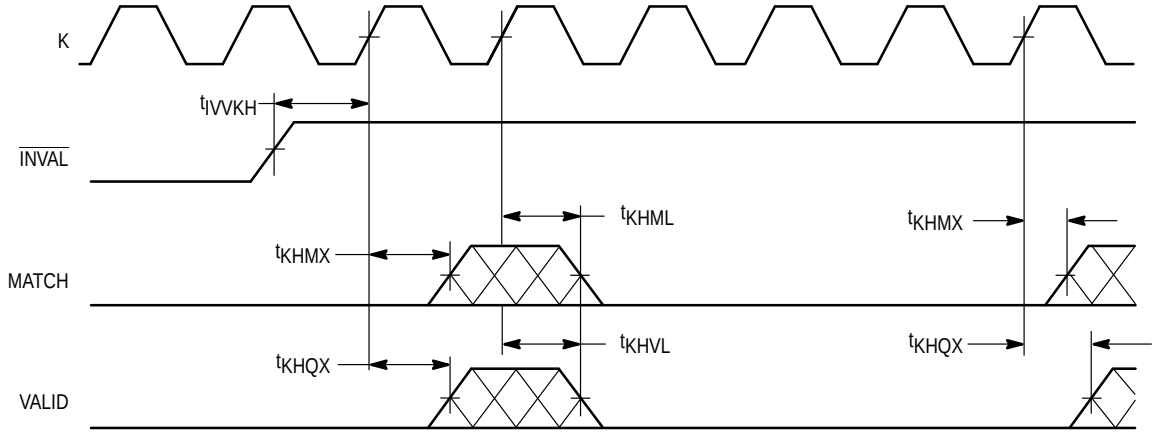
WRITE CYCLES



MEMORY INVALIDATION CYCLE



AT POWER–UP



NOTE: The first low to high transition of $\overline{\text{INVAL}}$ after power–up will initiate an invalidation cycle. All subsequent low to high transition will end invalidation cycles.

ORDERING INFORMATION
(Order by Full Part Number)

MCM 67T316 FN XX

Motorola Memory Prefix

Part Number

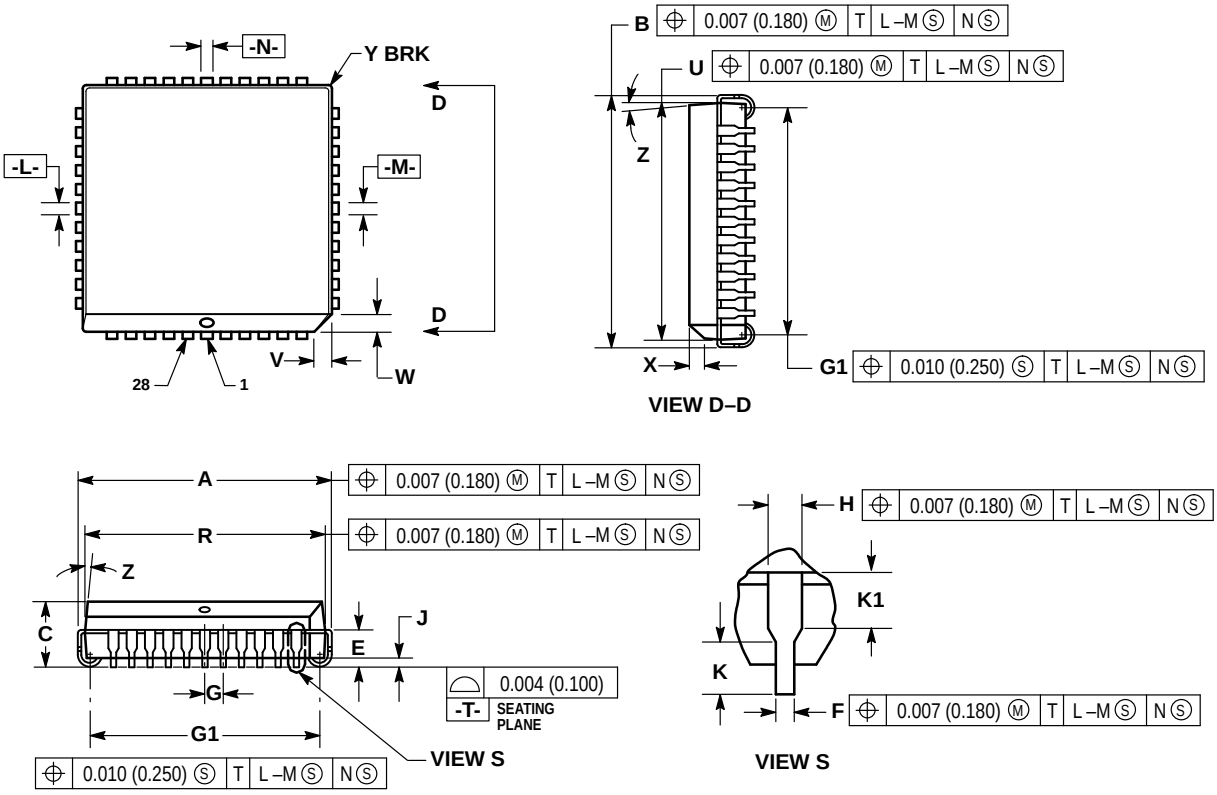
Speed (10 = 10 ns,12 = 12 ns)

Package (FN = PLCC)

Full Part Number — MCM67T316FN10
MCM67T316FN12

PACKAGE DIMENSIONS

FN PACKAGE
44–LEAD PLCC
CASE 777–02



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.610	0.630	15.50	16.00
K1	0.040	—	1.02	—

Literature Distribution Centers:
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
JAPAN: Nippon Motorola Ltd.; 4–32–1, Nishi–Gotanda, Shinagawa–ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.