MCM67Q804

256K x 4 Bit Separate I/O Synchronous Fast Static RAM

The MCM67Q804 is a 1,048,576 bit static random access memory, organized as 262,144 x 4 bits. This device is fabricated using Motorola's high–performance silicon–gate BiCMOS technology. It features separate TTL input and output buffers, which are fully I/O compatible at 3.3 V, and incorporates input and output registers on board with high speed SRAM. It also features transparent–write and data pass–through capabilities.

The synchronous design allows for precise cycle control with the use of an external single clock (K). The Addresses (A0 – A17), Data Input (D0 – D3), Data Output (Q0 – Q3), Write–Enable ($\overline{W}$), Chip–Enable ($\overline{E}$), and Output–Enable ($\overline{G}$), are registered in on the rising edge of Clock (K).

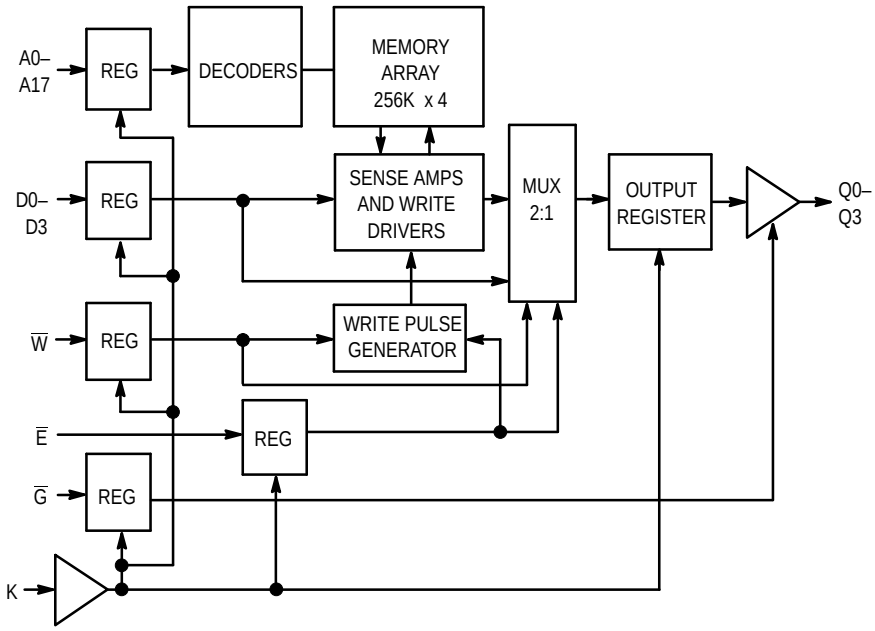
The control pins ($\overline{E}$, $\overline{W}$, $\overline{G}$) function differently in comparison to most synchronous SRAMs. This device will not deselect with $\overline{E}$ high. The RAM remains active at all times. If $\overline{E}$ is registered high, the output pins (Q0–Q8) will be driven if $\overline{G}$ is registered low. The Transparent–Write feature allows the output data to track the input data. $\overline{E}$, $\overline{G}$, and $\overline{W}$ must be asserted to perform a Transparent Write (Write and Pass–Through). The input data is available at the ouputs on the next rising edge of clock (K).

The pass–through function is always enabled. $\overline{E}$ high disables the write to the clock (K). only a clocked $\overline{G}$ high will three–state the outputs.

This device is available in a 400 mil, 36–lead surface–mount SOJ package.

- Single 5 V ± 5% Power Supply
- Fast Cycle Times: 10/12 ns Max
- Single Clock Operation
- TTL Input and Output Levels (3.3 V I/O Compatible)
- Address, Data Input, $\overline{E}$, $\overline{W}$, $\overline{G}$, Registers on Chip
- 100 MHz Maximum Clock Cycle Time
- Self Timed Write
- Separate Data Input and Output Pins
- Transparent–Write and Pass–Through
- High Output Drive Capability: 50 pF/Output at Rated Access Time

BLOCK DIAGRAM



REV 2
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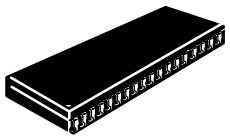
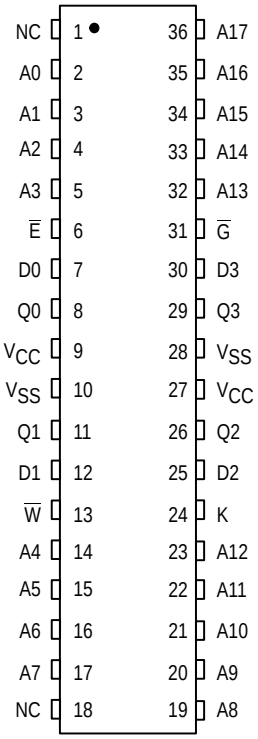


WJ PACKAGE
400 MIL SOJ
CASE 893–01

PIN ASSIGNMENT



PIN NAMES

A0 – A17	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0 – D3	Data Inputs
Q0 – Q3	Data Outputs
K	Clock Input
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

TRUTH TABLE

$\overline{E}$ (t_n)	$\overline{W}$ (t_n)	$\overline{G}$ (t_{n+1})	Mode	D0 – D3	Q0 – Q3 (t_{n+1})	V_{CC} Current
L	L	L	Write and Pass Thru	Valid	D0 – D3 (t_n)	I_{CC}
		H	Write	Valid	High–Z	I_{CC}
H	L	L	Pass Thru	Valid	D0 – D3 (t_n)	I_{CC}
		H	NOP	Don't Care	High–Z	I_{CC}
X	H	L	Read	Don't Care	Q_{out} (t_n)	I_{CC}
		H	Read	Don't Care	High–Z	I_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This is a synchronous device. All synchronous inputs must meet specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)		V_{CC}	4.75	5.25	V
Input High Voltage		V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage		V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	MCM67Q804–10 ns MCM67Q804–12 ns	I_{CCA}	— —	180 170	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	3.3	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance	C_{in}	6	pF
Output Capacitance	C_{out}	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67Q804–10		MCM67Q804–12		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12	—	ns	1
Clock Access Time	t_{KHQV}	—	5	—	6	ns	2
Clock Low Pulse Width	t_{KLKH}	4	—	4	—	ns	
Clock High Pulse Width	t_{KHKL}	4	—	4	—	ns	
Clock High to Data Output Invalid	t_{KHQX}	2	—	2	—	ns	
Clock High to Data Output High–Z	t_{KHQZ}	—	5	—	6	ns	
Setup Times: A $\overline{W}$ $\overline{E}$ $\overline{G}$ D0 – D3	t_{AVKH} t_{WVKH} t_{EVKH} t_{GVKH} t_{DVKH}	2	—	2	—	ns	3
Hold Times: A $\overline{W}$ $\overline{E}$ $\overline{G}$ D0 – D3	t_{KHAX} t_{KHWX} t_{KHEX} t_{KHGX} t_{KHDX}	1	—	1	—	ns	3

NOTES:
1. All read and write cycles are referenced from K.
2. Valid data from Clock High will be the data stored at the address or the last valid read cycle.
3. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

AC SPEC LOADS

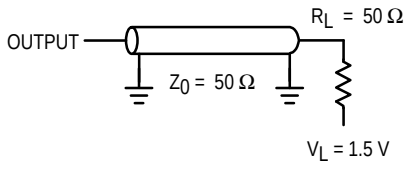


Figure 1A

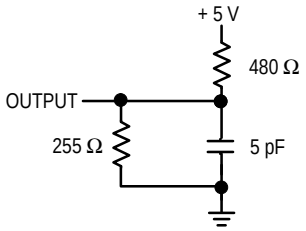
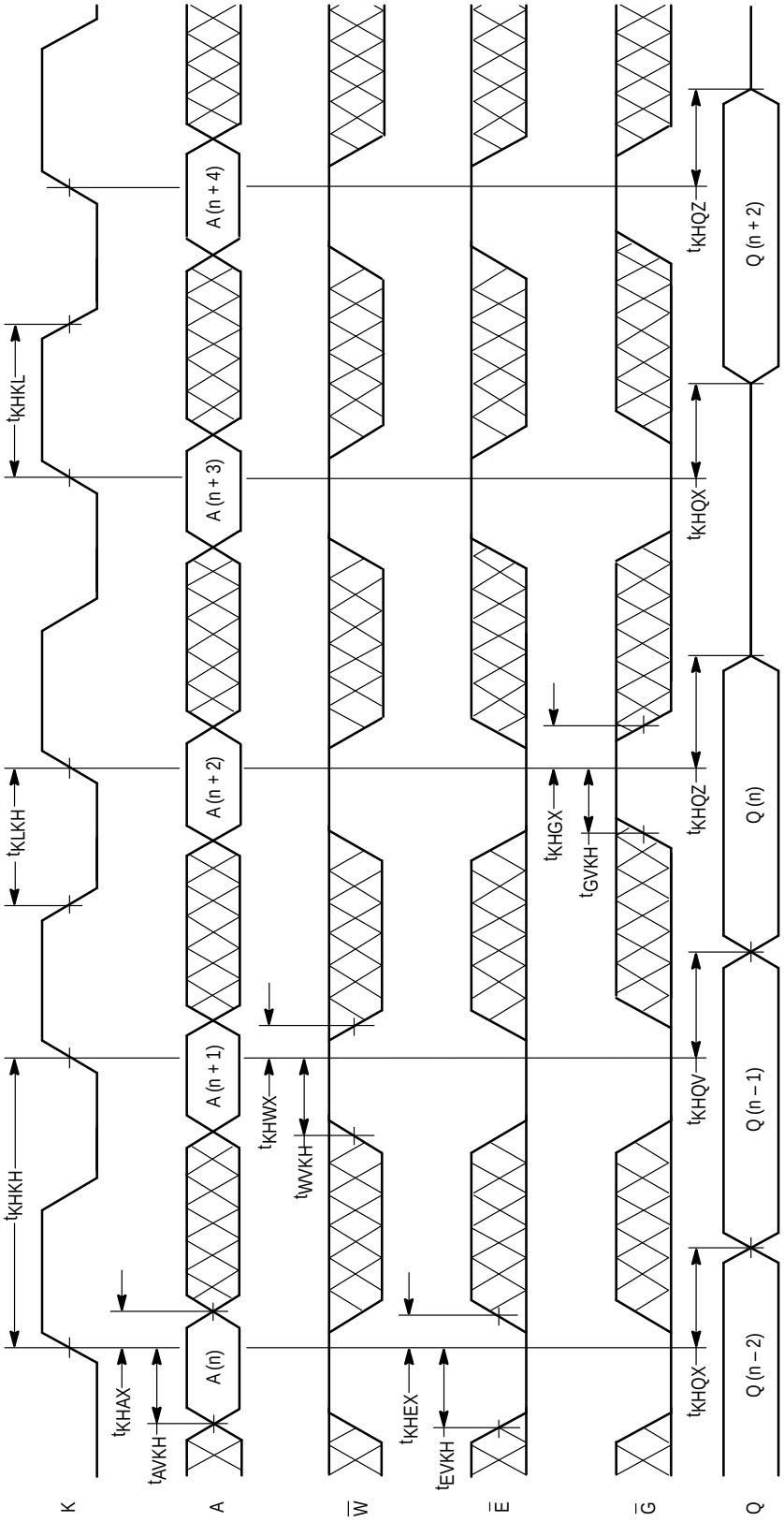
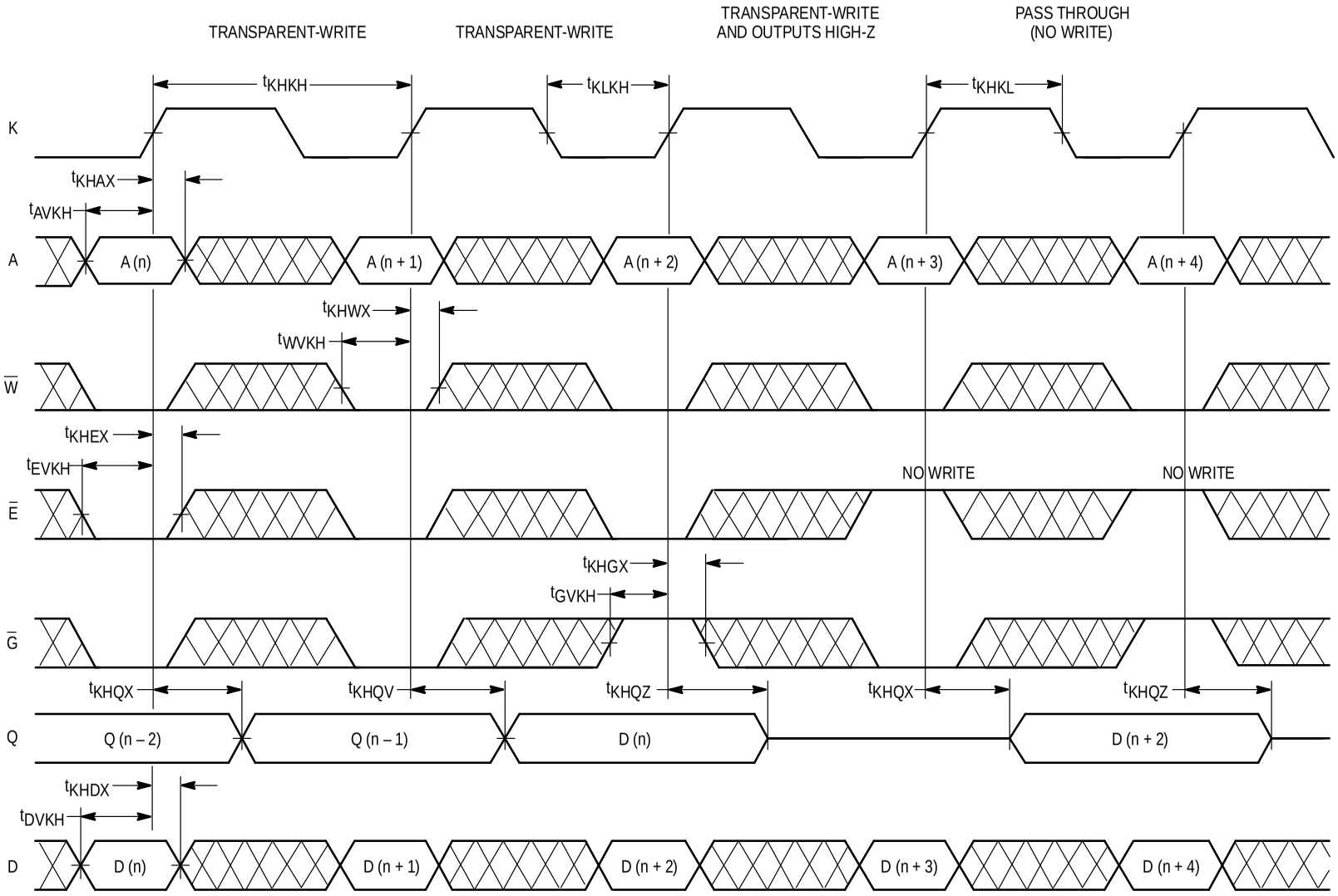


Figure 1B

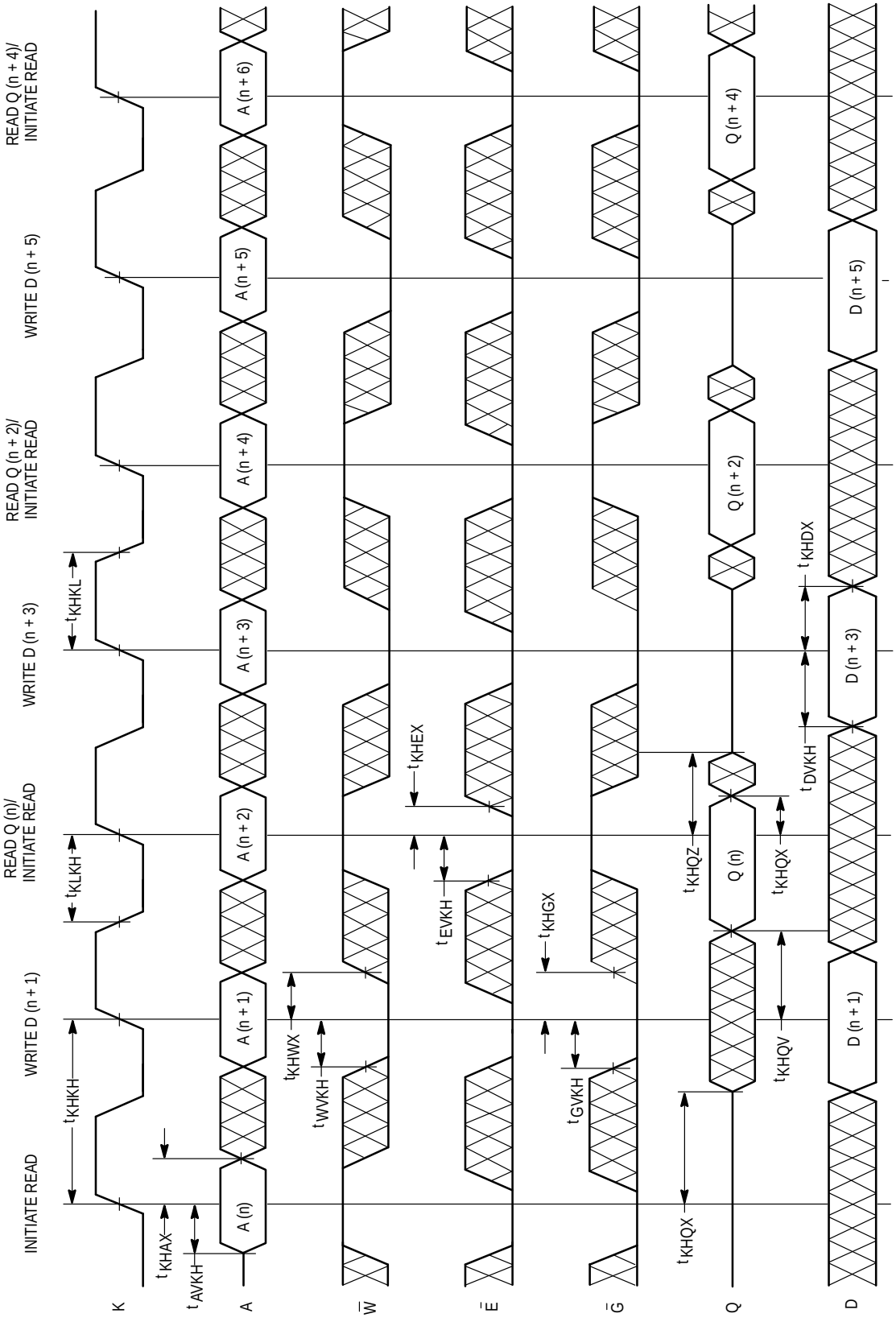
READ CYCLE TIMING



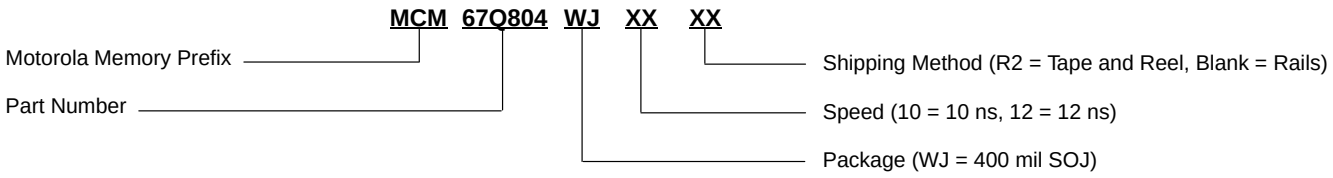
TRANSPARENT WRITE AND PASS–THROUGH CYCLE TIMING



COMBINATION READ/WRITE CYCLE TIMING



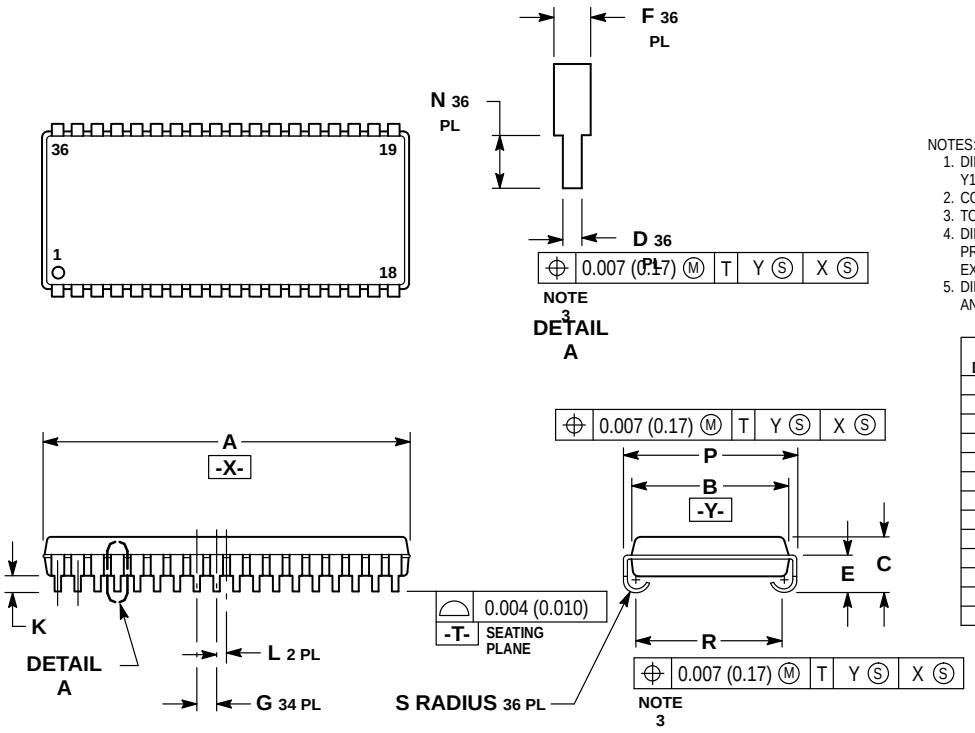
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM67Q804WJ10 MCM67Q804WJ12
MCM67Q804WJ10R2 MCM67Q804WJ12R2

PACKAGE DIMENSIONS

WJ PACKAGE
400 MIL SOJ
CASE 893–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TO BE DETERMINED AT PLANE -T-.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.006 (0.15) PER SIDE.
5. DIMENSION A AND B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.920	0.930	23.37	23.62
B	0.395	0.405	10.04	10.28
C	0.128	0.148	3.26	3.75
D	0.016	0.020	0.41	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BASIC		1.27 BASIC	
K	0.035	0.045	0.89	1.14
L	0.025 BASIC		0.64 BASIC	
N	0.030	0.045	0.77	1.14
P	0.435	0.445	11.05	11.30
R	0.365	0.375	9.28	9.52
S	0.030	0.040	0.77	1.01

Literature Distribution Centers:
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
JAPAN: Nippon Motorola Ltd.; 4–32–1, Nishi–Gotanda, Shinagawa–ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.