PRELIMINARY Notice: This is not a final specification Notice: This is not a final specification. Some parametric limits are subject to char

M66272FP

LCD CONTROLLER with VRAM

DESCRIPTION

The M66272FP is a graphic display-only controller for dot matrix type STN-LCD which is used widely for OA equipment, PDA, amusement equipment, etc.

It is capable of displaying six types of LCD by combining the panel configuration(single or dual scan), LCD display function(binary or gray scale), LCD display data bus width(4 or 8 bit).

Panel configuration	Binary/ gray scale	LCD display data	Displayable LCD size
Single scan	Binary	4bit	Equivalent to C40 x 240
		8bit	Equivalent to 640 x 240
	Gray scale	4bit	Equivalent to 320 x 240
		8bit	
Dual scan	Binary	4bit	Equivalent to 320 x 240 x 2 screens
	Gray scale	4bit	Equivalent to 320 x 120 x 2 screens

The M66272FP can support the reflective color type LCD (ECB : Electrically Controlled Birefringence).

The IC has a built-in 19200-byte VRAM as a display data memory. All of the VRAM addresses are externally opened. Direct addressing of display data can be performed from MPU, thus display data processing such as drawing can be efficiently carried out.

The built-in arbiter circuit(cycle steal system) which gives priority to display access allows timing-free access from MPU to VRAM, preventing display screen distortion.

The IC provides has a function for LCD module built-in system by lessening connect pins between the MPU and the IC.

FEATURES

- Display memory
 - Built-in 19200-byte(153.6-Kbit) VRAM(Equivalent to 320 x 240 dots x 2 screens)
 - All addresses of built-in VRAM are externally opened.

- Displayable LCD
 - Binary display Monochrome STN-LCD of up to 153600 dots(equivalent to 1/2 VGA)
- 4 gray scale display
 Monochrome STN-LCD of up to 76800 dots(equivalent to 1/4
- Monochrome SIN-LCD of up to 76800 dots(equivalent to 1/4 VGA)

Reflective color STN-LCD of up to 76800 dots (equivalent to 1/4 VGA)

- Interface with MPU

 - Capability of controlling BHE or LWR/HWR at the interface with a 16-bit MPU
- Interface with LCD
- LCD display data bus is a 4-bit or 8-bit parallel output.
- 4 kinds of control signals: CP, LP, FLM and M
- Display functions
- · Graphic display only
- Binary or 4 gray scale display(gray scale palette is used to set pseudo medium 2 gray scale.)
- Reflective color(ECB) uses a gray scale function.
- · Vertical scrolling is allowed within memory range.
- Additional function for LCD module built-in system
 Capability of interfacing with two-way 8/16-bit MPU(16-bit MPU
- byte access is not allowed.) • Access from MPU to VRAM is gained via the I/O register.
- 5V or 3V single power supply

APPLICATION

- PPC/FAX operation panel, display/operation panel of other OA equipment, multifunction/public telephone
- PDA/electronic notebook/information terminal, portable terminal
- · Game, Amusements, kid's computer etc.



MITSUBISHI < DIGITAL ASSP>

PRELIMINARY Notice: This is not a final specification Notice: This is not a tinal specification. Some parametric limits are subject to change.

2

M66272FP

LCD CONTROLLER with VRAM





PRELIMINARY Notice: This is not a final specification. Some parametric limits are subject to change.

M66272FP

LCD CONTROLLER with VRAM

PIN DESCRIPTIONS

P-15:0 input MPU data bus Output MPU data bus Output MPU address but MPU address bu	Item	Pin name	Input/ Output	Function	Number of pins
NPU Numeral solution is bits MPU, use Ar-14:00- with measure is a solution is of the MPU, use Ar-14:00- with measure is a solution is of the MPU, use Ar-14:00- with MPU and here is pained. 15 IOCS Input When solution is of the MPU, use Ar-14:00- with MPU and here is pained. 1 IOCS Input Chip select input of control register. 1 INCS Input Chip select input of control register. 1 INCS Input Chip select input of control register. 1 INCS Input Chip select input of control register. 1 INCS Input Chip select input of version and the meanal VRAM. Assign to memory space of MPU. 1 INVR Input Conv-Write strobe input When this pin is 'L', write data to the internal control register or VRAM. 1 MPUCL Input Read strobe input When this pin is 'L', write data to the internal control register or VRAM. 1 MPUCL Input Read strobe input When this pin is 'L', write data from the internal control register or VRAM. 1 MPUCL Input Read strobe input When this pin is 'L', write data from MPU. 1 RESET Input		D<15:0>	· ·		16
IOUS Impu When this pin is "L", select the internal control register. Assign to I/O space of MPU. 1 MCS Input Chip select input of VRAM 1 HWR Input Chip select input of VRAM 1 HWR Input High-Write strobe input 1 INVE Input High-Write strobe input 1 WR then this pin is "L", write data to the internal control register or VRAM. 1 INVE Input When this pin is "L", write data to the internal control register or VRAM. 1 INVE Input Set ad strobe input 1 MPUSEL Input Set ad strobe input 1 MPUSEL Input Set reset signal of MPU. When this pin is "L", write data to the internal control register or VRAM. 1 RESET Input Reset input Set reset signal of MPU. 1 RESET Input Reset input 1 1 SWAP Input Set reset signal of MPU. 1 1 WAT Output Set reset signal of MPU. 1 1 SWAP		A<14:0>	Input	When selecting 8-bit MPU, use A<14:0>. When selecting 16-bit MPU, use A<14:1> as a address bus. By combining A<0> and BHE, access to intern VRAM can be gained. When driving two screens (dual scan mode), notice that the allowable setup range of VRAM address restricted. Use A<7:0> for selecting address of control register.	
MCS Imput When this pin is "L," select the internal VRAM. Assign to memory space of MPU. 1 HWR Input High-Wite strobe input 1 WR Input When this pin is "L," write data to the internal CMAM. HWR is valid only in using 16-bit MPU 1 WR Input When this pin is "L," write data to the internal control register or VRAM. 1 WRU Input When this pin is "L," write data to the internal control register or VRAM. 1 MPU Input School input 1 1 MPU Reset input Use reset signed on MPU. When this pin is "L," initialize (reset) all internal control registers and counters. 1 MPUCLk Input Reset input Use reset signed on MPU. When this pin is "L," initialize (reset) all internal control registers and counters. 1 MPUCkk Input System clock output from MPU. 1 1 Wart NPU Gock MPU Gock 1 1 WART Reset input WPU dock when using 16-bit MPU concel SWAP to "vis" to transfer VDcnOp. in order of Upper/Lower byte of NPU dock when using 16-bit MPU concel SWAP to "vis" to transfer VDcnOp. in order of Upper/Lower byte of the WPU dock when using 16-bit MPU concel SWAP to "vis" to transtor of t		IOCS	Input		
HWR Input When this pin is "L", wire data to the internal VRAM. HWR is valid only in using 16-bit MPU 1 IWR Input Controlled byte access by LWR and HWR. 1 IWR Input Low-Write strobe input When this pin is "L", wire data to the internal control register or VRAM. 1 MPU Imput Single controlled byte access by LWR and HWR. 1 MPUSEL Input Single controlled byte access by LWR and HWR. 1 MPUSEL Input Single controlled byte access by LWR and HWR. 1 MPUSEL Input Single controlled byte access by LWR and HWR. 1 MPUSEL Input Single controlled byte access by LWR and set "Voo" for 16-bit MPU. 1 INSERTION RESET Input Were setsignal of MPU. When this pin is 'L', initialize (reset) all internal control registers and control register or Vsa'. 1 BHE Input MPU clock MPU. connect WAPU to Vsa'' to transfer VD-mCb' in order of Upper/Lower byte of WPU dots bas, revealing onnect Vroo' in order of Vsa''. 1 SWAP Input Were selecting the MPU. connect WAPT to 'sa'' to transfer VD-mCb' in order of Vsa''. 1 SWAP Vsa'''''''''''''''''''''''''''''''''		MCS	Input		1
LWR Input When this pin is "L", write data to the internal control register or VRAM. 1 RD Input Read strobe input When this pin is "L", read data from the internal control register or VRAM. 1 MPUSEL Input According to MPU, set "Vss" for 8-bit MPU and set "Vob" for 16-bit MPU. 1 RESET Input Reset input Use reset signal of MPU. When this pin is "L", initialize (reset) all internal control registers and counters. 1 MPUCLK Input Reset input Use reset signal of MPU. When this pin is "L", initialize (reset) all internal control registers and counters. 1 MPUCLK Input MPU clock Input system clock output from MPU. 1 BHE Input Bus-High-Enable input This pin is valid when using 16-bit MPU controlling byte access with A<0> and BHE. 1 SWAP Input Bus swap input When selecting 16-bit MPU. connect SWAP to "Vss" to transfer VD-m.0> in order of Upper/Lower byte of MPU data bus, reversally connect to "Vss" to transfer VD-m.0> in order of Upper/Lower byte of MPU data bus, reversally connect to "Vss" to transfer VD-m.0> in order of Upper/Lower byte of Beat witch. 1 WATT Output for MPU This signal makes WATT for MPU. Change WATT to "L" at timing of falling edge of overlapping with MCS and Bo or UWR and the display data bus for LCD 1 CSE Outpu		HWR	Input	When this pin is "L", write data to the internal VRAM. HWR is valid only in using 16-bit MPU	1
MPU Interface RD Input When this pin is "L", read data from the internal control register or VRAM. 1 MPUSEL Input 8/16-bit MPU select input According to MPU, sel "Vss" for 8-bit MPU and set "Voo" for 16-bit MPU. 1 RESET Input Reset input Use reset signal of MPU. When this pin is "L", initialize (reset) all internal control registers and counters. 1 MPUCLK Input MPU clock Input system clock output from MPU. 1 BHE Input Bus-High-Enable input This pin is value when using 16-bit MPU controlling byte access with A-c0> and BHE. Connect to "Voo" to select 8-bit MPU. 1 SWAP Input Bus swap input When selecting 16-bit MPU, connect SWAP to "Vss" to transfer VD-m0> in order of Upper/Lower byte of MPU data bus, reversally connect to "Vso" in order of Lower(Upper Vste. WHE selecting 16-bit MPU. Connect To "Vss" to transfer VD-m0> is one 27.0> to access to register of 80 kitwich. 1 WAT Output Transfer MCA and is any motion when requested access. 1 WAT Output WAT for MPU. Change WAT for WAT for MPU. Change WAT for WAT is princhication with the itsing adge of MPUCIX atter internal access. 1 CSE Output State output of internal cycle steal access. 1 The VD-r.O- Output Transfer tock 1		LWR	Input		1
MPUSEL Impu AP16-bit MPU select input According to MPU, set 'Vss' for 8-bit MPU and set 'Voo'' for 16-bit MPU. 1 RESET Input Reset input Use reset signal of MPU. When this pin is "L", initialize (reset) all internal control registers and counters. 1 MPUCLK Input MPU clock Input System clock output from MPU. 1 BHE Input MPU clock Input System clock output from MPU. 1 BHE Input Bus-High-Enable input This pin is valid when using 16-bit MPU controlling byte access with A<0> and BHE. 1 Connect to "Voo' to select 8-bit MPU. Connect to "Voo' to select 8-bit MPU. 1 SWAP Input Bus-swigh-Enable input This selecting 6-bit MPU. connect SWAP to "Vss" to transfer VDe:n.0> in order of Upper/Lower byte of MPU data base. 1 WAIT Output MPU data base. NPU data base. 1 WAIT Output MPU data base. 1 1 WAIT Output Cycle Steal Enable output State output of internal cycle steal access. 1 1 VDe7-ro. Output Cycle Steal Enable output State output of internal cycle steal access. 1 1 ILCD Output	MPU	RD	Input		1
RESET Input Use reset signal of MPU. When this pin is "L", initialize (reset) all internal control registers and counters. 1 MPUCLK Input MPUCLK Input MPU cook 1 BHE Input MPU cook MPU cook 1 BHE Input Bus-High-Enable input 1 1 SWAP Input Bus-High-Enable input 1 1 SWAP Input Bus sugn input Over the selecting field MPU connect SWAP to "Vss" to transfer OpenDo in order of Upper/Lower byte of WPU besides reversally connect to "Vos" in order of Upwer/Lower byte of WPU besides reversally connect to "Vss". Even if connecting to "Vss", use D-7.0> to access to register of selecting ebit MPU, connect to "Vss". Even if connecting to "Vsc", use D-7.0> to access to register of Selecting and HWE_And return to "H" at synchronization with the rising edge of Overlapping with MCS and RD or LWR and HWU. And return to "H" at synchronization with the rising edge of MPUCLX after internal processing. (Output WAIT on the VD, Change WAIT to "L" at time of dailing edge of OP by putting 4-bit or 8-bit in parallel. The CO deside and HWE_And return to "H" at synchronization with the rising edge of OVERAMI to "L" at time display data to the transfer of display data to LCD. Take the CO display data to SID. 1 VD-7:0> Output Display data transfer of display data to LCD. Take the cloplay data of VD-0: To LCD at alling edge of CP. Take the cloplay data and the transfer of disp	-	MPUSEL	Input		1
MPUCLX Input Input system clock output from MPU. 1 BHE Input Input system clock output from MPU. 1 BHE Input Bus-High-Enable input 1 SWAP Input Bus-High-Enable input 1 SWAP Input Bus swap input When selecting 16-bit MPU, connect SWAP to "Vss" to transfer VD <n:0> in order of Upper/Lower byte of 8-bit width. 1 SWAP Input Bus swap input When selecting 8-bit MPU, connect SWAP to "Vss" to transfer VD<n:0> in order of Upper/Lower byte of 8-bit width. 1 WAIT Output War output for MPU This signal makes WAIT for MPU. Change WAIT to "L" at timing of falling edge of overlapping with MCS and PRD. And return to "H" at synchronization with her ising edge of MPUCLK after internal processing. (Output WAIT only when requested access. 1 CSE Output Cycle Steal Enable output Steal access. 1 The Vor.70> Output Transfer the LCD display data to LCD. The the display data of DV-nO> to LCD at falling edge of CP by putting 4-bit or 8-bit in parallel. The Vor.nO> output pin in use differs depending on the number of driven screens and the display mode. 1 LCD Display data torsfer clock Shit clock for the transfer of display data to LCD. Take the display data to LCD. Take the display</n:0></n:0>		RESET	Input	Reset input Use reset signal of MPU. When this pin is "L", initialize (reset) all internal control registers and	
BHE Input This pin is valid when using 16-bit MPU controlling byte access with A<0> and BHE. Connect to "Von" to select 8-bit MPU. 1 SWAP Input Bus swap input When selecting 16-bit MPU, connect SWAP to "Vss" to transfer VD-n:0- in order of Upper/Lower byte of MPU data bus, reversally connect to "Vss". Even if connecting to "Von", use D<7:0- to access to register of 8-bit width. 1 WAIT Output WAIT output for MPU. This signal makes WAIT for MPU. Change WAIT to "L" at timing of falling edge of overlapping with MCS and RD or LWR and HWR. And return to "H" at synchronization with the rising edge of MPUCLK after internal access; 1 CSE Output Cycle Steal Enable output State output of internal cycle steal access. 1 VD<7:0-		MPUCLK	Input		
SWAP Input When selecting 16-bit MPU, connect SWAP to "Vse" to transfer VD-cn:D> in order of Upper/Lower byte of MPU data bus, reversally connect to "Vob" in order of Lower/Upper byte. 1 WARIT Output When selecting 8-bit MPU, connect to "Vse". Even if connecting to "Vob", use D<7:D> to access to register of 8-bit width. 1 WAIT Output WAIT output for MPU This signal makes WAIT for MPU. Change WAIT to "L" at timing of falling edge of MPUCLX fatter internal access.) 1 CSE Output Cycle Steal Enable output State output of internal cycle steal access. 1 VD<7:D> Output Display data bus for CD Transfer the LCD display data in synchronization with a rising edge of CP by putting 4-bit or 8-bit in parallel. The VD-n:D> output in use differs depending on the number of driven screens and the display mode. 8 LCD interface Display data tartaffer olock 1 1 FLM Output Shift clock for the transfer of display data for LCD Trake the display data of VD-m:D> to LCD at falling edge of CP. 1 LCD interface Display data latch pulse This clock use both as the latch pulse of display data for LCD and the transfer of scanning signal. This clock use both as the latch pulse of display data for LCD and the transfer of scanning signal. This clock use both as the latch pulse of display data for LCD and the transfer of scanning signal. This signal for driving scanning line. This signal for driving SCD by alter		BHE	Input	This pin is valid when using 16-bit MPU controlling byte access with A<0> and \overline{BHE} .	1
Image: ward to the second se		SWAP	Input	When selecting 16-bit MPU, connect SWAP to "Vss" to transfer VD <n:0> in order of Upper/Lower byte of MPU data bus, reversally connect to "Vbb" in order of Lower/Upper byte. When selecting 8-bit MPU, connect to "Vss". Even if connecting to "Vbb", use D<7:0> to access to register of</n:0>	
CSE Output State output of internal cycle steal access. 1 VD<7:0> Output Display data bus for LCD Transfer the LCD display data in synchronization with a rising edge of CP by putting 4-bit or 8-bit in parallel. The VD=r:0> output pin in use differs depending on the number of driven screens and the display mode. 8 CP Output Display data transfer clock Shift clock for the transfer of display data to LCD. Take the display data of VD=r:0> to LCD at falling edge of CP. 1 LP Output Display data and the transfer of display data for LCD and the transfer of scanning signal. LP is output when it finishes transferring display data for LCD and the transfer of scanning signal. LP is output when it finishes transferring display data for LCD and the transfer of scanning signal. Let of display data and the transfer of scanning signal at falling edge of LP. 1 FLM Output First Line Marker signal output Output the start pulse of scanning line. This signal is "H" active, the IC for driving scanning line catches FLM at falling edge of LP. 1 M Output LCD (ON/OFF) control signal output Signal for driving LCD by alternating current. 1 LCDENB Output LCD (ON/OFF) control signal output Output data which is set at bit "0" of mode register (R1) in the control register. This signal can be used for controlling the LCD power supply, because LCDENB is set to "L" by RESET. 1 Vob — Power supp		WAIT	Output	This signal makes WAIT for MPU. Change WAIT to "L" at timing of falling edge of overlapping with MCS and RD or LWR and HWR. And return to "H" at synchronization with the rising edge of MPUCLK after internal processing. (Output WAIT only when requested access from MPU to VRAM is gained during cycle steal	1
VD<7:0> Output Transfer the LCD display data in synchronization with a rising edge of CP by putting 4-bit or 8-bit in parallel. The VD <n:0> output pin in use differs depending on the number of driven screens and the display mode. 8 CP Output Display data transfer clock Shift clock for the transfer of display data to LCD. Take the display data of VD<n:0> to LCD at falling edge of CP. 1 LP Output Display data latch pulse This clock use both as the latch pulse of display data for LCD and the transfer of scanning signal. LP is output when it finishes transferring display data of LCD. Take the display data and the transfer of scanning signal at falling edge of LP. 1 FLM Output First Line Marker signal output Output the start pulse of scanning line. This signal is "H" active, the IC for driving scanning line catches FLM at falling edge of LP. 1 M Output LCD alternating signal output Signal for driving LCD by alternating current. 1 LCDENB Output LCD (ON/OFF) control signal output Signal for controlling the LCD power supply, because LCDENB is set to "L" by RESET. 1 Others Vob — Power supply pin 7</n:0></n:0>		CSE	Output		1
CP Output Shift clock for the transfer of display data to LCD. Take the display data of VD <n:0> to LCD at falling edge of CP. 1 LCD LP Output Display data latch pulse This clock use both as the latch pulse of display data of LCD and the transfer of scanning signal. LP is output when it finishes transferring display data of a line. Latch of display data and the transfer of scanning signal at falling edge of LP. 1 FLM Output First Line Marker signal output Output the start pulse of scanning line. This signal is "H" active, the IC for driving scanning line catches FLM at falling edge of LP. 1 M Output LCD alternating signal output Signal for driving LCD by alternating current. 1 LCDENB Output LCD (ON/OFF) control signal output Output data which is set at bit "0" of mode register (R1) in the control register. This signal can be used for controlling the LCD power supply, because LCDENB is set to "L" by RESET. 1 Others Vod — Power supply pin 7</n:0>		VD<7:0>	Output	Transfer the LCD display data in synchronization with a rising edge of CP by putting 4-bit or 8-bit in parallel.	8
LCD interface LP Output This clock use both as the latch pulse of display data for LCD and the transfer of scanning signal. LP is output when it finishes transferring display data of a line. Latch of display data and the transfer of scanning signal at falling edge of LP. 1 FLM Output First Line Marker signal output Output the start pulse of scanning line. This signal is "H" active, the IC for driving scanning line catches FLM at falling edge of LP. 1 M Output LCD alternating signal output Signal for driving LCD by alternating current. 1 LCDENB Output LCD (ON/OFF) control signal output Output data which is set at bit "0" of mode register (R1) in the control register. This signal can be used for controlling the LCD power supply, because LCDENB is set to "L" by RESET. 1 Others Vob — Ground 12		СР	Output	Shift clock for the transfer of display data to LCD.	1
FLM Output First Line Marker signal output Output the start pulse of scanning line. This signal is "H" active, the IC for driving scanning line catches FLM at falling edge of LP. 1 M Output LCD alternating signal output Signal for driving LCD by alternating current. 1 LCDENB Output LCD (ON/OFF) control signal output Output data which is set at bit "0" of mode register (R1) in the control register. This signal can be used for controlling the LCD power supply, because LCDENB is set to "L" by RESET. 1 Others Vod — Power supply pin 7 Others Use Ground 12			Output	This clock use both as the latch pulse of display data for LCD and the transfer of scanning signal. LP is output when it finishes transferring display data of a line.	1
M Output Signal for driving LCD by alternating current. 1 LCDENB Output LCD (ON/OFF) control signal output Output data which is set at bit "0" of mode register (R1) in the control register. This signal can be used for controlling the LCD power supply, because LCDENB is set to "L" by RESET. 1 Others Vod — Power supply pin 7 Vts — Ground 12			Output	Output the start pulse of scanning line.	1
LCDENB Output Output data which is set at bit "0" of mode register (R1) in the control register. This signal can be used for controlling the LCD power supply, because LCDENB is set to "L" by RESET. 1 Vbb Power supply pin 7 Others Vss Ground 12		М	Output		1
Others Vss — Ground 12		LCDENB	Output	Output data which is set at bit "0" of mode register (R1) in the control register. This signal can be	1
	Others	Vss N.C		Ground No connection	12 5

PRELIMINARY Notice: This is not a final specification: Some parametric limits are subject to change

LCD CONTROLLER with VRAM

OUTLINE

M66272FP is a graphic display only controller for displaying a dot matrix type STN-LCD.

• LCD display mode

It is capable of displaying six types of LCD by combining the panel configuration, binary/gray scale, LCD display data bus width.

Display mode	Panel configuration	Binary/ gray scale	LCD display data	Displayable LCD size
1	Single scan	Dimensi	4bit	Equivalent to
2		Binary	8bit	640 x 240
3		Crovesolo	4bit	Equivalent to
4		Gray scale	8bit	320 x 240
5	Dual scan	Binary	4bit	Equivalent to 320 x 240 x 2 screens
6		Gray scale	4bit	Equivalent to 320 x 240 x 2 screens

• Control register

When accessing the control register from MPU, use pins $\overline{\text{IOCS}}$, $\overline{\text{LWR}}$, $\overline{\text{RD}}$, A<7:0> and D<7:0>. (However, use D<15:0> only when 16-bit MPU controls the LCD module built-in support function.)

The IC contains the following registers as control registers.

Operation control	R1 to R11	
Supporting LCD module built-in type	R12 to 14 or R15 to 16	
Gray scale pattern table	R17 to R80	

• VRAM

This IC has a built-in 19200-byte VRAM which is equivalent to two screens of 320 x 240 dots LCD.

When accessing VRAM from MPU, use pins \overline{MCS} , \overline{HWR} , \overline{LWR} , \overline{RD} , \overline{BHE} , A<14:0> and D<15:0>.

Use of MPUSEL input can support both 8-bit MPU and 16-bit MPU.

The VRAM address settable range is restricted depending on the panel configuration, as follows.

VRAM address settable range

- ♦ When single scan mode
- A<14:0>=0000 to 4AFFH --- 19200 byte



- ♦When dual scan mode
- For the 1st screen --- A<14:0>=0000 to 257FH --- 9600 byte • For the 2nd screen --- A<14:0>=2580 to 4AFFH --- 9600 byte

0000н				
VRAM for the 1st screen				
		257Fн		
2580н				
VRAM for the 2nd screen				
		4AFFн		

• Cycle steal system

Cycle steal system is interact method of transforming display data for LCD from VRAM and accessing VRAM from MPU on the basic cycle (MAINCLK) of internal operation.

Basic timing is two clocks of MAINCLK, and assign first clock to the access from MPU to VRAM and second clock to the transfer of display data from VRAM to LCD.

In accessing VRAM from MPU, output \overrightarrow{WAIT} . Change \overrightarrow{WAIT} to "L" at the timing of the falling edge of overlapping with \overrightarrow{MCS} and \overrightarrow{RD} or \overrightarrow{LWR} / \overrightarrow{HWR} , and return to "H" at synchronizing with rising edge of MPUCLK after internal processing.

For the cycle steal system, this IC provides a cycle steal control function to improve data transfer efficiency in a line. This function gains access with the cycle steal system by taking WAIT for MPU during the display term with necessity for the display data transfer from built-in VRAM to LCD. On the other side, it does not output WAIT for keeping throughput of MPU during horizontal synchronous term (idle running term) with no necessity for the display data transfer from VRAM to LCD side.

• Output to LCD side

Dist

LCD display data VD<7:0> is output in parallel per 4 bits or 8 bits in synchronization with the rising edge of CP. Pin VD<n:0> differs depending on the display mode.

	Single	Dual scan				
	4-bit transfer	8-bit transfer	4-bit transfer			
			VD<7:4>			
	VD<3:0>	VD<7:0>	VD<3:0>			
pla	y mode 13	24	56			

When display data for a line has been sent, LP outputs data in synchronization with the falling edge of MAINCLK.

The IC enables adjustment to an optimum value of the frame frequency as requested from the LCD PANEL side by adjusting pulse width of LP with the LPW register value.

FLM is output when the display data for the first line has been sent.

M output is an LCD alternating signal for driving LCD with alternating current.

M output cycles can be set in lines with the M output cycle variable register and is available to prevent LCD from deterioration.

• Gray scale display function

Gray scale display can assign 2-bit VRAM data to a picture element of LCD display to show the display density at four levels.

Gray scale display pattern tables 0 and 1 (4 x 4 matrix x 16 patterns x 2 medium gray scale), consisting of SRAM of 64 bytes in total, can set any gray scale display pattern.

Application to reflective color type LCD

The above gradation display function is available to control about four display colors on the reflective color type LCD with ECB (Electrically Controlled Birefringence).