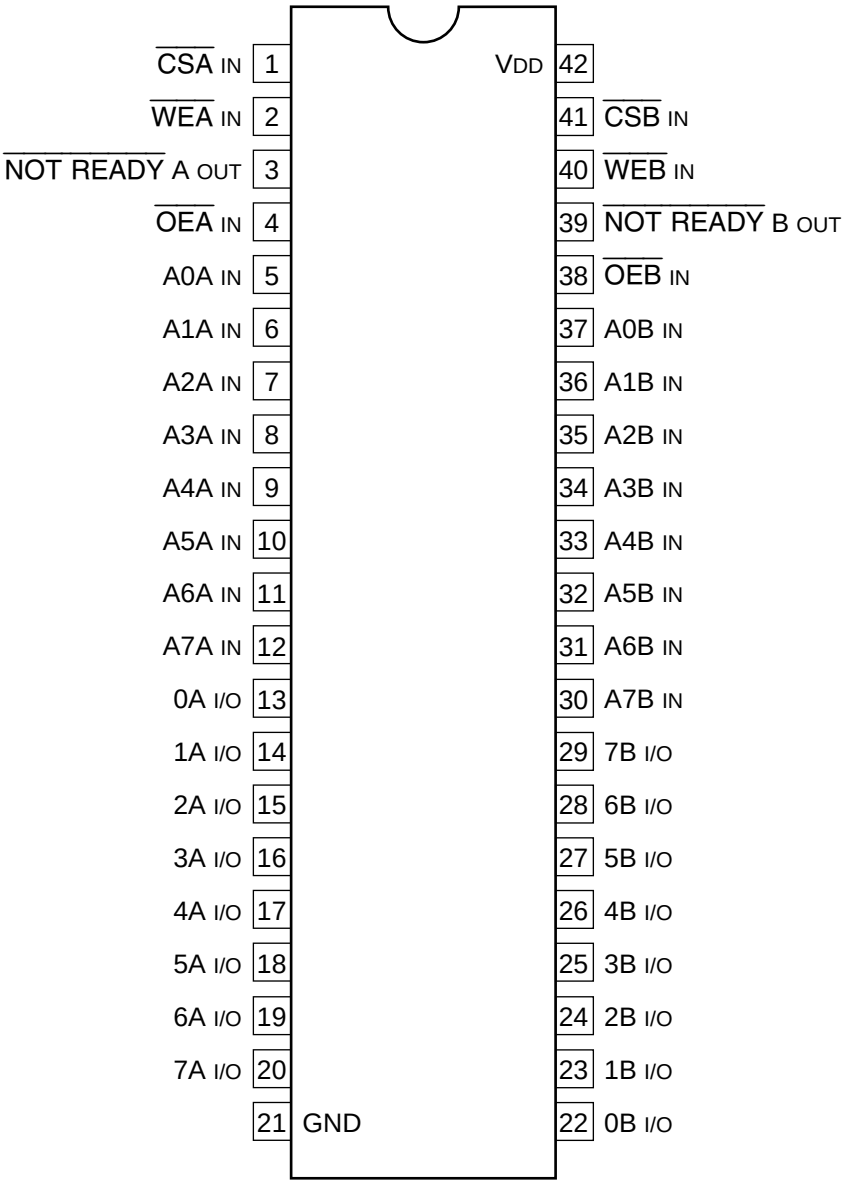
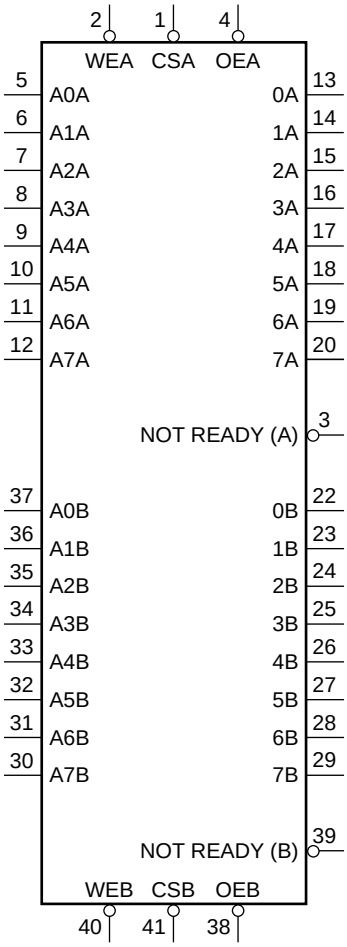
# C-MOS 2 K (256 × 8)-BIT DUAL PORT STATIC RAM

—TOP VIEW—



**A PORT**

**INPUT**

| | | |
|---|---|---|
| A0A - A7A | : | ADDRESS |
| $\overline{OSA}$ | : | CHIP SELECT |
| $\overline{OEA}$ | : | OUTPUT ENABLE |
| $\overline{WEA}$ | : | WRITE ENABLE |

**OUTPUT**

| | | |
|---|---|---|
| $\overline{NOT\ READY\ A}$ | : | NOT READY A |

**INPUT/OUTPUT**

| | | |
|---|---|---|
| 0A - 7A | : | DATA |

**B PORT**

**INPUT**

| | | |
|---|---|---|
| B0B - B7B | : | ADDRESS |
| $\overline{OSB}$ | : | CHIP SELECT |
| $\overline{OEB}$ | : | OUTPUT ENABLE |
| $\overline{WEB}$ | : | WRITE ENABLE |

**OUTPUT**

| | | |
|---|---|---|
| $\overline{NOT\ READY\ B}$ | : | NOT READY B |

**INPUT/OUTPUT**

| | | |
|---|---|---|
| 0B - 7B | : | DATA |