PRELIMINARY
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Some parametric limits are subject to change.

# M65824FP

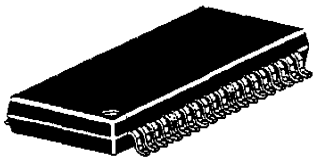
# SIGNAL PROCESSOR FOR CD PLAYER WITH BUILT-IN D/A

## DESCRIPTION

The M65824FP is a CMOS IC for playback of a compact disk (CD-DA).
It is equipped with memory, non-adjustment PLL, 4fs digital filter and D-A converter.
The M65824FP can configure a compact CD-DA system.

## FEATURES

- Non-adjustment EFM-PLL with wide lock-range (built-in VCO)
- Jitter margin ± 8 frames
- Operatable CLV servo command
- Attenuation (-12 dB)
- Built-in 4fs digital filter
- Built-in digital de-emphasis circuit
- Built-in D-A converter
- Compact set by the adoption of a compact package
- Built-in analog LPF
- External D-A mode

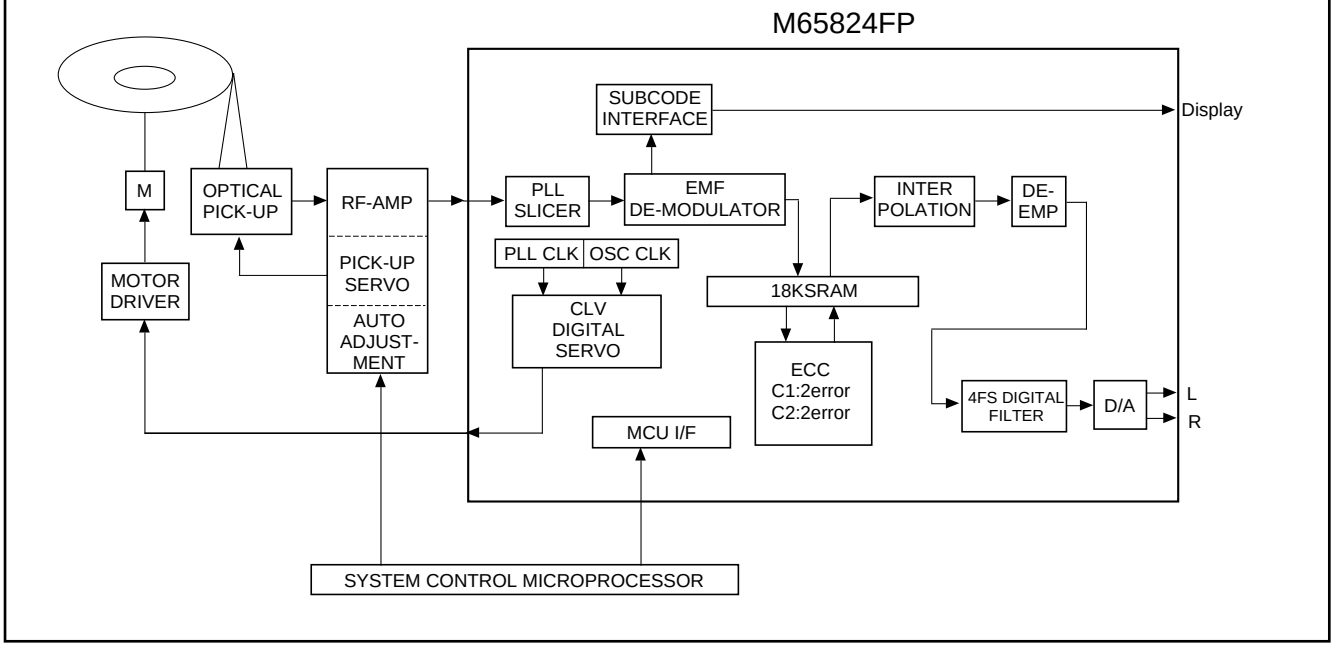


Outline 42P2R-A
0.8mm pitch 450mil SSOP
(8.4mm x 17.5mm x 2.0mm)

## RECOMMENDED OPERATING CONDITIONS

Supply voltage range (interface)..... $DV_{DD}$ = 2.7 to 5.5V
Supply voltage range (internal circuit, analog)
..... DSPS, $AV_{DD}$ = 2.7 to 3.3V
Rated supply voltage (interface)..... $DV_{DD}$ = 5.0V
Rated supply voltage (internal circuit, analog)
..... DSPS, $AV_{DD}$ = 3.0V
Rated power consumption..... 100 mW

## SYSTEM CONFIGURATION



# M65824FP

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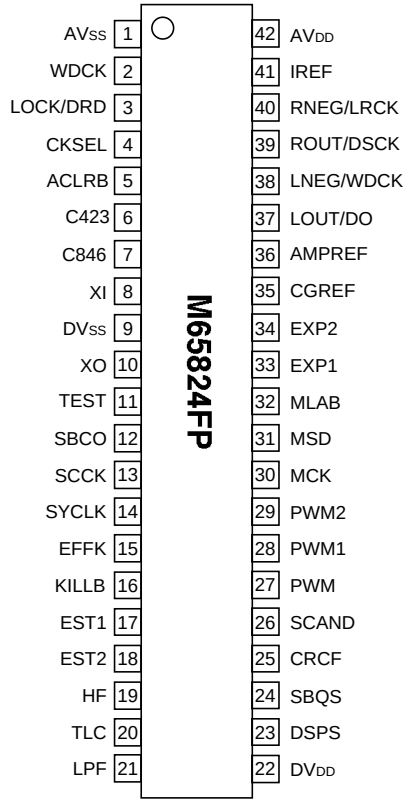
## SIGNAL PROCESSOR FOR CD PLAYER WITH BUILT-IN D/A

### PIN CONFIGURATION (TOP VIEW)




Outline 42P2R-A

### BUILT-IN FUNCTIONS

| | |
|---|---|
| •D/A converter | •64fs 1 bit ∑ Δ D-A converter<br>•S/N:74dB (typ.) |
| •Memory | •Built-in 18K SRAM<br>•Jitter margin ± 8 frames |
| •PLL block | •Built-in non-adjustment VCO (Bit clock reproduction)<br>• Non-adjustment slice level control |
| •EFM demodulator | •EFM modulation<br>•Frame sync detection/protection and insertion<br>•Frame monitor output |
| •Subcode modulator | •Modulation of subcodes P to W. serial output (conforming to EIJA CP-309)<br>•Subcode Q register<br>•CRC check<br>•Subcode sync signal output (S0/S1) |
| •CIRC block | •Emphasis detection, built-in de-emphasis control<br>•C1: double correction, C2: double correction<br>•Unscramble<br>•De-interleave |
| •Interpolation processing unit | •Error monitor output<br>•Average value interpolation and pre-value hold |
| •D-A interface | •Mute control |
| •Digital filter | •Quadruple over sampling I I R type filter |
| •De-emphasis block | •Bi-primary I I R filter<br>•Emphasis detection/automatic operation |
| •CLV servo block | •PWM output<br>•Reduced disk rotation detection output |
| •Microcomputer I/F block | •CLV servo control command<br>•Mute control<br>•-12 dB attenuation<br>•Subcode Q register interface |

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## PIN DESCRIPTION

| Pin No. | Symbol | I/O | Function |
|---|---|---|---|
| ① | AVSS | - | Analog system GND |
| ② | WDCK | O | Word clock output: f=88.2kHz |
| ③ | LOCK/DRD | O | Sync status/reduced disk rotation detection output |
| ④ | CKSEL | I | System clock select input, "L": 8.4672 MHz/"H": 16.9344 MHz |
| ⑤ | ACLRB | I | System reset input: reset="L" |
| ⑥ | C423 | O | Crystal system 4.2336 MHz clock output |
| ⑦ | C846 | O | Crystal system 8.4672 MHz clock output |
| ⑧ | XI | I | Crystal oscillator input (built-in feedback resistance)<br>CKSEL="L": 8.4672MHz/CKSEL="H": 16.9344MHz |
| ⑨ | DVss | - | Digital system GND |
| ⑩ | XO | O | Crystal oscillator output |
| ⑪ | TEST | I | Shipment test pin: For test="H" |
| ⑫ | SBCO | O | Subcode serial output |
| ⑬ | SCCK | I | Subcode read clock input |
| ⑭ | SYCLK | O | Frame sync output: Lock="H" |
| ⑮ | EFFK | O | PLL system frame clock output: duty≒50% |
| ⑯ | KILLB | O | Digital silence output: Silence="L" open drain output |
| ⑰ | EST1 | O | Error status output 1: at C1 error detection="H" |
| ⑱ | EST2 | O | Error status output 2: at C2 error detection="H" |
| ⑲ | HF | I | Playback signal input |
| ⑳ | TLC | O | Slice level control output |
| ㉑ | LPF | I/O | PLL loop filter connection terminal |
| ㉒ | DVDD | - | Power supply to I/O block |
| ㉓ | DSPS | - | Power supply to internal logic circuit |
| ㉔ | SBQS | O | Subcode Q register read interrupt signal: Read enable: "L" |
| ㉕ | CRCF | O | CRC result of subcode Q: CRC OK="H" |
| ㉖ | SCAND | O | Subcode sync signal output: Synchronization="H" |
| ㉗ | PWM | O | Disk motor drive PWM output (both sides) |
| ㉘ | PWM1 | O | Disk motor drive PWM output 1 (acceleration side) |
| ㉙ | PWM2 | O | Disk motor drive PWM output 2 (deceleration side) |
| ㉚ | MCK | I | Microcomputer I/F shift lock |
| ㉛ | MSD | I/O | Microcomputer I/F serial data I/O |
| ㉜ | MLAB | I | Microcomputer I/F latch clock (built-in 22kΩ pull-up resistance) |
| ㉝ | EXP1 | I | Additional microcomputer input port 1 (built-in 4.7kΩ pull-up resistance) |
| ㉞ | EXP2 | I | Additional microcomputer input port 2 (built-in 4.7kΩ pull-up resistance) |
| ㉟ | CGREF | I | Current source reference current input pin for LPF |
| ㊱ | AMPREF | I | Operation amplifier reference voltage setting pin for LPF |
| ㊲ | LOUT/DO | O | L-ch audio signal output/serial data output (in external D-A mode) |
| ㊳ | LNEG/WDCK | O | L-ch current source output/word clock output (in external D-A mode) |
| ㊴ | ROUT/DSCK | O | R-ch audio signal output/data shift clock output (in external D-A mode) |
| ㊵ | RNEG/LRCK | O | R-ch current source output/L-R clock output (in external D/A mode) |
| ㊶ | IREF | I | Detection/PLL circuit reference current input |
| ㊷ | AVDD | - | Analog system power supply |

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**ABSOLUTE MAXIMUM RATINGS** (Ta=25°C, unless otherwise noted)

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $DV_{DD}$-$DV_{SS}$ | Supply voltage (I/O) | -0.3 to +6.5 | V |
| $AV_{DD}$-$AV_{SS}$ | Supply voltage (analog) | -0.3 to +3.6 | V |
| DSPS-$DV_{SS}$ | Supply voltage (internal circuit) | -0.3 to +3.6 | V |
| $V_I$ | Input voltage | $DV_{DD}$-0.3≤$V_I$≤$DV_{DD}$+0.3 | V |
| Vo | Output voltage | $DV_{SS}$≤$V_O$≤$DV_{DD}$ | V |
| $P_d$ | Power dissipation | 350 | mW |
| $T_{opr}$ | Operating temperature | -10 to +70 | °C |
| $T_{stg}$ | Storage temperature | -40 to +125 | °C |

**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $DV_{DD}$ | Supply voltage (I/O) | | 2.7 | 5.0 | 5.5 | V |
| $AV_{DD}$ | Supply voltage (analog) | | 2.7 | 3.0 | 3.3 | V |
| DSPS | Supply voltage (internal circuit) | | 2.7 | 3.0 | 3.3 | V |
| $V_{IH}$ | Input voltage ("H" level) | | $DV_{DD}$•0.7 | - | $DV_{DD}$ | V |
| $V_{OL}$ | Output voltage ("L" level) | | $DV_{SS}$ | - | $DV_{SS}$•0.3 | V |
| fosc | Oscillation frequency | | - | 8.4672 | - | MHz |
| fvco | Oscillation frequency | | - | 8.6436 | - | MHz |

**ELECTRICAL CHARACTERISTICS** (Ta=25°C, $V_{DD}$=5V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $I_{DD}$ | Circuit current | fosc=8.4672MHz fvco=8.6436MHz | - | 20 | - | mA |
| $V_{OH}$ | Output voltage ("H" level) | $DV_{DD}$=5.0V $I_{OH}$=-1.0mA | 4.5 | - | - | V |
| $V_{OL}$ | Output voltage ("L" level) | $DV_{DD}$=5.0V $I_{OL}$=1.0mA | - | - | 0.4 | V |
| $I_{IH}$ | Input voltage ("H" level) | $V_{IH}$=4.5 | - | - | 2 | µA |
| $I_{IL}$ | Input voltage ("L" level) | $V_{IL}$=0.5V | -2 | - | - | µA |

**POWER SUPPLY**

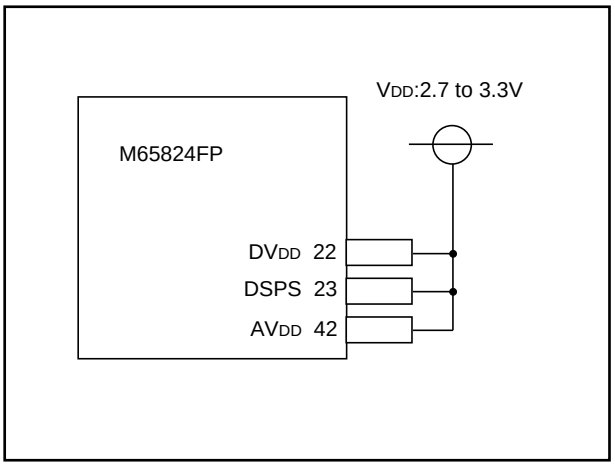


**Fig.1 3.0V system application example (supply voltage range of 2.7V to 3.3V)**

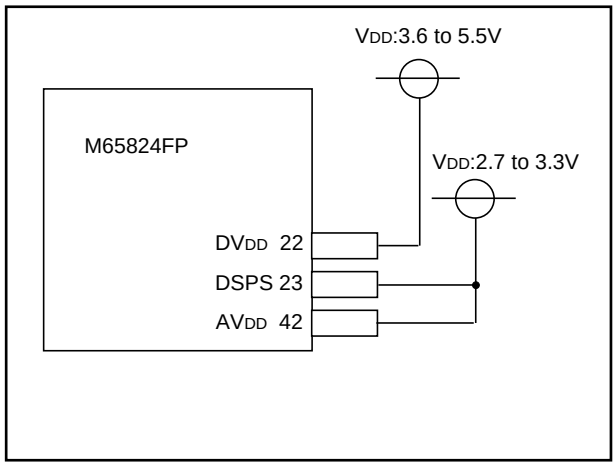


**Fig.2 5.0V system application example (two power supplies are required)**

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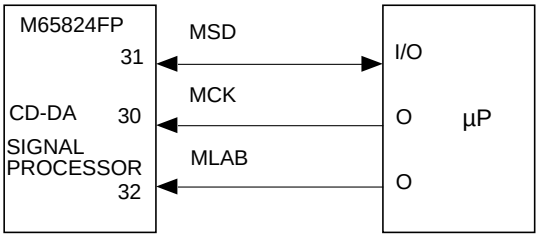
## FUNCTION DESCRIPTION

### 1. MICROCOMPUTER INTERFACE

**(1) Pin assignments**




**(2) Description**

MLAB: Latch signal/data I/O switching signal
(MLAB="H":Write from µP)
(MLAB="L":Read from µP)

MCK: Clock signal
MSD: Serial data I/O

**(3) Operation description**

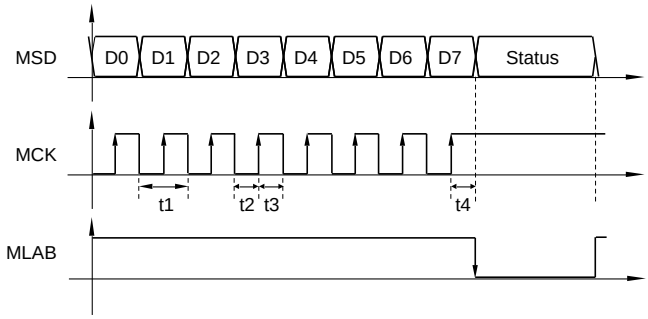
• Microcomputer command read/write

Data (MSD) is read at a rising edge of the clock pulse (MCK).
When a command is determined at a falling edge of the latch line (MLAB), the data line (MSD) is concurrently switched to the output mode to output a status requested by data bits D3, D2, D1 and D0.
When the latch line is set to "H", the data line is returned to the input mode again.

•Status request/interface command

When requesting various types of the M65824FP status, a microcomputer writes data in D3, D2, D1 and D0 for indicating the requested status in advance.
After this command is latched, the status is continuously output while the latch line (MLAB) is set to "L".

**(4) Microcomputer I/F timing chart**




| Symbol | Parameter | Min. | Unit |
|---|---|---|---|
| t1 | Shift clock width | 200 | nsec |
| t2 | Shift clock setup | 100 | nsec |
| t3 | Shift clock hold | 100 | nsec |
| t4 | Shift clock setup | 100 | nsec |

**(5) M65824FP command list**

Initial value after power is turned on: 00000000

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| Disk motor | | Audio function | | Status/interface command | | | |

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### (6) Detailed data

① Disk motor control

| D7 | D6 | Function |
|---|---|---|
| 0 | 0 | Disk motor off |
| 0 | 1 | Accelerates the disk motor. Applies the maximum acceleration voltage to the motor. |
| 1 | 0 | Decelerates the disk motor. Applies the maximum deceleration voltage to the motor. |
| 1 | 1 | Disk motor CLV control |

② Audio functions

| D5 | D4 | Function |
|---|---|---|
| 0 | 0 | Muting |
| 0 | 1 | Muting release |
| 1 | 0 | Reserved |
| 1 | 1 | 12 dB attenuation |

③ Status/interface command

| D3 | D2 | D1 | D0 | Function |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Detects reduced disk rotating speed. "L" when the disk rotating speed is 2/3 or more of the normal speed. |
| 0 | 0 | 0 | 1 | PLL lock status. "L" at locked. |
| 0 | 0 | 1 | 0 | Subcode read status. "L" when new subcode is received |
| 0 | 0 | 1 | 1 | External D-A mode (In case of input after reset) |
| 0 | 1 | 0 | 0 | Logical value of EXP1 (pin㉝) |
| 0 | 1 | 0 | 1 | Logical value of EXP2 (pin㉞) |
| 0 | 1 | 1 | 0 | Reserved |
| 0 | 1 | 1 | 1 | Reserved |
| 1 | 0 | 0 | 0 | PLL loop close (= HFD: "L") |
| 1 | 0 | 0 | 1 | PLL loop open (= HFD: "H") |
| 1 | 0 | 1 | 0 | Reserved |
| 1 | 0 | 1 | 1 | Reserved |
| 1 | 1 | 0 | 0 | Reserved |
| 1 | 1 | 0 | 1 | Reserved |
| 1 | 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | 1 | Reserved |

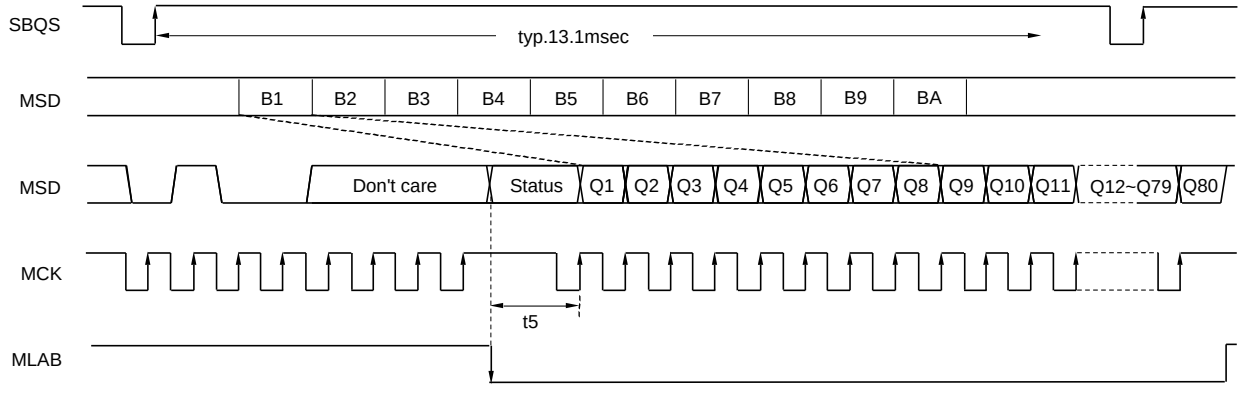
### (7) Subcode Q register interface

Data of subcode Q is stored in the internal 80-bit register and can be read using a microcomputer.

Subcode ready status command is written to read subcode Q using a microcomputer. (MSD DATA 0100xxxx)

When the subcode ready status is set to "L", a clock is sent with the latch line (MLAB) kept set to "L" to read the data of subcode Q from the internal register.

Read all subcode Q data from the rising edge of SBQS until the next rising edge (for approximately 13.1 msec).




t5: Mode setup time (min. 200 nsec)

•SBQS is set to "L" when both the following two conditions are satisfied at the same time.

(a) CRC check OK

(b) When the two subcode syncs (S0, S1) are normal

•A microcomputer can read information on subcode Q using the M65824FP only when SBQS is set to "L".

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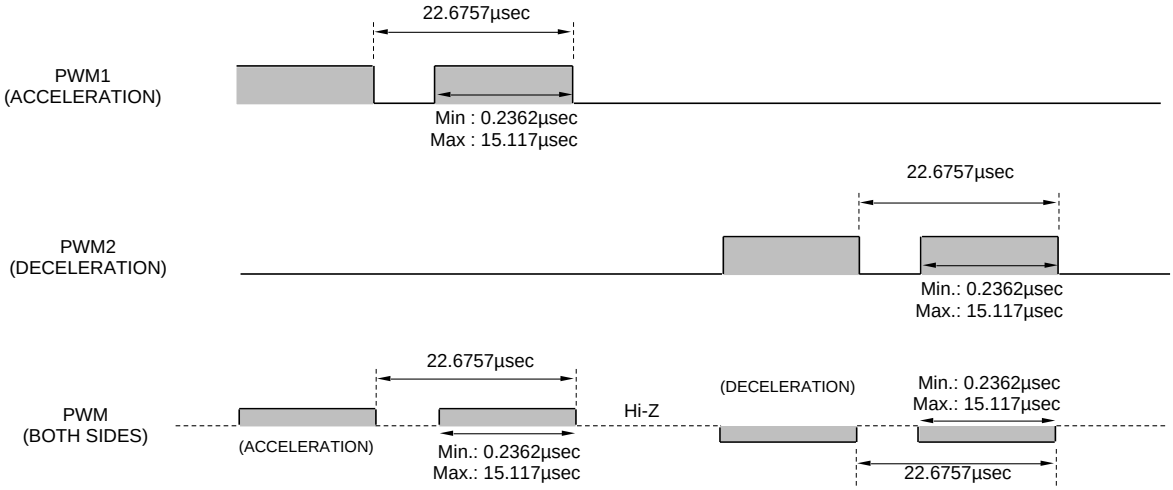
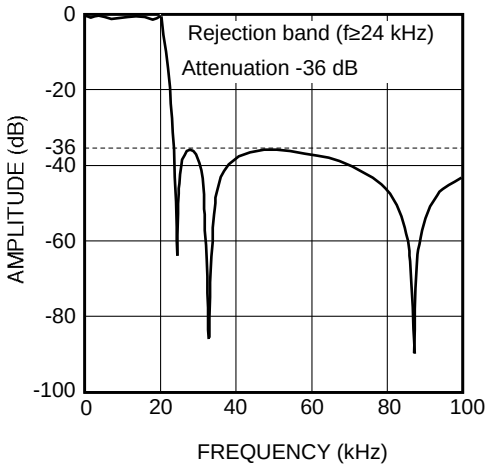
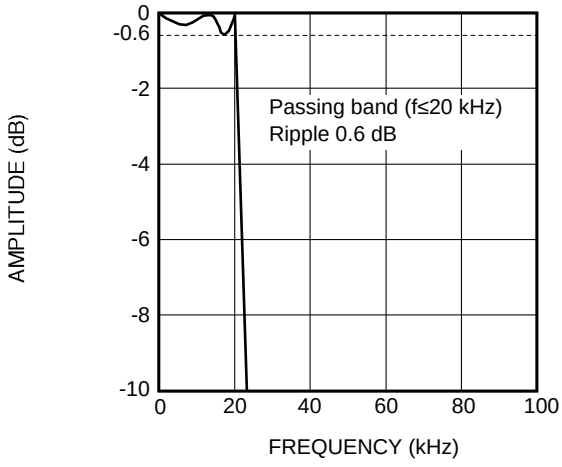
**2. DISK MOTOR CONTROL PULSE (CLV mode)**




**3. DIGITAL FILTER**



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## APPLICATION EXAMPLE