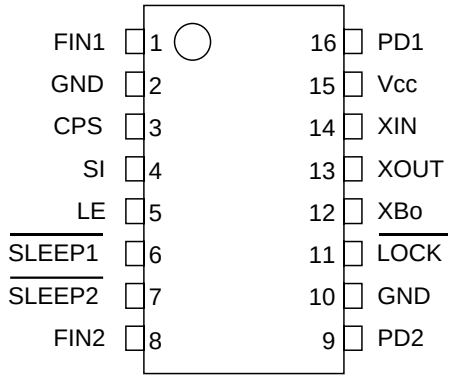
M64811AGP

1.1GHz/500MHz DUAL PLL FREQUENCY SYNTHESIZER FOR DIGITAL CELLULAR PHONE

DESCRIPTION

The M64811AGP is a 1.1GHz/500MHz band two-system one-chip PLL frequency synthesizer .
Using a high performance Bi-CMOS process , the product contains one two-modulus (1/32 and 1/33) prescaler that accepts inputs up to 1.1GHz and another two-modulus (1/16 and 1/17) prescaler that accepts inputs up to 500MHz ,thus helping make the equipment compact .

PIN CONFIGURATION (TOP VIEW)



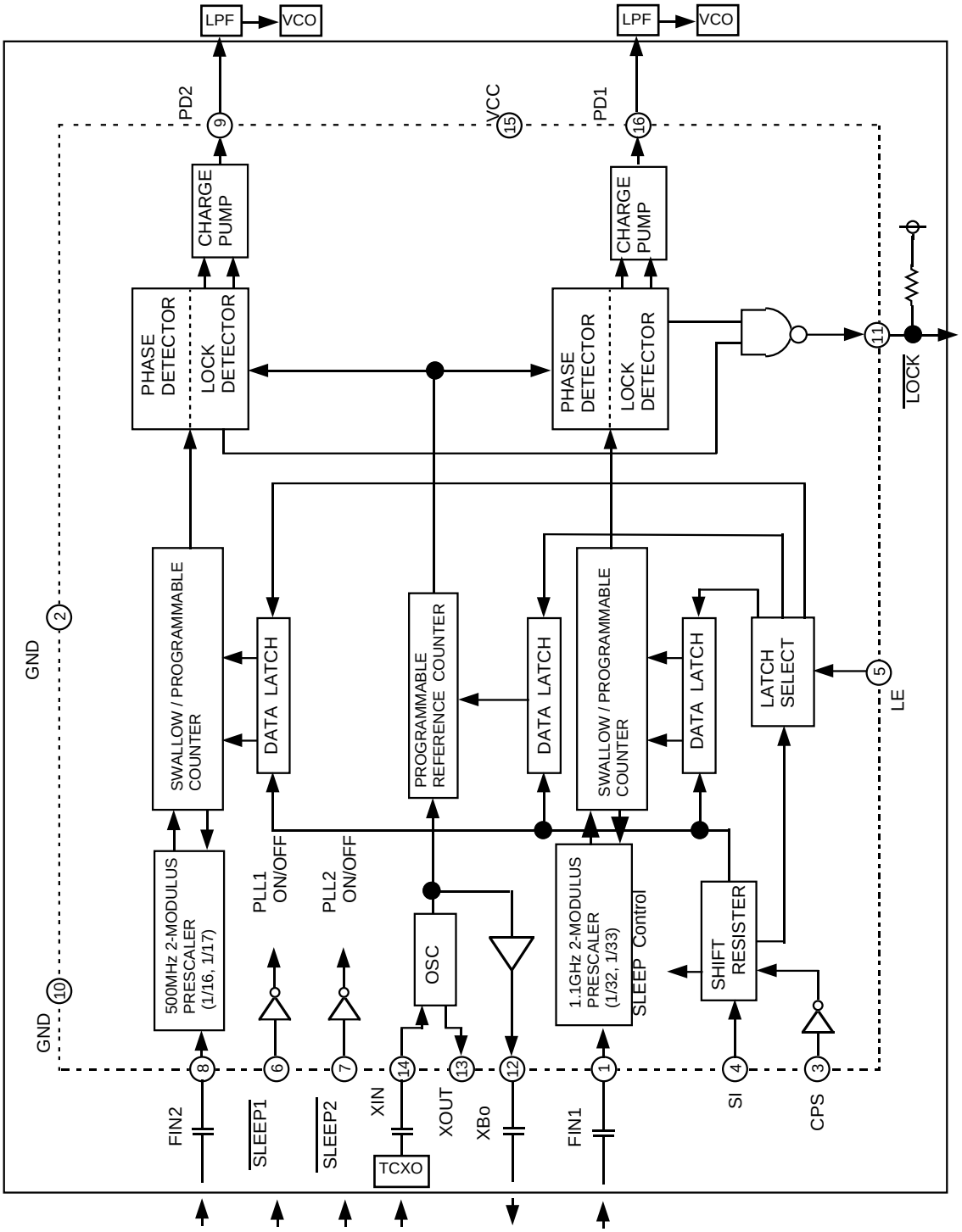
FEATURES

- Operating supply voltage : 2.7V~3.6V
- Operating temperature : -30°C~+85°C
- 2 PLL systems (1.1GHz and 500MHz) are on one chip .
  PLL1 : 700MHz~1.1GHz PLL2 : 100MHz~500MHz
- Low power consumption (Icc=8mA Typ at Vcc=3V) .
- Dividing ratio setting ranges :
  FIN1 for 1.1GHz VCO• • • • • N(VCO1)=1,024~131,071
  FIN2 for 500MHz VCO• • • • • N(VCO2)=256~131,071
  OSC for Fref • • • • • • • • • • • • • N(Fref)=5~2,047
- Each loop has input pin for sleep mode .
  Power supplies to 2 loops can be independently turned ON/OFF .
  Also can be controlled by the serial data . (When SLEEP1 and SLEEP2 is "H" .)
- The PLL standard oscillation circuit can adopt a B-E Colpitts type oscillation circuit to from a stable oscillation circuit.
- Current controlled charge pump . (Icp=±2mA const.)
- Locked condition detecting output
  If a phase difference smaller than 3 times (Δt) of the OSC period continues for 15 periods or longer , the condition is judged as locked, and the LOCK terminal goes to "L" .
  (When , for example , fosc=19.2 MHz , Δt=156 ns)
- PLL lock/unlock status indicate function .
  (Judged in the system turned on if the other system is turned off .)
- Small package (16pin SSOP, lead pitch : 0.65mm)

APPLICATION

- Digital cordless phone (CT2)
- Digital cellular phone (PDC)

BLOCK DIAGRAM



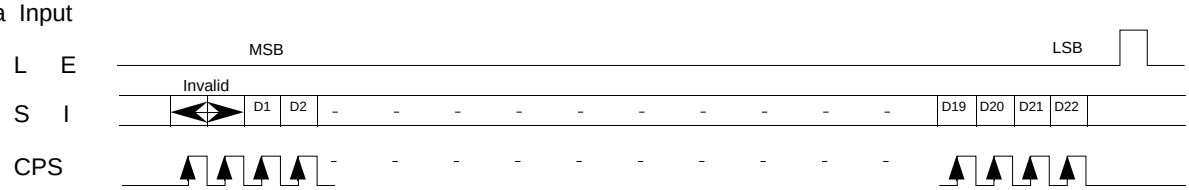
1.1GHz/500MHz DUAL PLL FREQUENCY SYNTHESIZER FOR DIGITAL CELLULAR PHONE

FUNCTION DESCRIPTION OF PINS

Pin No.	Pin Identification	Description
1	FIN1	Input from the VCO , Fmax = 1.1GHz .
2	GND	Ground .
3	CPS	Clock pulse input . Shift register clock input pin .
4	SI	Binary serial data input . Shift register data input pin
5	LE	Load enable input . When LE is HIGH , data stored in the shift registers is loaded into the appropriate latch .
6	$\overline{\text{SLEEP1}}$	PLL1 power control . "H" = normal operation , "L"=power down .
7	$\overline{\text{SLEEP2}}$	PLL2 power control . "H" = normal operation , "L"=power down .
8	FIN2	Input from the VCO , Fmax = 500MHz .
9	PD2	Charge pump2 output . Tristate output . High Z when PLL2 power is off .
10	GND	Ground .
11	$\overline{\text{LOCK}}$	When loops are locked ••••••••"L" , When one of loops is unlocked••••••••"High Z" . If one loop is sleep mode , the status of the other loop is checked for judgment .
12	XBo	Buffer output of oscillator .
13	XOUT	Crystal Oscillator input .
14	XIN	
15	Vcc	Power supply . Vcc = 2.7~3.6V .
16	PD1	Charge pump1 output . Tristate output . High Z when PLL1 power is off .

FUNCTION DESCRIPTION

1.Data Input

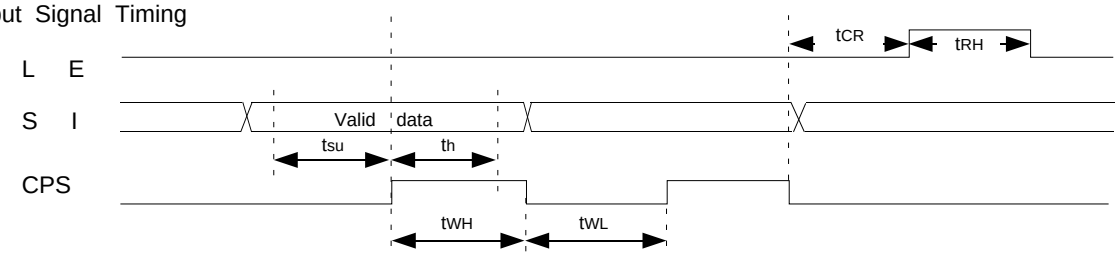


Note 1) At the leading edge of the CPS input , the status of the SI input is written into the shift register .

Note 2) The bit just before LE becomes "H" is LSB , and SI before MSB becomes invalid .

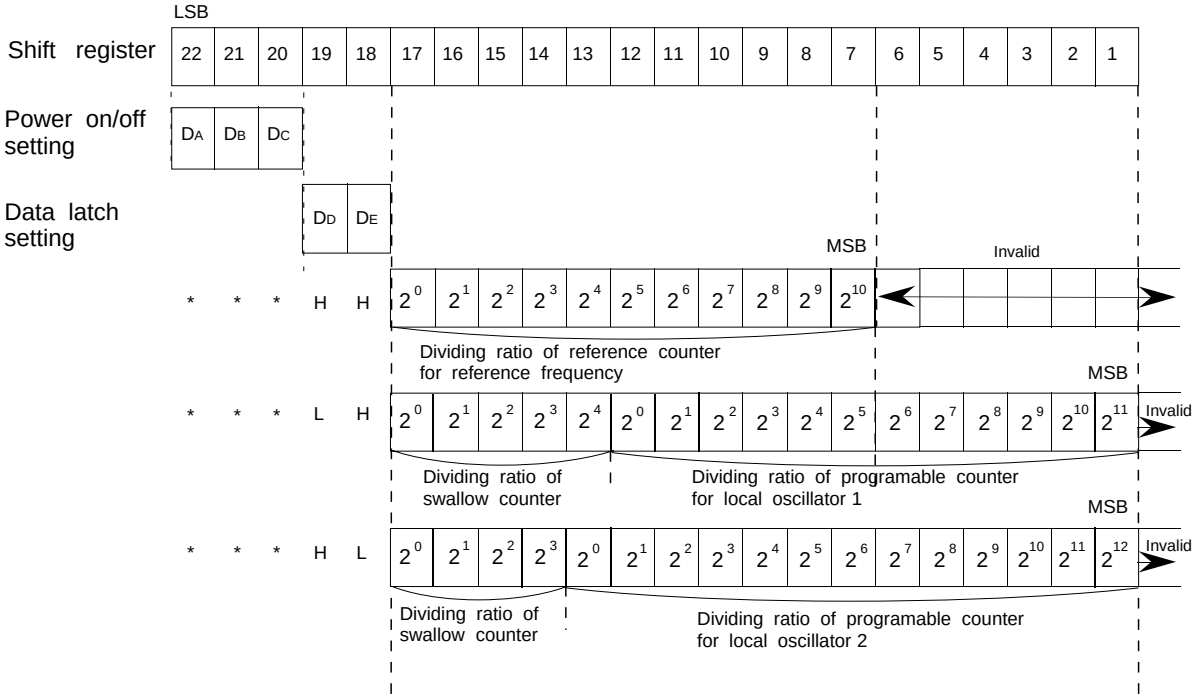
Note 3) When LE is "H" , the data stored in the shift registers is loaded into the appropriate latch .

2.Input Signal Timing



tsu=th=tWH=tWL=0.1µsmin.
tCR=tRH=0.1µsmin.

3.Bit Configuration of Shift Register



Note 4) Power on/off control of PLL system is set by D_A, D_B, and D_F.

External Control Pin		Serial Data			Description			
$\overline{SLEEP1}$	$\overline{SLEEP2}$	D_A	D_B	D_C	PLL1	PLL2	OSC	XBo
L	L	*	*	*	OFF	OFF	ON	ON
L	H	0	0	*	OFF	ON	ON	ON
L	H	0	1	*	OFF	OFF	ON	ON
L	H	1	0	*	OFF	ON	ON	ON
L	H	1	1	*	OFF	OFF	ON	ON
H	L	0	0	*	ON	OFF	ON	ON
H	L	0	1	*	ON	OFF	ON	ON
H	L	1	0	*	OFF	OFF	ON	ON
H	L	1	1	*	OFF	OFF	ON	ON
H	H	1	1	1	OFF	OFF	OFF	OFF
H	H	1	1	0	OFF	OFF	ON	ON
H	H	1	0	1	OFF	ON	ON	OFF
H	H	1	0	0	OFF	ON	ON	ON
H	H	0	1	1	ON	OFF	ON	OFF
H	H	0	1	0	ON	OFF	ON	ON
H	H	0	0	1	ON	ON	ON	OFF
H	H	0	0	0	ON	ON	ON	ON

ON;Power on , OFF;Power off

Note 5) D_D and D_E are used to select latched data to be updated.

Data		Description
D_D	D_E	
0	0	Unused.
0	1	Data latched for local oscillator 1 is updated.
1	0	Data latched for local oscillator 2 is updated.
1	1	Data latched for reference frequency .

Note 6) Dividing ratio of the reference counter for reference frequency is given by 11-bit binary coads .

N(fREF1)=5~2047

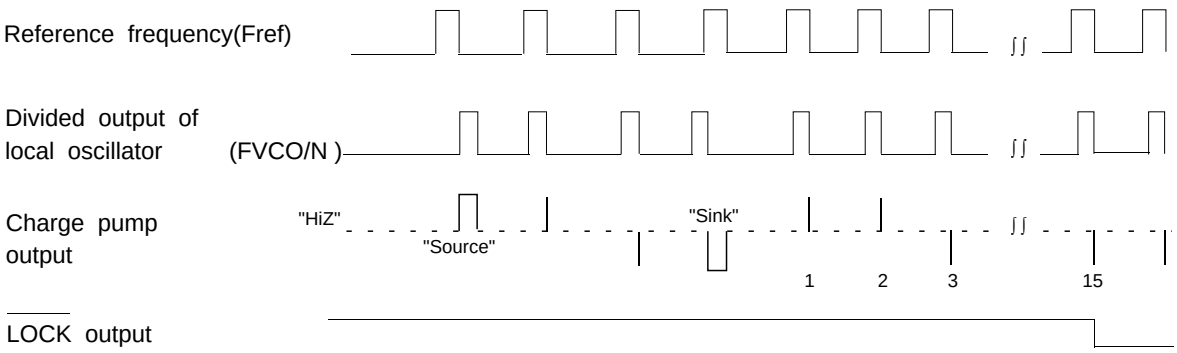
Note 7) Dividing ratio N(VCO1) of VCO1 for local oscillator1 is given by 5-bit swallow counter and 12-bit programable counter .

N(VCO1)=32 x M+A (A<M)
M : Preset dividing ratio of 12-bit programmable counter (32~4095)
A : Preset dividing ratio of 5-bit swallow counter (0~31)

Note 8) Dividing ratio N(VCO2) of VCO2 for local oscillator2 is given by 4-bit swallow counter and 13-bit programable counter .

N(VCO2)=16 x M+A (A<M)
M : Preset dividing ratio of 13-bit programmable counter (16~38191)
A : Preset dividing ratio of 4-bit swallow counter (0~315)

4.Charge Pump and LOCK Detection



Note 9) If the phase of divided local oscillator output (FVCO/N) is behind that of the reference frequency (Fref) , the charge pump output becomes "Source" status , if advancing , "Sink" status .

Note 10) If a phase difference smaller than 3 times of the OSC period continues for 15 periods longer , the $\overline{\text{LOCK}}$ output becomes "L" .
(When , for example , Fosc = 19.2 MHz , Δt = 156 ns)

Note 11) If one of the power supplies to PLLs is turned off , a judgment is made based on only the condition of the other loop .

Note 12) The $\overline{\text{LOCK}}$ output circuit yields an open drain N-channel transistor output . It should be pulled up to Vcc .

5.Sleep Mode Input

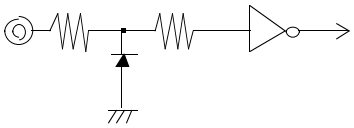
By status of $\overline{\text{SLEEP1}}$ and $\overline{\text{SLEEP2}}$, each PLL can be selected to either sleep mode (Power supply is turned off .) or operation mode .

If $\overline{\text{SLEEP}}$ input is "H" , the PLL becomes normal operation mode .
(Power supplies to turn ON/OFF can be controlled by the serial data ; submit to note 4 .)

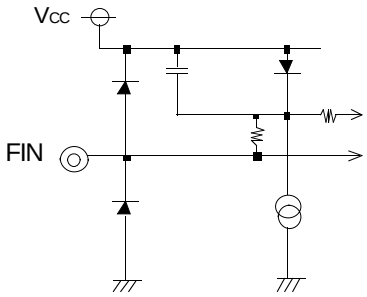
If $\overline{\text{SLEEP}}$ input is "L" , the PLL becomes sleep mode . (Power supply is turned off .)

INPUT / OUTPUT CIRCUIT DIAGRAM

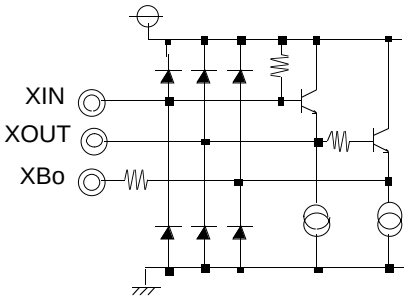
1 SI,CPS<LE,$\overline{SLEEP1}$,$\overline{SLEEP2}$



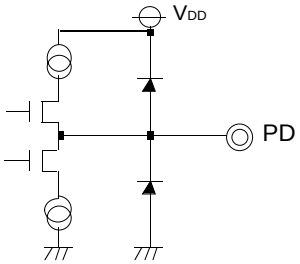
2 Prescaler input(FIN1,FIN2)



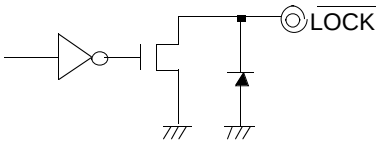
3 OSC input



4 Charge Pump output(PD1,PD2)



5 $\overline{LOCK}$



ABSOLUTE MAXIMUM RATINGS (Ta= -30~85°C, unless otherwise specified .)

Symbol	Parameter	Test Condition	Ratings		Unit
			Min.	Max.	
Vcc	Supply Voltage	GND=0V	-0.3	4.5	V
V I	Input Voltage	SI , CPS , LE pin : GND=0V	-0.3	4.5	V
VO	Output Voltage	Output pin : GND=0V	-0.3	4.5	V
Pd	Power Dissipation	Ta=85°C(Allowable dissipation of package)		250	mW
Vopd	Open Drain Voltage	GND=0V	-0.3	4.5	V
Topr	Operating Temperature		-30	85	°C
Tstg	Storage Temperature		-40	125	°C

RECOMMENDED OPERATING CONDITIONS (Ta= -30~85°C, unless otherwise specified .)

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
Vcc	Supply Voltage		2.7		3.6	V
FIN1	Operating Frequency	Vcc=2.7~3.6V	0.7		1.1	GHz
FIN2			100		500	MHz
VIN1	Input Sensitivity	FIN1=1.0~2.0GHz	-10		2	dBm
VIN2		FIN2=100~500MHz	-16		-4	
VXIN	Oscillator Sensitivity @	Vcc=2.7~3.6V	0.4		1.0	Vp-p

@Recommendation : X'tal (19.2MHz)

ELECTRICAL CHARACTERISTICS (Ta= 25°C, unless otherwise specified .)

Symbol	Parameter	Pin	Test Condition	Limits			Unit
				Min.	Typ.	Max.	
I PD-SOURCE	Charge Pump Output (Source) Current	PD1 , PD2	Vcc=3.0V , VPD=Vcc/2		2.0		mA
I PD-SINK	Charge Pump Output (Sink) Current				-2.0		
Icc1	Supply Current	Vcc	Vcc=3V , Both PLLs are on .		8.0		mA
Icc2			Vcc=3V , Only PLL1 is on .		5.5		
Icc3			Vcc=3V , Only PLL2 is on .		4.5		
Icc4			Vcc=3V , Both PLLs are off .			10	µA

HANDLING PRECAUTIONS

1. This IC contains fine structure components to achieve high performance . Therefore , take extra precaution to protect the IC from surge voltage caused by static electricity .
2. If one of two PLLs is not used , please make power supply of that turn off .