M62001L,FP/M62002L,FP/M62003L,FP/M62004L,FP/ M62005L,FP/M62006L,FP/M62007L,FP/M62008L,FP

LOW POWER 2 OUTPUT SYSTEM RESET IC SERIES

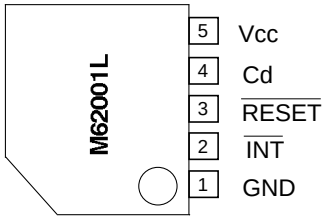
DESCRIPTION

The M62001~8 are semiconductor integrated circuits whose optimum use is for the detection of the rise and fall in the power supply to a microcomputer system in order to reset or release the microcomputer system.
The M62001~8 carry out voltage detection in 2 steps and have 2 output pins.As Bi-CMOS process and low power dissipating circuits are employed,they output optimum signals through each output pin to a system that requires RAM backup, As output signals,interruption(INT) and compulsive reset(RESET) signals are available.The interruption signal(INT) is used to alter the microcomputer from normal mode to backup mode and vice versa. these output signals are classified into pulse type(M62001~M62004) and hold type (M62005~M62008).

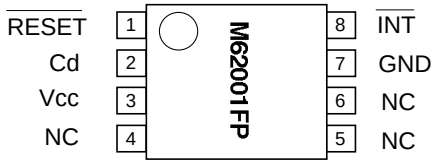
FEATURES

- Bi-CMOS process realizes a configuration of low current dissipating circuits.
  Circuit current
  Icc=5μA(Typ.,normal mode,Vcc=5.0V)
  Icc=1μA(Typ.,backup mode,Vcc=2.5V)
- Two-step detection of supply voltage
  Detection voltage in normal mode (2-types)
  Vs=4.45V/4.25V(Typ.)
  Detection voltage in backup mode
  V_{BATT}=2.15V(Typ.)
- Two outputs
  Reset output ($\overline{RESET}$):Output of compulsive reset signal
  Interruption output($\overline{INT}$):Output of interruption signal
- Two types of output forms:CMOS and open drain
- Two types of interruption output (INT) signals
  Pulse type (M62001~M62004)
  Hold type (M62005~M62008)
- Two types of outline packages
  5-pin plastic SIP (single in-line package)
  8-pin plastic SOP (mini flat package)
- Output based on RAM backup mode (See the timing chart.)

PIN CONFIGURATION (TOP VIEW)



Outline 5P5T(M62001L~8L)



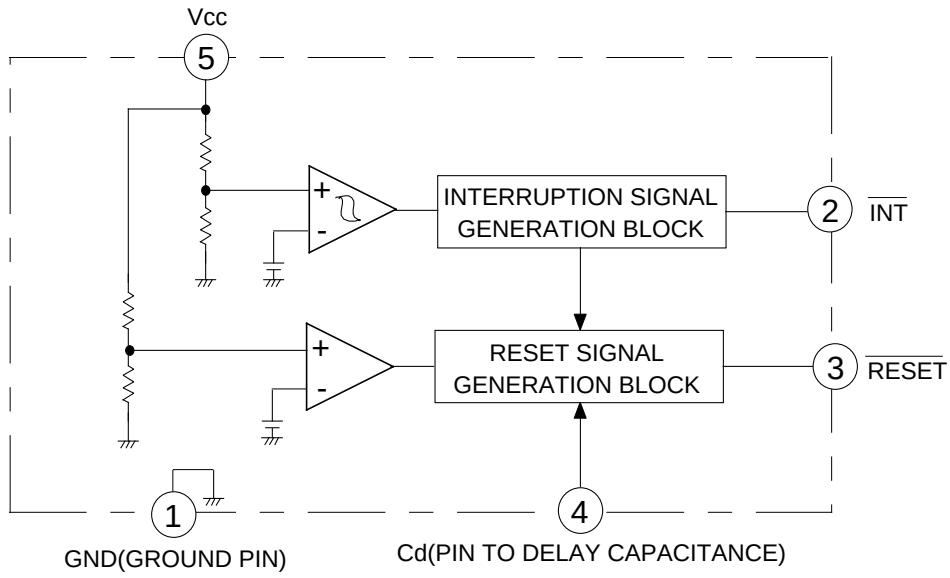
Outline 8P2S-A(M62001FP~8FP)

NC:NO CONNECTION

APPLICATION

Prevention of malfunction of microcomputer systems in electronic,equipment such as OA equipment, industrial equipment,and home-use electronic appliances.

BLOCK DIAGRAM



NOTE:This is an example showing pin Nos.of M62001L~8L.(See PIN CONFIGURATION.)

M62001L,FP/M62002L,FP/M62003L,FP/M62004L,FP/ M62005L,FP/M62006L,FP/M62007L,FP/M62008L,FP

LOW POWER 2 OUTPUT SYSTEM RESET IC SERIES

ABSOLUTE MAXIMUM RATINGS

(Ta=25°C, unless otherwise noted,These ratings commonly apply to the M62001L/FP~M62008L/FP.)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		8	V
I_{SINK}	Output sink current		5	mA
Pd	Power dissipation		440	mW
K_Θ	Thermal derating	(Ta≥25°C)	4.4	mW/°C
T_{opr}	Operating temperature		-20 ~ +75	°C
T_{stg}	Storage temperature		-40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta=25°C, unless otherwise noted,These ratings commonly apply to the M62001L/8L.)

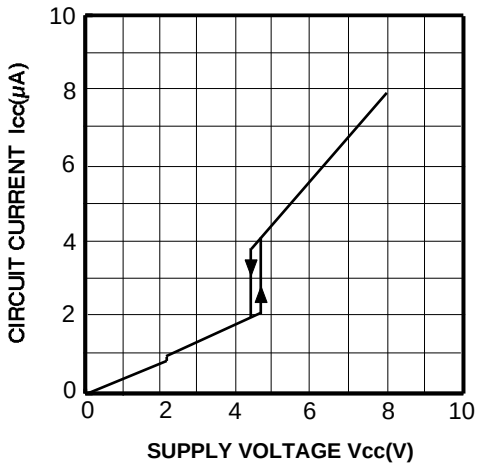
Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
Vs	Supply voltage	Interruption level during Vcc drop (Equivalent to V_{SL})	(M62001,M62002, M62005,M62006)	4.30	4.45	4.60	V
			(M62003,M62004, M62007,M62008)	4.05	4.25	4.45	
V_{BATT}	Battery voltage	Reset level at backup		2.00	2.15	2.30	V
ΔVs	Hysteresis voltage	$\Delta Vs=V_{SH}-V_{SL}$			100		mV
I_{CC}	Circuit current	Vcc=5.0V:In normal mode			5.0	20	μA
		Vcc=2.5V:In backup mode			1.0	4	
V_{sat1}	Sink ability	Vcc=4V,Io=4mA (Output saturation voltage of N-ch transistor)			0.2	0.4	V
V_{sat2}	Source ability	Vcc=4V,Io=1mA (Output saturation voltage of P-ch transistor: [CMOS output] M62001,M62003, M62005,M62007)			0.2	0.4	V
td	Delay time	External capacitance Cd=0.33μF			50		ms
tpw	Pulse width	Output pulse width (M62001,M62002, M62003,M62004)			7	10	μS
$t_{\overline{RESET}}$	Reset output response time	Time between Vcc(when falling)=V_{BATT} and output of RESET signal			30		μS
$t_{\overline{INT}}$	Interruption output reset time	Time between Vcc(when falling)=Vs and output of INT signal			100		μS

SUMMARY OF M62001L/FP~M62008L/FP

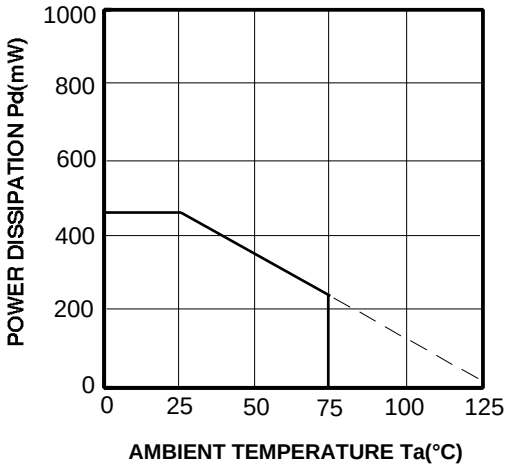
Type	Supply voltage detection level Vs(V)	Battery voltage detection level $V_{BATT(V)}$	Output form	Interruption signal output mode
M62001	4.45	2.15	CMOS	Pulse output 
M62002			Open drain	
M62003	4.25		CMOS	
M62004			Open drain	
M62005	4.45		CMOS	Hold output 
M62006			Open drain	
M62007	4.25		CMOS	
M62008			Open drain	

TYPICAL CHARACTERISTICS

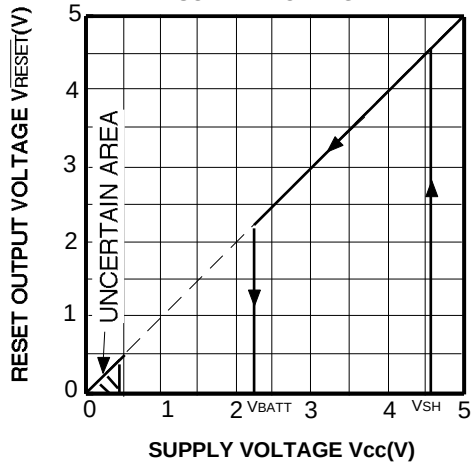
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



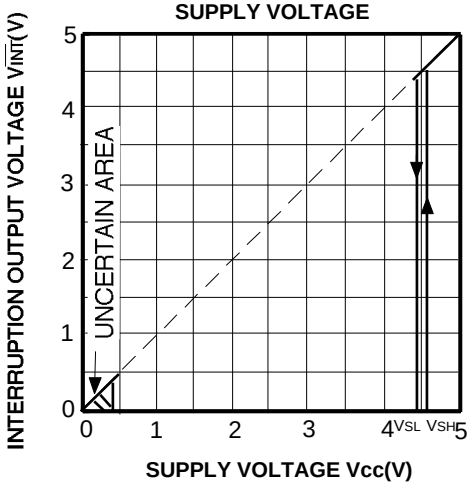
THERMAL DERATING (MAXIMUM RATING)



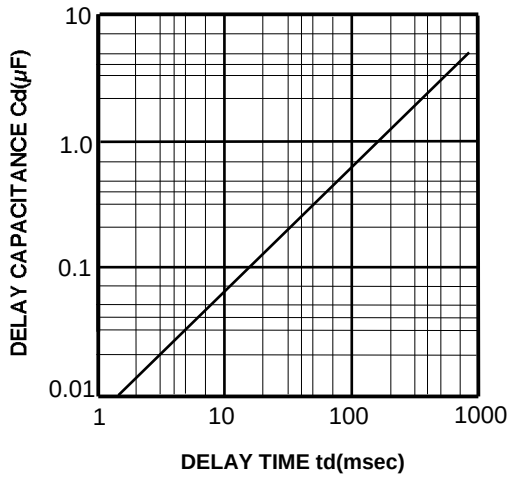
RESET OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



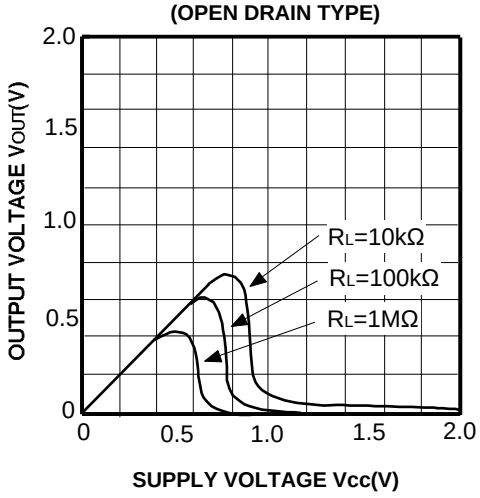
INTERRUPTION OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



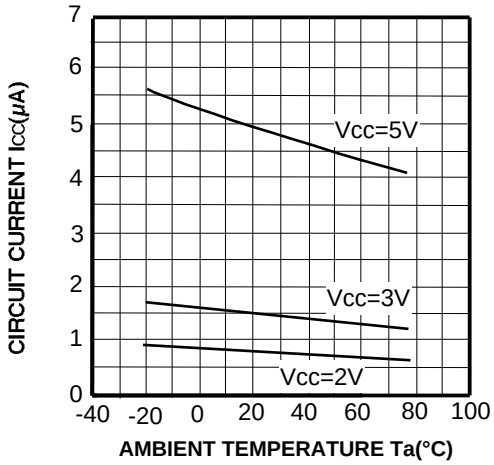
DELAY CAPACITANCE vs. DELAY TIME



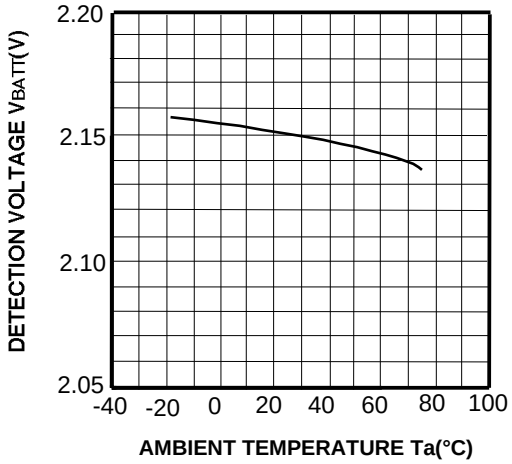
LIMIT OPERATING VOLTAGE (OPEN DRAIN TYPE)



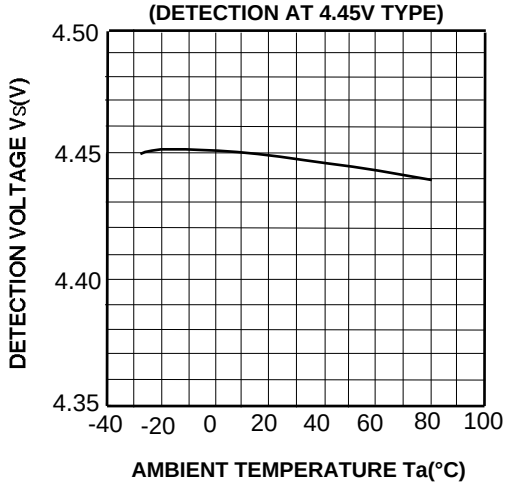
CIRCUIT CURRENT vs. AMBIENT TEMPERATURE



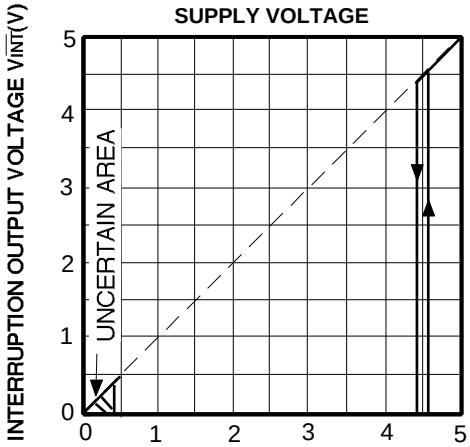
DETECTION VOLTAGE vs. AMBIENT TEMPERATURE



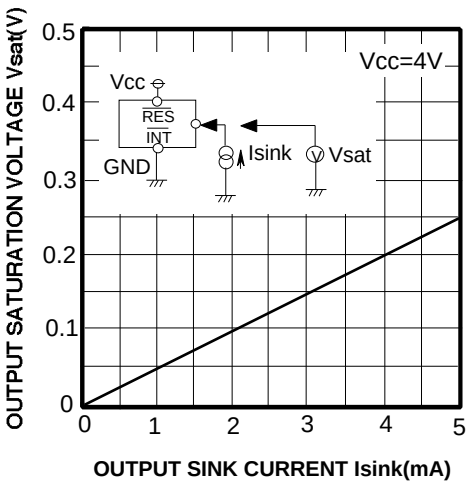
DETECTION VOLTAGE vs. AMBIENT TEMPERATURE (DETECTION AT 4.45V TYPE)



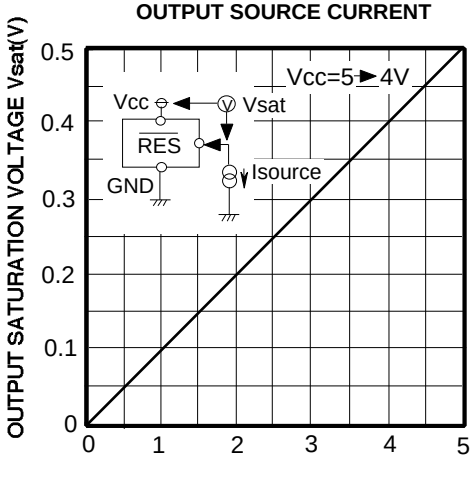
INTERRUPTION OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



Nch OUTPUT SATURATION VOLTAGE vs. OUTPUT SINK CURRENT



Pch OUTPUT SATURATION VOLTAGE vs. OUTPUT SOURCE CURRENT



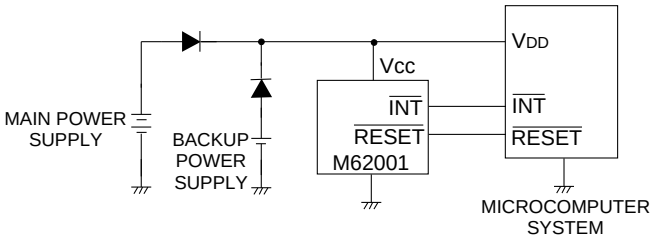
M62001L,FP/M62002L,FP/M62003L,FP/M62004L,FP/ M62005L,FP/M62006L,FP/M62007L,FP/M62008L,FP

LOW POWER 2 OUTPUT SYSTEM RESET IC SERIES

OPERATION PRINCIPLE

DESCRIPTION

In general,the memory backup function of a microcomputer,as shown in figure,uses two diodes to switch between main power supply and backup power supply.The M62001~M62008 are ICs that,in such memory backup operation,monitor in 2 steps each voltage on the V_{DD} line.



The ICs have an intelligent sequence such as substantial hysteresis action of RESET toward normal state at restoration of supply voltage,as well as 2-step detection in low power dissipation mode.

OPERATION IN DETAIL

1.Two Step Detection

The ICs perform 2-step detection of supply voltage and have 2 output pins ($\overline{INT}$ and $\overline{RESET}$).Although they have 2 comparators for 2-step detection,they differ significantly from such that are simply provided with independent detectors,because the $\overline{RESET}$ output signal is dependent at power-up and the like upon the $\overline{INT}$ output signal.

2.$\overline{INT}$ output (Detection of 4.45V and 4.25V)

The $\overline{INT}$ output at the power-up of supply voltage detects V_{SH} (4.45V/4.25V)to inform the microcomputer system of the fact that the supply voltage has reached its normal level.When the supply voltage drops from its normal level to V_{SL}(4.45V/4.25V)an interruption signal is output to alter the microcomputer system into RAM backup mode. The microcomputer at this point enters sleep state and secures memory by a stop command issued by the interruption signal.These detection voltage ,V_{SH} the rise,and V_{SL} the fall,of supply voltage,have a 100-mV hysteresis voltage between themselves.

$$V_{SH}-V_{SL}\fallingdotseq 100(mV)$$

3.$\overline{RESET}$ Output (Detection of 2.15V)

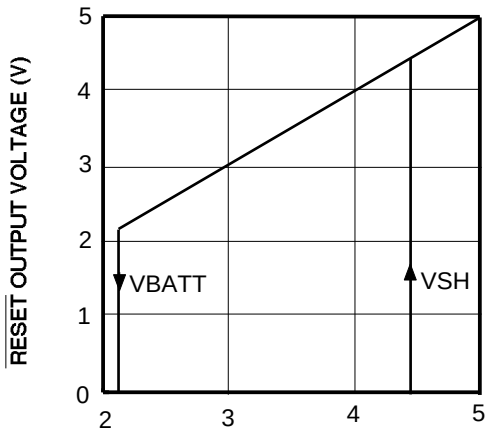
The $\overline{RESET}$ outputs a signal to prevent the microcomputer from malfunctioning due to a drop in supply voltage.
When powering up,$\overline{RESET}$ is kept at low level until the supply voltage reaches V_{SH}.If the supply voltage rises to V_{SH},$\overline{RESET}$ is set to high level.By inserting a capacitor between the Cd pin and GND,it is possible to produce a desired delay time (td).To set a delay time,equation below is used.

$$td\fallingdotseq 1.52X10^{5}\,XCd(sec)$$

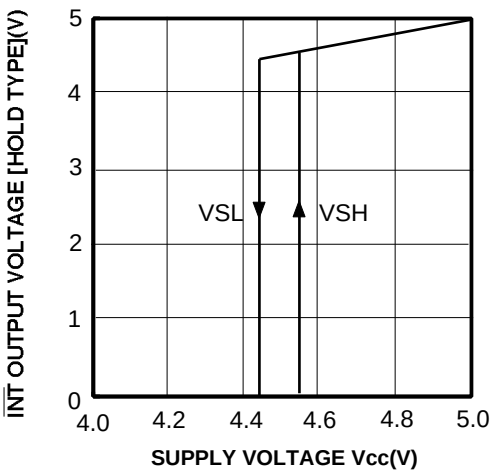
Once the supply voltage has exceeded V_{SH} and the $\overline{RESET}$ output is set to high level,$\overline{RESET}$ maintains the high level until the supply voltage drops to V_{BATT}.When the supply voltage drops to V_{BATT},$\overline{RESET}$ goes low thereby resetting and initializing the microcomputer.

The $\overline{RESET}$ output has a large hysteresis voltage of approximately 2V between the rise in supply voltage at power-up and its fall.

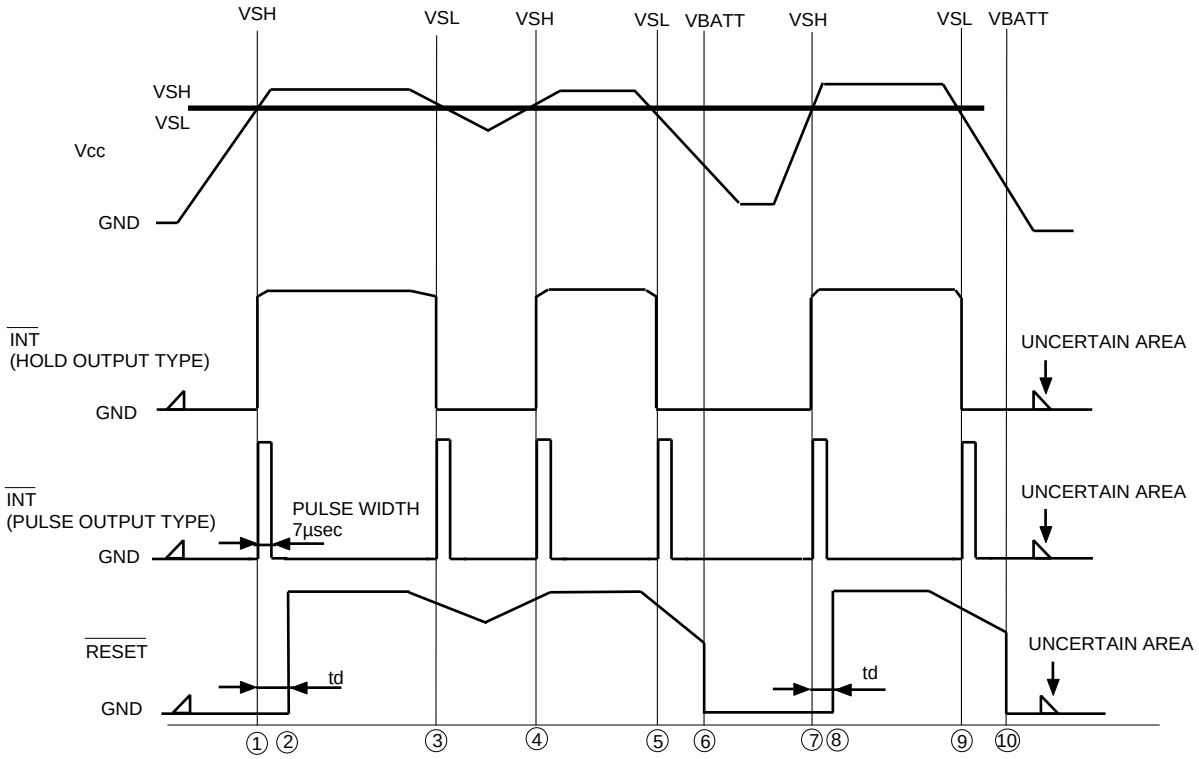
$\overline{RESET}$ OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



$\overline{INT}$ OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



OPERATION DESCRIPTION



① If Vcc rises to V_{SH}(4.55V/4.35V),the $\overline{INT}$ output it set to high level.
*1.A pulse is output if $\overline{INT}$ is of pulse output type.
② $\overline{RESET}$ goes high td(s) after V_{SH}
*td=1.52X105XC(sec)
③ If Vcc drops to V_{SH}(4.55V/4.25V),$\overline{INT}$ goes low.
*1.A pulse is output if $\overline{INT}$ is of pulse output type.
*2.The $\overline{RESET}$ output continues to be held high.
④ If Vcc returns to V_{SH},the $\overline{INT}$ output is set to high level.
⑤ Same as ③.
⑥ If Vcc becomes lower than V_{BATT}(2.15V),the $\overline{RESET}$ output is set to low thereby resetting the microcomputer and initializing system.
⑦ Same as ①.
⑧ Same as ②.
⑨ Same as ③ and ⑤.
⑩ Same as ⑥.

APPLICATION EXAMPLE