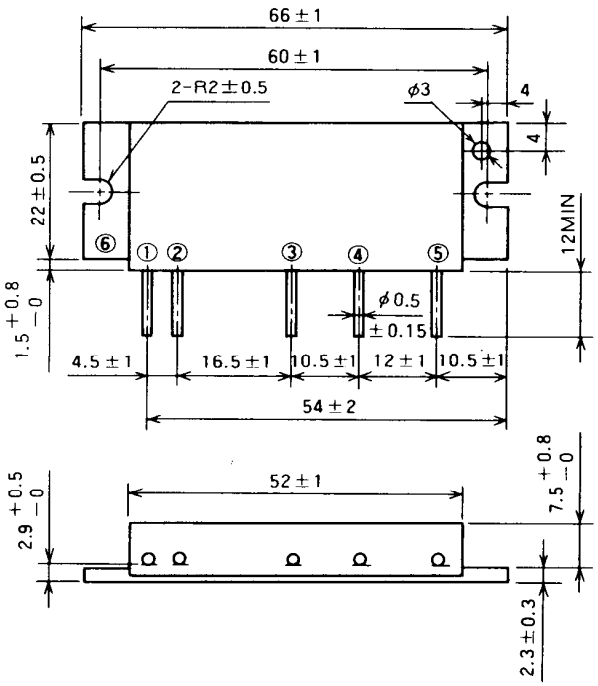
# M57789

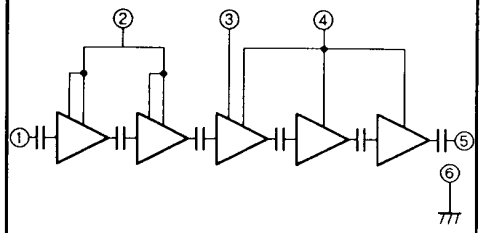
## 889-915MHz, 12.5V, 12W, FM MOBILE RADIO

**OUTLINE DRAWING** Dimensions in mm




H3

**BLOCK DIAGRAM**



PIN :
①Pin : RF INPUT
②Vcc1 : 1st. DC SUPPLY
③VBB : BASE BIAS SUPPLY
④Vcc2 : 2nd. DC SUPPLY
⑤Po : RF OUTPUT
⑥GND : FIN

**ABSOLUTE MAXIMUM RATINGS** (Tc = 25℃ unless otherwise noted)

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC1}$ | Supply voltage | | 13 | V |
| $V_{CC2}$ | | | 17 | V |
| $V_{BB}$ | Base bias | | 9 | V |
| Icc | Total current | $Z_G = Z_L = 50\ \Omega$ | 5 | A |
| $P_{in(max)}$ | Input power | $Z_G = Z_L = 50\ \Omega$, $V_{CC1} \leqq 12.5V$ | 10 | mW |
| $P_{o(max)}$ | Output power | $Z_G = Z_L = 50\ \Omega$ | 20 | W |
| $T_{C(OP)}$ | Operation case temperature | | −30 to 110 | ℃ |
| $T_{stg}$ | Storage temperature | | −40 to 110 | ℃ |

Note. Above parameters are guaranteed independently.

**ELECTRICAL CHARACTERISTICS** (Tc = 25℃ unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| f | Frequency range | $V_{CC1} = V_{CC2} = 12.5$, $V_{BB} = 8V$<br>$P_{in} = 5mW$<br>$Z_G = Z_L = 50\ \Omega$ | 889 | 915 | MHz |
| Po | Output power | | 12 | | W |
| $\eta_T$ | Total efficiency | | 30 | | % |
| 2fo | 2nd. harmonic | | | −30 | dBc |
| $\rho_{in}$ | Input VSWR | | | 2.8 | − |
| − | Load VSWR tolerance | $V_{CC1}$=12.5V, $V_{CC2}$=15.2V, $V_{BB}$=8V<br>Po = 12W($P_{in}$ : controlled), $Z_G$ = 50Ω<br>Load VSWR=20:1(All phase), 5sec. | No degradation or destroy | | − |

Note. Above parameters, ratings, limits and conditions are subject to change.



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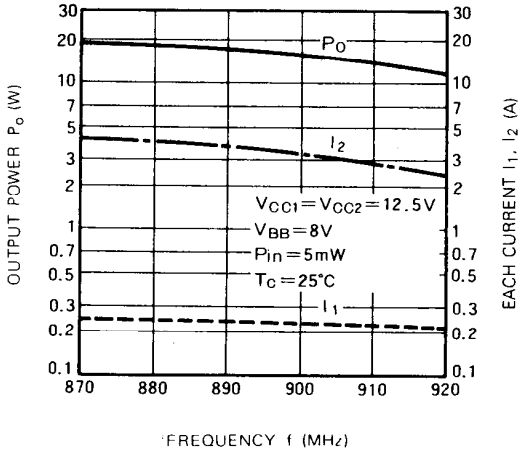
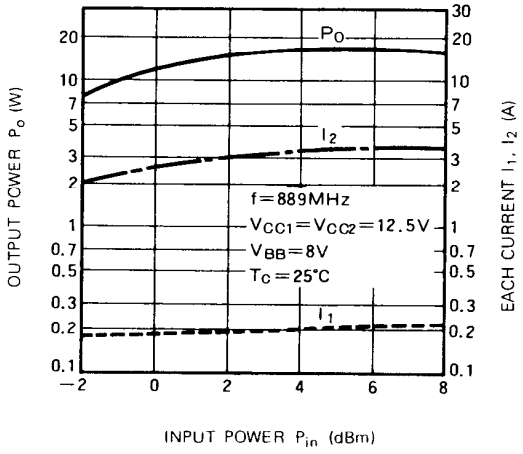
## TYPICAL PERFORMANCE DATA

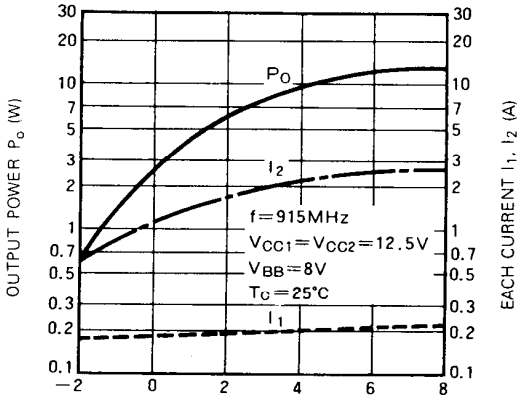
### OUTPUT POWER, EACH CURRENT VS. FREQUENCY



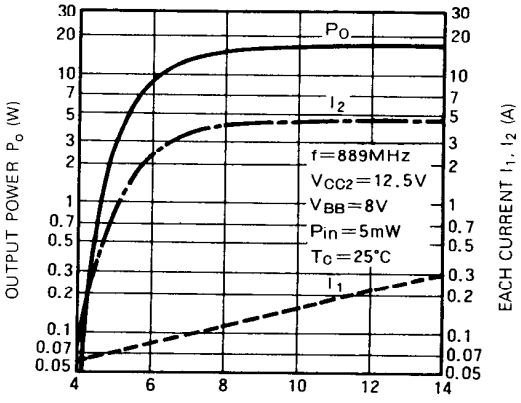

### OUTPUT POWER, EACH CURRENT VS. INPUT POWER



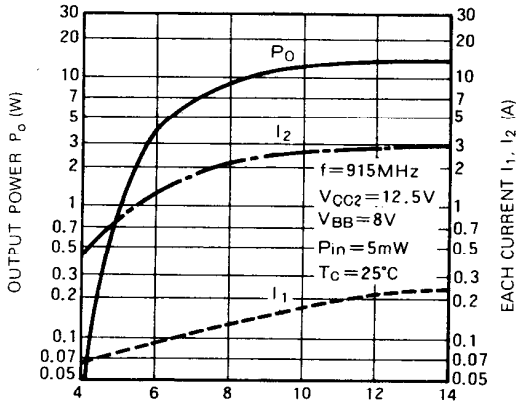

### OUTPUT POWER, EACH CURRENT VS. INPUT POWER




### OUTPUT POWER, EACH CURRENT VS. 1st DC SUPPLY VOLTAGE




### OUTPUT POWER, EACH CURRENT VS. 1st DC SUPPLY VOLTAGE



## DESIGN CONSIDERATION OF HEAT RADIATION

Please refer to the following consideration when designing a heat sink.

### 1. Junction temperature of incorporated transistors at standard operation.

(1) Thermal resistances between junction of incorporated transistors and case are shown in the followings.

a) First stage transistor
$R_{th(j-c)1}$ = 20°C/W (Typ.)

b) Second stage transistor
$R_{th(j-c)2}$ = 17.5°C/W (Typ.)

c) Third stage transistor
$R_{th(j-c)3}$ = 15°C/W (Typ.)

d) Fourth stage transistor
$R_{th(j-c)4}$ = 7.5°C/W (Typ.)

e) Final stage transistor
$R_{th(j-c)5}$ = 3.75°C/W (Typ.)

(2) $V_{CC}$, $I_T$, RF input & output power conditions at standard operation for each stage transistors are estimated as follows.
$P_O$ = 12W, $V_{CC1} = V_{CC2} = V_{CC3}$ = 12.5V, $P_{in}$ = 5mW,
$\eta_T$ = 30% (minimum ratings),
$I_1$ = 0.23A (Total current from 1st stage to 2nd stage)
$I_2$ = 2.97A (Total current from 3rd stage to 5th stage)
The conditions at standard operation for each stage transistors are shown in Table 1.

- Junction temperature of the first stage transistor
$T_{j1} = (V_{CC1} \times I_{T1} - P_{O1} + P_{in}) \times R_{th(j-c)1} + T_C$ (Note 1)
$= (12.5 \times 0.06 - 0.02 + 0.005) \times 20 + T_C$
$= 14.6 + T_C$ (°C)

Note 1: Case temperature of device

- Junction temperature of the second stage transistor
$T_{j2} = (V_{CC1} \times I_{T2} - P_{O2} + P_{O1}) \times R_{th(j-c)2} + T_C$
$= (12.5 \times 0.17 - 0.4 + 0.03) \times 17.5 + T_C$
$= 30.7 + T_C$ (°C)
- Junction temperature of the third stage transistor
$T_{j3} = (V_{CC2} \times I_{T3} - P_{O3} + P_{O2}) \times R_{th(j-c)3} + T_C$
$= (12.5 \times 0.28 - 1.3 + 0.4) \times 15 + T_C$
$= 39.0 + T_C$ (°C)
- Junction temperature of the fourth stage transistor
$T_{j4} = (V_{CC2} \times I_{T4} - P_{O4} + P_{O3}) \times R_{th(j-c)4} + T_C$
$= (12.5 \times 0.77 - 4.8 + 1.3) \times 7.5 + T_C$
$= 45.9 + T_C$ (°C)
- Junction temperature of the final stage transistor
$T_{j5} = (V_{CC3} \times I_{T5} - P_{O5} + P_{O4}) \times R_{th(j-c)5} + T_C$
$= (12.5 \times 1.92 - 12 + 4.8) \times 3.75 + T_C$
$= 63.0 + T_C$ (°C)

### 2. Heating sink design

In thermal design of heat sink, keep the case temperature below 90°C at output power $P_O$ = 12W and ambient temperatue = 60°C.

**Table 1: The conditions at standard operation**

| Stage | $V_{CC}$ (V) | $I_T$ (mA) | $P_{in}$ (mW) | $P_O$ (mW) |
|---|---|---|---|---|
| 1st | 12.5 | 60 | 5 | 30 |
| 2nd | 12.5 | 170 | 30 | 400 |
| 3rd | 12.5 | 280 | 400 | 1300 |
| 4th | 12.5 | 770 | 1300 | 4800 |
| 5th | 12.5 | 1920 | 4800 | 12000 |

The thermal resistance $R_{th(c-a)}$ (Note 2) of the heat sink to realize this:

$$R_{th(c-a)} = \frac{T_C - T_a}{(P_O/\eta_T) - P_P + P_{in}} = \frac{90 - 60}{(12/0.3 - 12 + 0.001)}$$

$= 1.00$ (°C/W)

Note 2: Including the contact thermal resistance between device and heat sink

Mounting the device on the heat sink with above thermal resistance, junction temperatures of each transistor become;
$T_{j1}$ = 105°C, $T_{j2}$ = 121°C, $T_{j3}$ = 129°C, $T_{j4}$ = 136°C,
$T_{j5}$ = 153°C at $T_a$ = 60°C, $T_C$ = 90°C.
Since the annual average of ambient temperature is 30°C, junction temperatures of each transistor become;
$T_{j1}$ = 75°C, $T_{j2}$ = 91°C, $T_{j3}$ = 99°C, $T_{j4}$ = 106°C,
$T_{j5}$ = 123°C.
As the maximum junction temperature of these incorporated transistors $T_{jmax}$ are 153°C, application under fully derated condition is ensured.