

Technical drawing of a mechanical part, showing a top view and a side view. The top view is a rectangle with a width of 66 ± 1 and a height of 22 ± 0.5 . It features a central slot with a width of 12 ± 1 and a depth of 16.5 ± 1 . The slot is flanked by two vertical sections, each with a width of 12 ± 1 . The total width of the top view is 66 ± 1 . The side view shows a rectangular profile with a width of 52 ± 1 and a height of 23 ± 0.3 . The side view also shows a central slot with a width of 12 ± 1 and a depth of 16.5 ± 1 . The total width of the side view is 52 ± 1 . The drawing includes various dimension lines and labels, such as $2-R2 \pm 0.3$ for the rounded corners and $\phi 3$ for the hole diameter. The part is labeled with numbers 1 through 5, indicating specific features or sections.

H3

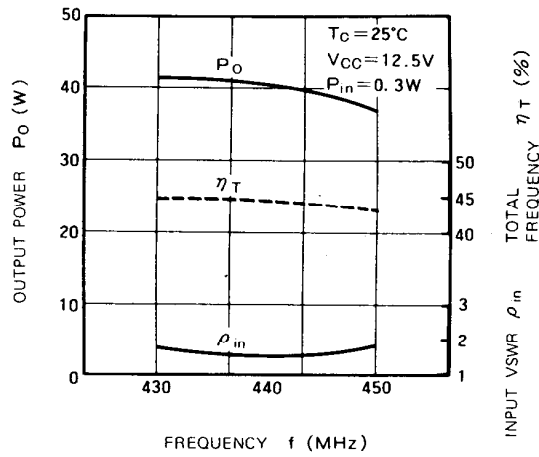
①Pin : RF INPUT
②Vcc1 : 1st. DC SUPPLY
③Vcc2 : 2nd. DC SUPPLY
④Vcc3 : 3rd. DC SUPPLY
⑤Po : RF OUTPUT
⑥GND : FIN

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		17	V
I _{CC}	Total current		10	A
P _{in(max)}	Input power	Z _G = Z _L = 50 Ω	0.6	W
P _{O(max)}	Output power	Z _G = Z _L = 50 Ω	40	W
T _{C(OP)}	Operation case temperature		− 30 to 110	°C
T _{stg}	Storage temperature		− 40 to 110	°C

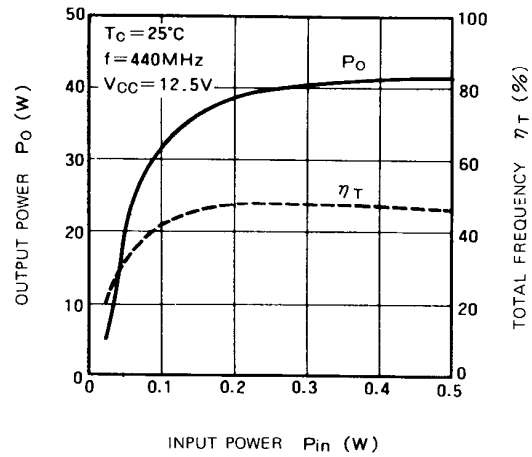
Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
f	Frequency range	$P_{in} = 0.3W$ $V_{CC} = 12.5V$ $Z_G = Z_L = 50 \Omega$	430	450	MHz
P _o	Output power		30		W
η_T	Total efficiency		40		%
2f _o	2nd. harmonic			- 30	dBc
3f _o	3rd. harmonic			- 30	dBc
ρ_{in}	Input VSWR			2.8	-
-	Load VSWR tolerance	$V_{CC} = 15.2V$, $P_o = 30W$ (P_{in} : controlled) Load VSWR=20:1 (All phase), 2sec. $Z_G = 50 \Omega$	No degradation or destroy		-

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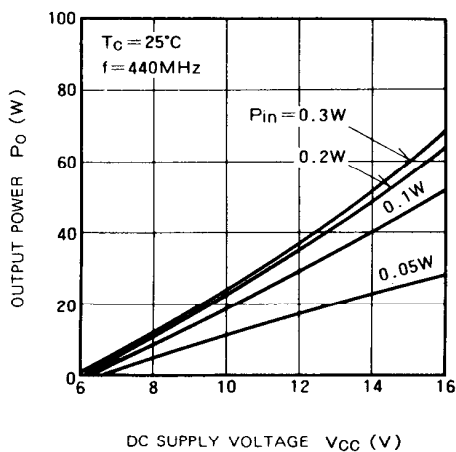
OUTPUT POWER, TOTAL EFFICIENCY,
INPUT VSWR VS. FREQUENCY (M57729)



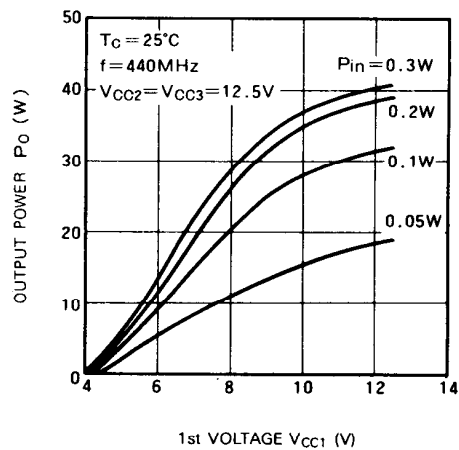
OUTPUT POWER, TOTAL EFFICIENCY,
VS. INPUT POWER (M57729)



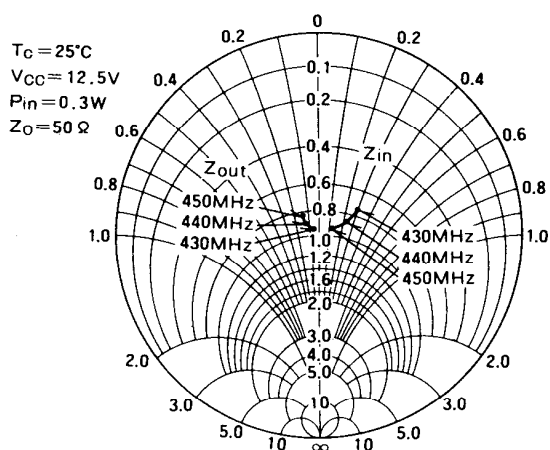
OUTPUT POWER VS. DC SUPPLY
VOLTAGE (M57729)



OUTPUT POWER VS. 1st
VOLTAGE (M57729)



INPUT IMPEDANCE, OUTPUT
IMPEDANCE VS. FREQUENCY
(M57729)



DESIGN CONSIDERATION OF HEAT RADIATION

Please refer to following consideration when designing heat sink.

1. Junction temperature of incorporated transistors at standard operation.

(1) Thermal resistance between junction and package of incorporated transistors.

a) First stage transistor

$$R_{th(j-c)1} = 12^{\circ}\text{C/W (Typ.)}$$

b) Second stage transistor

$$R_{th(j-c)2} = 4^{\circ}\text{C/W (Typ.)}$$

c) Final stage transistor

$$R_{th(j-c)3} = 2^{\circ}\text{C/W (Typ.)}$$

(2) Junction temperature of incorporated transistors at standard operation.

- Conditions for standard operation.

$P_O = 30\text{W}$, $V_{CC} = 12.5\text{V}$, $P_{in} = 0.3\text{W}$, $\eta_T = 40\%$ (minimum rating), P_{O1} (Note 1) = 2.0W , P_{O2} (2) = 8.0W , $I_T = 6.0\text{A}$ (I_{T1} (3) = 0.35A , I_{T2} (4) = 1.32A , I_{T3} (5) = 4.33A)

Note 1: Output power of the first stage transistor

Note 2: Output power of the second stage transistor

Note 3: Circuit current of the first stage transistor

Note 4: Circuit current of the second stage transistor

Note 5: Circuit current of the final stage transistor

- Junction temperature of the first stage transistor

$$\begin{aligned} T_{j1} &= (V_{CC} \times I_{T1} - P_{O1} + P_{in}) \times R_{th(j-c)1} + T_C^{(6)} \\ &= (12.5 \times 0.35 - 2.0 + 0.3) \times 12 + T_C \\ &= 32 + T_C (^{\circ}\text{C}) \end{aligned}$$

Note 6: Package temperature of device

- Junction temperature of the second stage transistor

$$\begin{aligned} T_{j2} &= (V_{CC} \times I_{T2} - P_{O2} + P_{O1}) \times R_{th(j-c)2} + T_C \\ &= (12.5 \times 1.32 - 8.0 + 2.0) \times 4 + T_C \\ &= 42 + T_C (^{\circ}\text{C}) \end{aligned}$$

- Junction temperature of the final stage transistor

$$\begin{aligned} T_{j3} &= (V_{CC} \times I_{T3} - P_O + P_{O2}) \times R_{th(j-c)3} + T_C \\ &= (12.5 \times 4.33 - 30 + 8) \times 2 + T_C \\ &= 64 + T_C (^{\circ}\text{C}) \end{aligned}$$

2. Heat sink design

In thermal design of heat sink, try to keep the package temperature at the upper limit of the operating ambient temperature (normally $T_a = 60^{\circ}\text{C}$) and at the output power of 7W below 90°C .

The thermal resistance $R_{th(c-a)}^{(7)}$ of the heat sink to realize this:

$$\begin{aligned} R_{th(c-a)} &= \frac{T_c - T_a}{(P_O/\eta_T) - P_O + P_{in}} = \frac{90 - 60}{(30/0.4) - 30 + 0.3} \\ &= 0.66 (^{\circ}\text{C/W}) \end{aligned}$$

Note 7: Inclusive of the contact thermal resistance between device and heat sink

Mounting the heat sink of the above thermal resistance on the device,

$$T_{j1} = 122^{\circ}\text{C}, T_{j2} = 132^{\circ}\text{C}, T_{j3} = 155^{\circ}\text{C} \text{ at } T_a = 60^{\circ}\text{C}, T_c = 90^{\circ}\text{C}.$$

In the annual average of ambient temperature is 30°C ,

$$T_{j1} = 92^{\circ}\text{C}, T_{j2} = 102^{\circ}\text{C}, T_{j3} = 125^{\circ}\text{C}.$$

As the maximum junction temperature of these incorporated transistors T_{jmax} are 175°C , application under fully derated condition is ensured.