

M56620AP**Bi-CMOS 8-BIT PARALLEL-INPUT LATCHED DRIVER****DESCRIPTION**

The M56620AP is a semiconductor integrated circuit fabricated using Bi-CMOS technology. It contains bipolar 8 output drivers of CMOS latch.

FEATURES

- Enable input for output control
- Low supply current $I_{CC} \leq 10\mu A$ at standby
- Input level is compatible with standard CMOS
- Driver: Withstand voltage $BV_{CEO} \geq 50V$
Large drive current ($I_{O(max)} = 500mA$)
- Wide operating temperature range $T_a = -20 - +75^\circ C$

APPLICATION

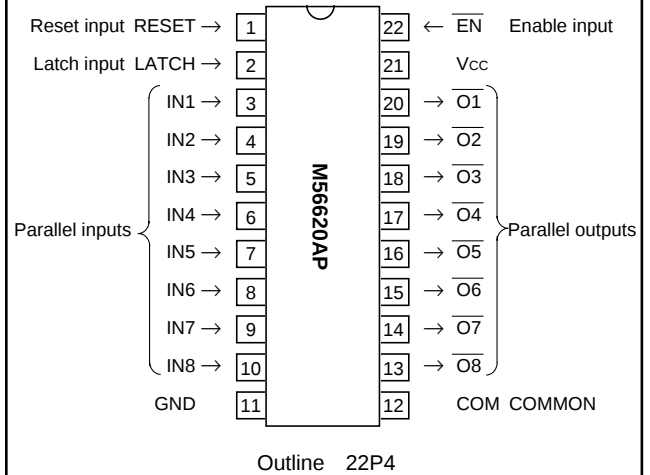
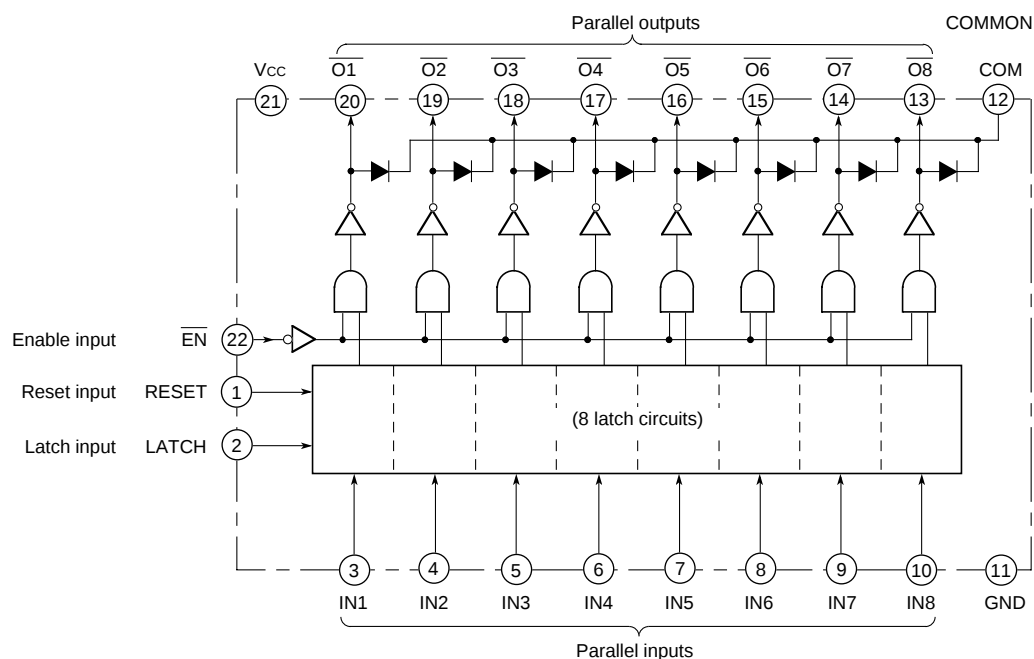
Thermal printer head dot driver, Relay driver, Solenoid driver

FUNCTION

When data is applied to inputs IN1 – IN8 and LATCH input is set to “H”, the data will be latched with the truth table. Note that when an “H” signal is applied to the RESET input, the latch will maintain the reset state.

When the $\overline{EN}$ input is set to “L” and the data maintained in the latch are “H”, the corresponding output will be ON and become “L”.

When both the LATCH and RESET inputs are “L”, the latch will maintain the prior state irrespective of input signals IN1 – IN8.

PIN CONFIGURATION (TOP VIEW)**BLOCK DIAGRAM**

M56620AP

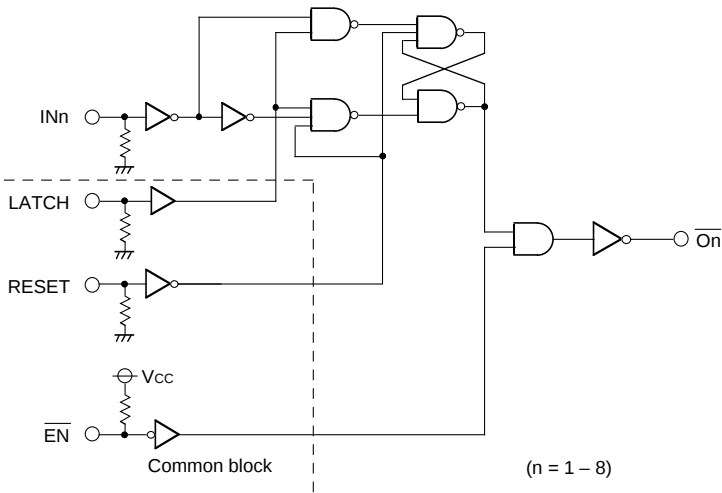
Bi-CMOS 8-BIT PARALLEL-INPUT LATCHED DRIVER

TRUTH TABLE

Input				Output $\overline{\text{On}}$	
INn	LATCH	RESET	$\overline{\text{EN}}$	t-1	t
L	H	L	L	x	H
H	H	L	L	x	L
x	x	H	x	x	H
x	x	x	H	x	H
x	L	L	L	L	L
x	L	L	L	H	H

L: low level
H: high level
x: low level or high level
t-1: previous state
t: current state
H output: OFF state
L output: ON state

LOGIC DIAGRAM (One circuit)

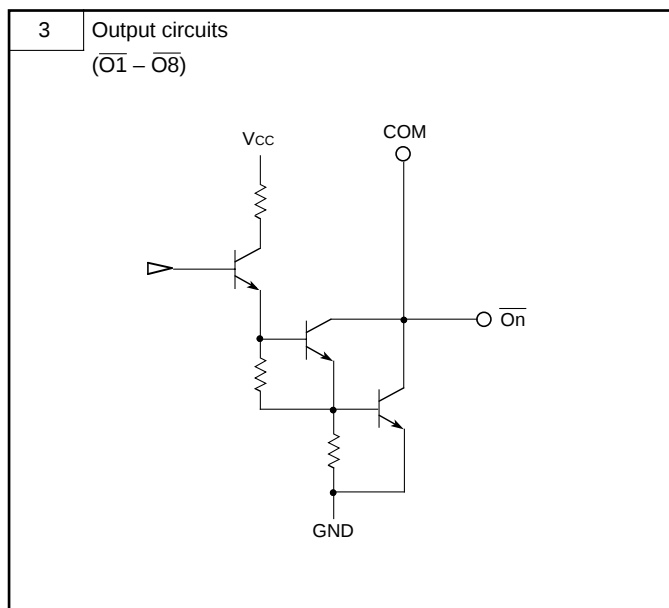


INPUT/OUTPUT EQUIVALENT CIRCUITS

1	Input circuits (INn, LATCH, RESET)	2	Input circuit ($\overline{\text{EN}}$)

M56620AP

Bi-CMOS 8-BIT PARALLEL-INPUT LATCHED DRIVER



ABSOLUTE MAXIMUM RATINGS (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.3 – +8	V
V _I	Input voltage		-0.3 – V _{CC} +0.3	V
V _O	Output voltage	Output: OFF	0 – +50	V
I _O	Output current	Output: ON	500	mA
P _d	Power dissipation	Ta=25°C	1.25	W
T _{opr}	Operating temperature		-20 – 75	°C
T _{stg}	Storage temperature		-55 – 125	°C

RECOMMENDED OPERATING CONDITION (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply voltage		4	5	6	V
V _O	Output apply voltage	Output: OFF			50	V
I _O	Output current (per circuit)	All outputs go in ON state simultaneously. Duty cycle < 15%			350	mA

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=5V, unless otherwise noted)

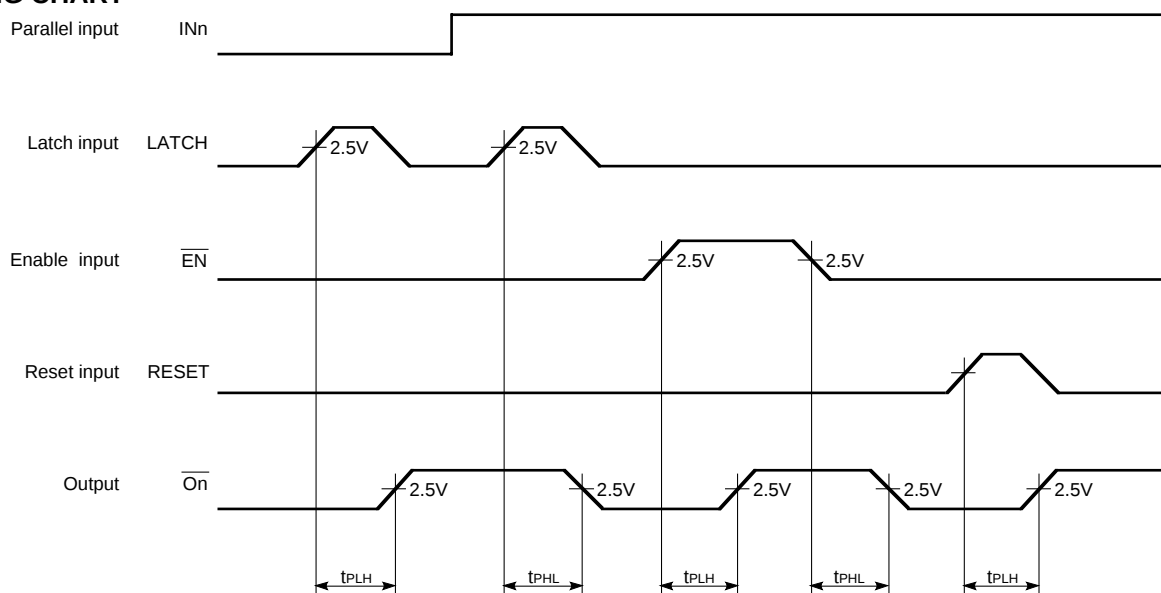
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{IH}	High-level input voltage	Ta=-20 – 75°C	0.7V _{CC}		V _{CC}	V
V _{IL}	Low-level input voltage		0		0.3V _{CC}	V
R _{IN}	Input resistance	V _{IN} =1.5 – 3.5V	50		2000	kΩ
V _{OL1}	Low-level output voltage	I _{OL} =100mA			1.1	V
V _{OL2}		I _{OL} =200mA			1.3	V
V _{OL3}		I _{OL} =350mA			1.6	V
I _{OLK}	Output leak current	V _O =50V			50	μA
V _F	Clamping diode forward voltage	I _F =350V			2	V
I _R	Clamping diode reverse current	V _R =50V			50	μA
I _{CC1}	Supply current	EN=5V, All other inputs = 0V			10	μA
I _{CC2}		EN=0V, One output is ON.		1.0	1.5	mA

M56620AP

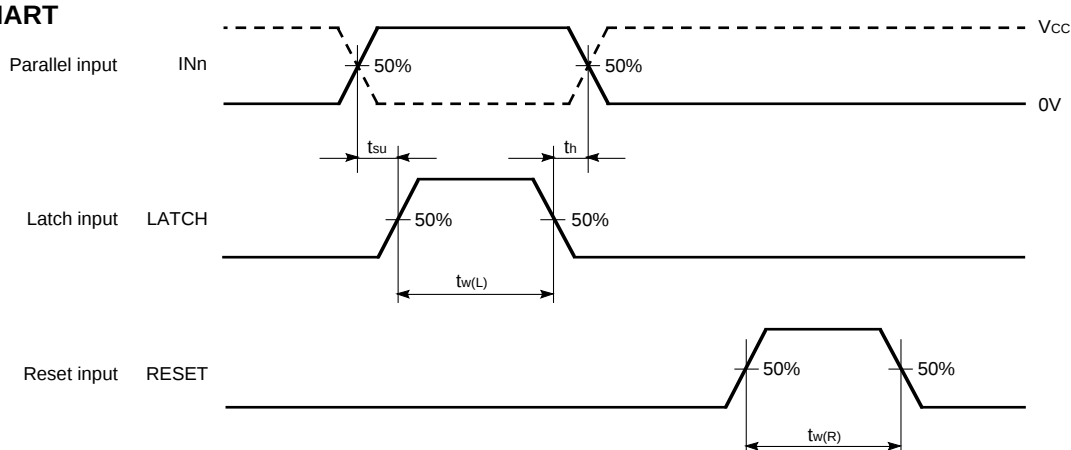
Bi-CMOS 8-BIT PARALLEL-INPUT LATCHED DRIVER

SWITCHING CHARACTERISTICS (Ta=25°C, Vcc=5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t _{PLH}	Low-to-high-level output propagation time From input LATCH to output $\overline{\text{On}}$	V _{IH} =5V V _{IL} =0V R _L =100Ω C _L =15pF			5	μs
t _{PHL}	High-to-low-level output propagation time From input LATCH to output $\overline{\text{On}}$				0.5	μs
t _{PLH}	Low-to-high-level output propagation time From input $\overline{\text{EN}}$ to output $\overline{\text{On}}$				5	μs
t _{PHL}	High-to-low-level output propagation time From input $\overline{\text{EN}}$ to output $\overline{\text{On}}$				0.5	μs
t _{PLH}	Low-to-high-level output propagation time From input RESET to output $\overline{\text{On}}$				5	μs

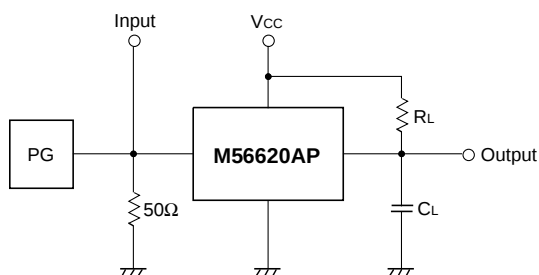
TIMING CHART**TIMING REQUIREMENTS** (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t _{w(L)}	Latch pulse width		0.1			μs
t _{w(R)}	Reset pulse width		0.1			μs
t _{su}	Data setup time		0.05			μs
t _h	Data hold time		0.1			μs

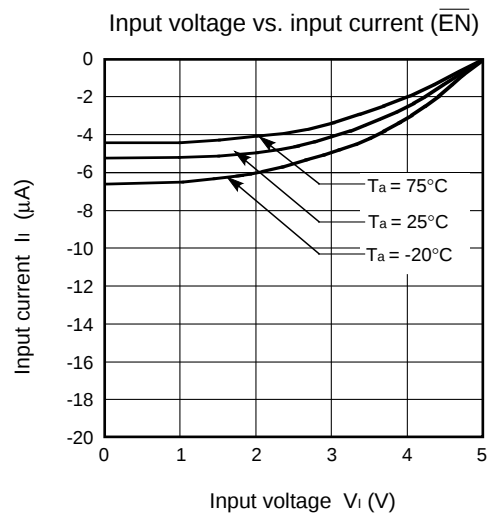
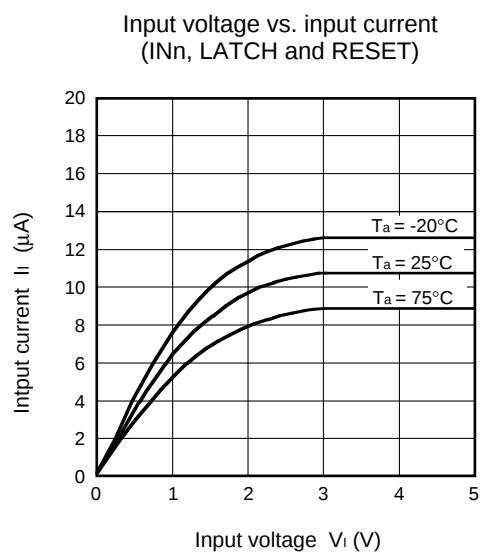
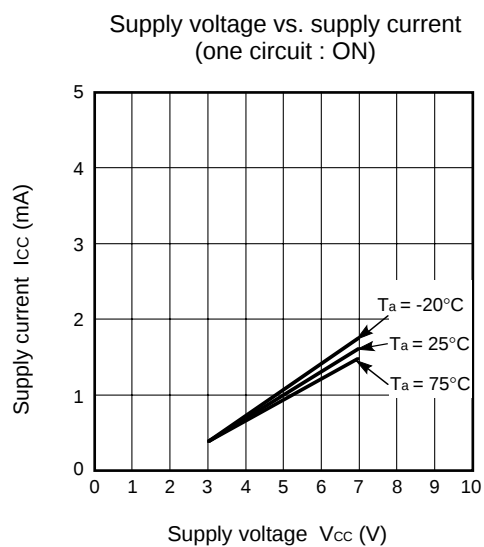
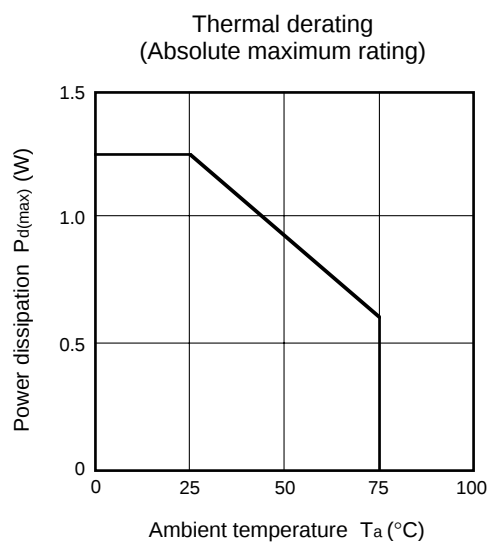
TIMING CHART

M56620AP

Bi-CMOS 8-BIT PARALLEL-INPUT LATCHED DRIVER

TEST CIRCUIT

- The input waveform: $t_r \leq 20\text{ns}$, $t_f \leq 20\text{ns}$
- The capacitance C_L includes the wiring stray capacitance and probe input capacitance.

TYPICAL CHARACTERISTICS

M56620AP

Bi-CMOS 8-BIT PARALLEL-INPUT LATCHED DRIVER

