M54972P/FP

Bi-CMOS 8-BIT SERIAL-INPUT LATCHED DRIVER

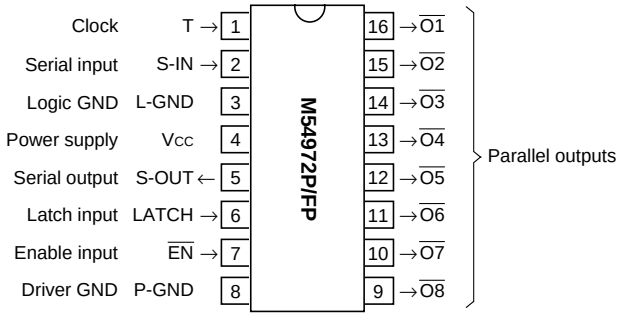
DESCRIPTION

The M54972 is a semiconductor integrated circuit consisting of 8 stages of CMOS shift registers and latches with serial inputs and serial or parallel outputs. It is based on Bi-CMOS process technology, and has 8 bipolar drivers at the parallel outputs.

FEATURES

- Serial input and serial or parallel output
- Serial output enables cascade connection
- Built-in latch for each stage
- Enable input provides output control
- Low supply current (standby current $I_{CC} \leq 10\mu A$)
- Serial I/O level is compatible with typical CMOS devices
- Driver features: High withstand voltage ($BV_{CEO} \geq 30V$)
  Capable of large drive currents ($I_{O(max)}$=300mA)
  Low output saturation voltage V_{OL} < 0.6V at I_O=300mA
- Wide operating temperature range T_a=-20 – +75°C

PIN CONFIGURATION (TOP VIEW)



Outline 16P4(P)
16P2N-A(FP)

APPLICATION

Dot drivers for thermal print heads. Serial/parallel conversion. Drivers for relays and solenoids.

FUNCTION

The M54972 consists of 8 stages of D-type flip flops connected to 8 latches.

Data is input to serial input S-IN, and clock pulses are input to clock input T. When the clock changes from low to high, the input data enters the first shift register and data already in the shift registers is shifted sequentially.

The serial output S-OUT is used to connect multiple M54972 to expand the number of parallel outputs. S-OUT is connected to S-IN of the next stage.

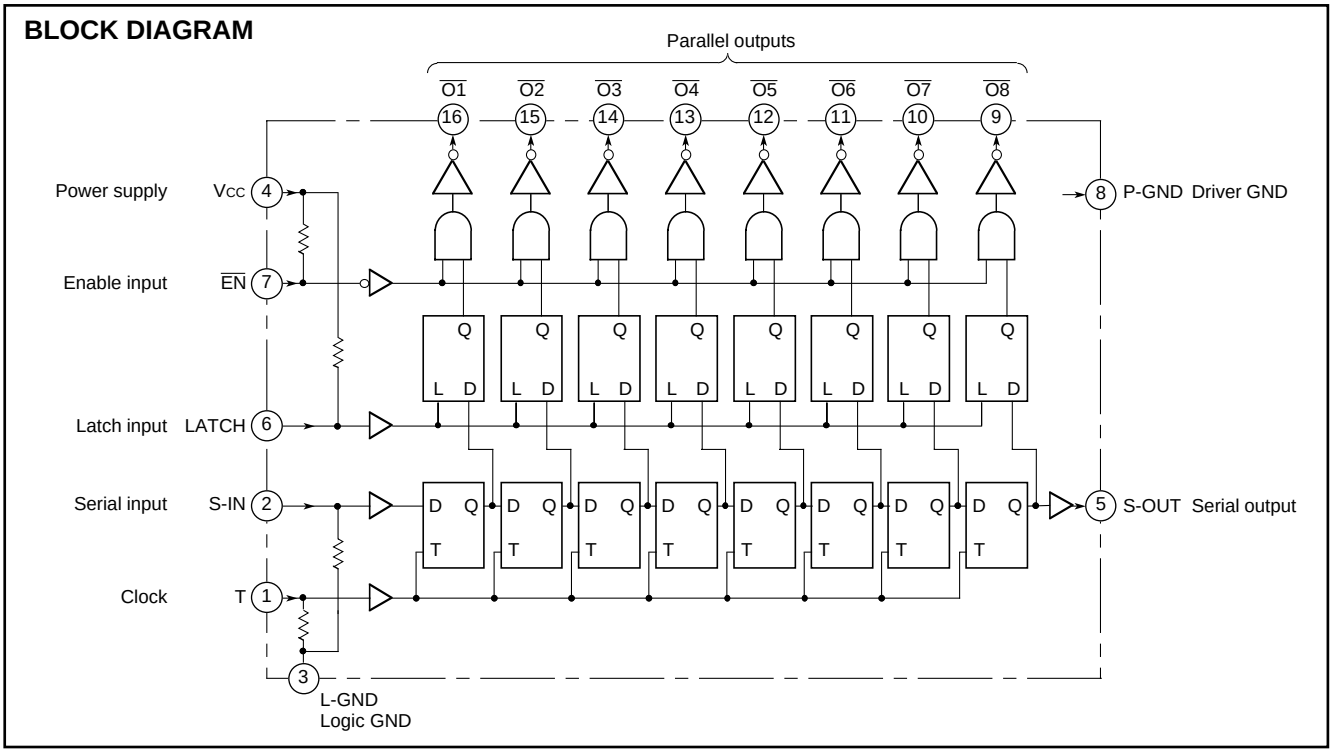
For parallel output. When the clock pulse changes from low to high, latch input (LATCH) is high and output enable input ($\overline{EN}$) is low the serial input data at S-IN appears at output $\overline{O1}$ and the other data already present is shifted sequentially to outputs $\overline{O2}$ through $\overline{O8}$.

The parallel outputs are inverted.

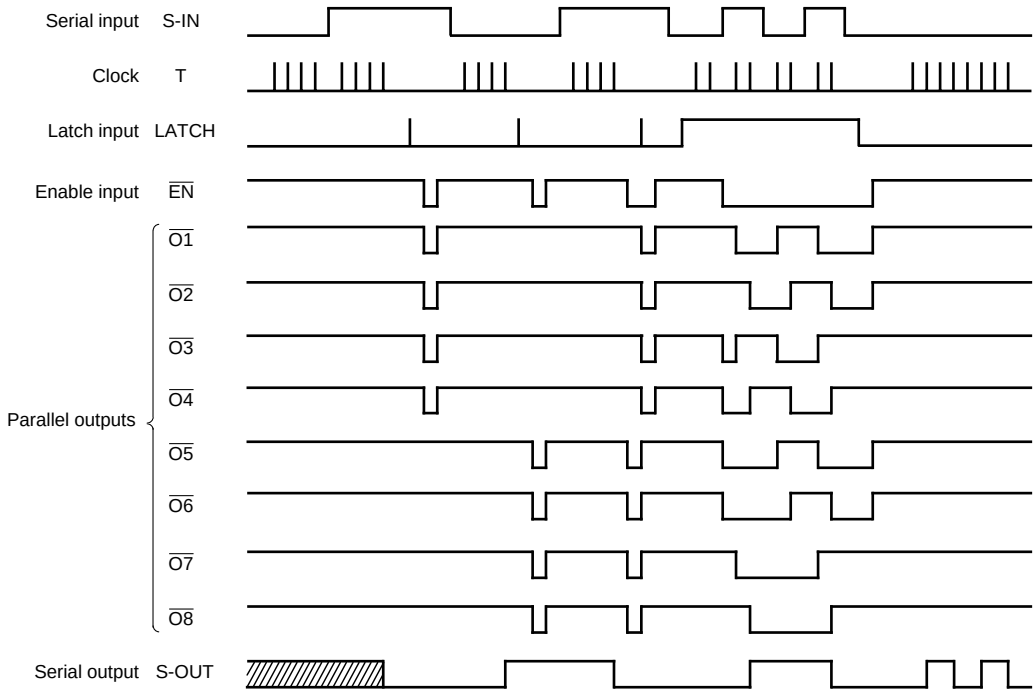
When the latch input is held low, the latch retains the stored data. When the $\overline{EN}$ input is high, outputs $\overline{O1}$ through $\overline{O8}$ all turn off. As the internal logic is unstable when the power is turned on, the $\overline{EN}$ input should be kept high (setting outputs $\overline{O1}$ through $\overline{O8}$ off) until input data is set and the internal logic is initialized.

L-GND is the GND of CMOS logic circuit and P-GND is the GND of output driver circuits $\overline{O1}$ through $\overline{O8}$ which employ bipolar transistors capable of large drive currents.

BLOCK DIAGRAM



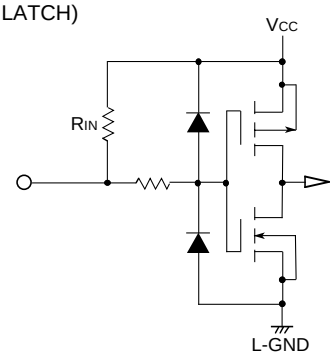
TIMING CHART



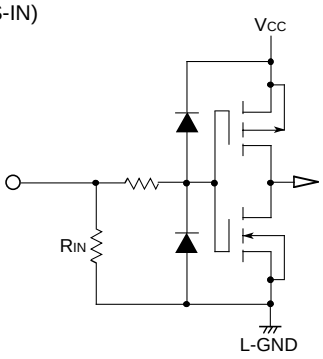
*The shaded area shows the unstable state.

INPUT/OUTPUT CIRCUIT DIAGRAM

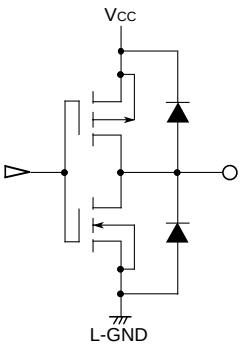
1 Inputs with pullup resistors ($\overline{EN}$, LATCH)



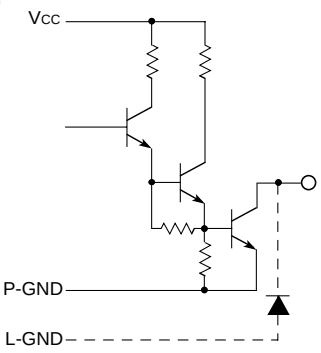
2 Inputs with pulldown resistors (T, S-IN)



3 Serial output (S-OUT)



4 Parallel outputs ($\overline{O1}$ – $\overline{O8}$)



ABSOLUTE MAXIMUM RATINGS (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Conditions		Ratings	Unit
V_{CC}	Supply voltage			-0.5 – +8	V
V_I	Input voltage			-0.5 – V_{CC}+0.5	V
V_O	Output voltage	S-OUT		-0.5 – V_{CC}+0.5	V
		$\overline{O1}$ – $\overline{O8}$: OFF		-0.5 – +30	
I_O	Output current	$\overline{O1}$ – $\overline{O8}$: ON		300	mA
P_d	Power dissipation	T_a=25°C	M54972P	1.25	W
			M54972FP	0.8	
T_{opr}	Operating temperature			-20 – 75	°C
T_{stg}	Storage temperature			-55 – 125	°C

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage			4	5	6	V
V_O	Applied output voltage	$\overline{O1}$ – $\overline{O8}$: OFF				30	V
I_O	Output current (per circuit)	$\overline{O1}$ – $\overline{O8}$: ON, Duty cycle < 35%	M54972P			300	mA
		$\overline{O1}$ – $\overline{O8}$: ON, Duty cycle < 70%				200	
		$\overline{O1}$ – $\overline{O8}$: ON, Duty cycle < 15%	M54972FP			200	

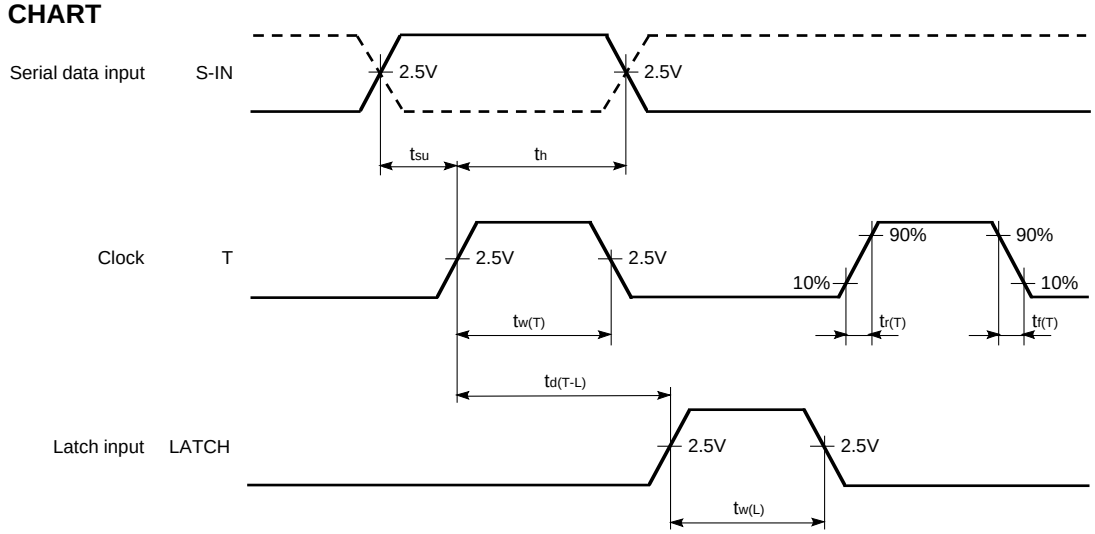
ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=5V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{IH}	High-level input voltage		T_a=-20 – 75°C, V_{CC}=4 – 6V	0.7V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.3V_{CC}	V
I_{IH}	High-level input current	T, S-IN	V_{IH}=5V			100	µA
I_{IL}	Low-level input current	$\overline{EN}$, LATCH	V_{IL}=0V			-100	µA
R_{IN}	Input resistance			50			kΩ
V_{OH}	High-level output voltage	S-OUT	|I_O|≤1µA	4.9			V
V_{OL}	Low-level output voltage	S-OUT				0.1	V
I_{OH}	High-level output current	S-OUT	V_{OH}=4.5V	-100			µA
I_{OL}	Low-level output current	S-OUT	V_{OL}=0.4V	400			µA
V_{OL1}	Low-level output voltage	$\overline{O1}$ – $\overline{O8}$	I_{OL}=200mA			0.5	V
V_{OL2}							
V_{OL3}			I_{OL}=300mA			0.6	V
I_{OLK}	Output leak current	$\overline{O1}$ – $\overline{O8}$	V_O=30V ($\overline{O1}$ – $\overline{O8}$: OFF)			50	µA
I_{CC1}	Supply current		Input: open, All driver outputs: OFF			10	µA
I_{CC2}			One driver output is ON.			7.5	mA

TIMING REQUIREMENTS (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$f_{(T)}$	Clock frequency	Input duty cycle: 40 – 60%			2	MHz
$t_{w(T)}$	Clock pulse width		200			ns
$t_{w(L)}$	Latch pulse width		200			ns
t_{su}	Data setup time		100			ns
t_h	Data hold time		100			ns
$t_{d(T-L)}$	Clock-latch time		400			ns
$t_{r(T)}$	Clock pulse rise time				500	ns
$t_{f(T)}$	Clock pulse fall time				500	ns

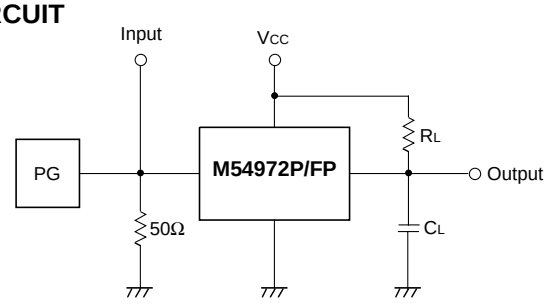
TIMING CHART



SWITCHING CHARACTERISTICS (Ta=25°C, VCC=5V, unless otherwise noted)

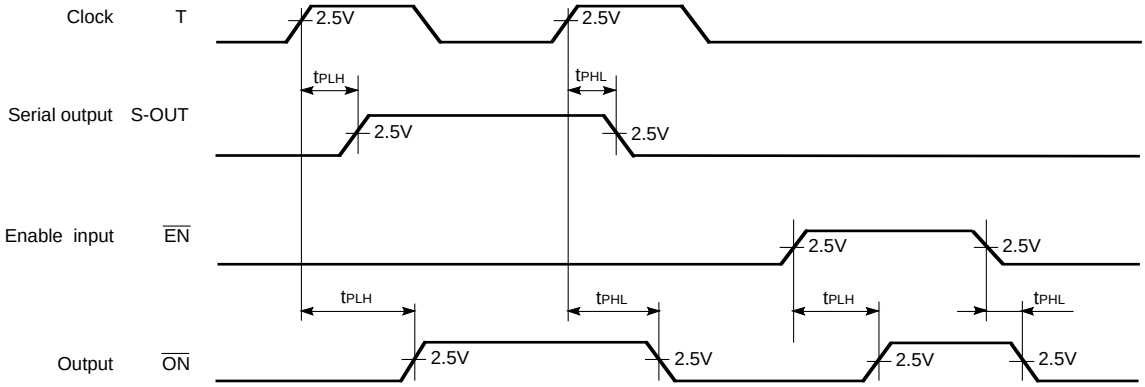
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{PLH}	Low-to-high-level output propagation time From input T to output S-OUT	V_{IH}=5V V_{IL}=0V R_L(S-OUT)=∞ R_L($\overline{ON}$)=100Ω (N=1–8) C_L=15pF			0.3	µs
t_{PHL}	High-to-low-level output propagation time From input T to output S-OUT				0.3	µs
t_{PLH}	Low-to-high-level output propagation time From input T to output $\overline{ON}$				10	µs
t_{PHL}	High-to-low-level output propagation time From input T to output $\overline{ON}$				5	µs
t_{PLH}	Low-to-high-level output propagation time From input $\overline{EN}$ to output $\overline{ON}$				10	µs
t_{PHL}	High-to-low-level output propagation time From input $\overline{EN}$ to output $\overline{ON}$				5	µs

TEST CIRCUIT



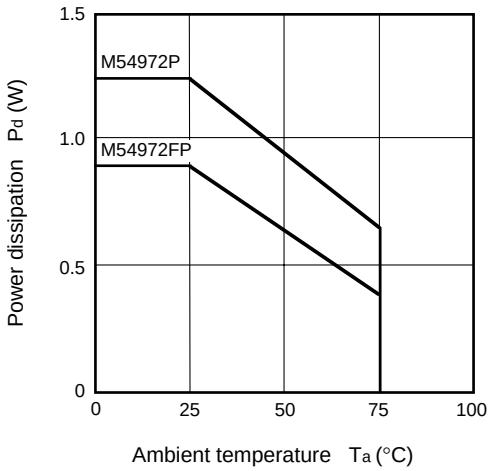
- The input waveform:
  $t_r \leq 20ns$, $t_f \leq 20ns$
- The capacitance C_L includes the stray wiring capacitance and probe input capacitance.

TIMING CHART

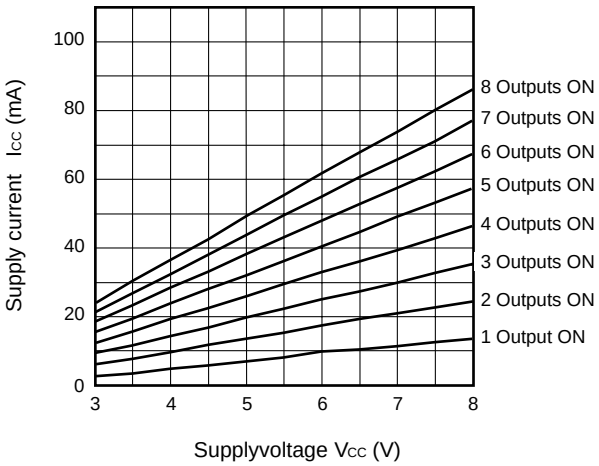


TYPICAL CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

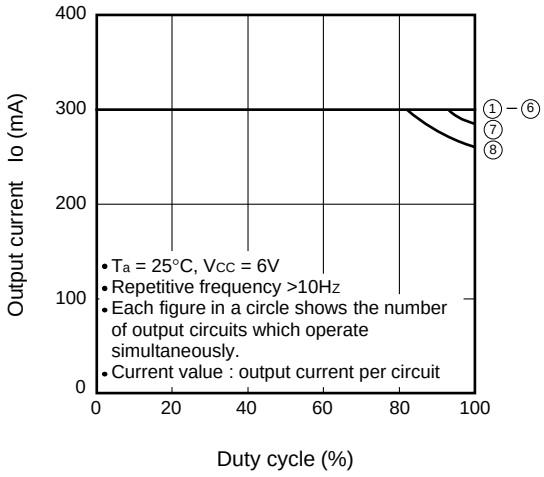
Thermal derating
(Absolute maximum rating)



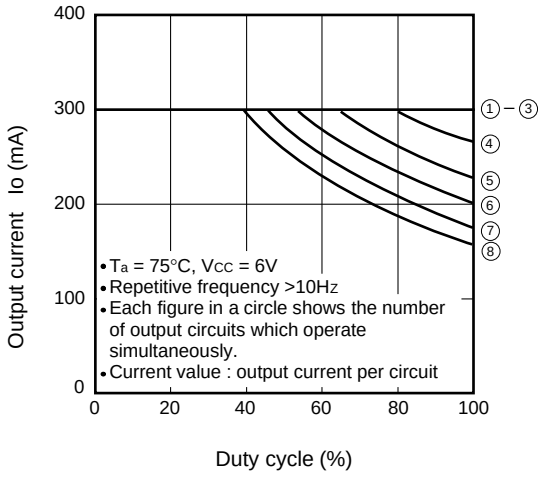
V_{CC} vs. I_{CC}



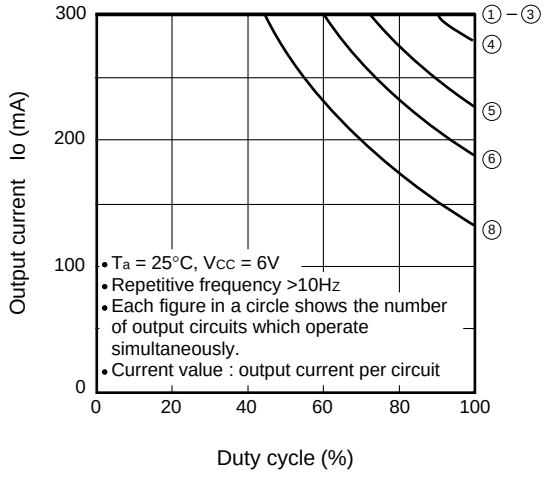
Duty cycle vs. allowable output current
(M54972P)



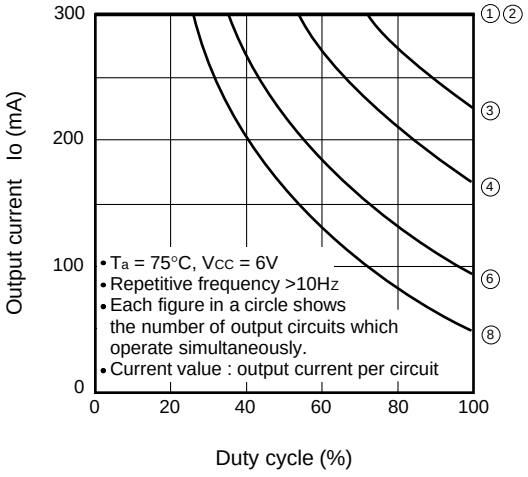
Duty cycle vs. allowable output current
(M54972P)



Duty cycle vs. allowable output current
(M54972FP)



Duty cycle vs. allowable output current
(M54972FP)



Driver output V_{OL} vs. I_{OL} (common)