**MOTOROLA**
**SEMICONDUCTOR**
**TECHNICAL DATA**

**Order this document**
**by MCM54100A/D**

# MCM54100A
# MCM5L4100A

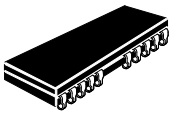
*Advance Information*

# 4M x 1 CMOS Dynamic RAM
## Fast Page Mode

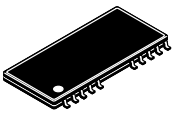
The MCM54100A is a 0.7µ CMOS high–speed dynamic random access memory. It is organized as 4,194,304 one–bit words and fabricated with CMOS silicon–gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM54100A requires only 11 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300 mil J lead small outline package and a 300 mil thin small outline package (TSOP).

- Three–State Data Output
- Fast Page Mode
- Test Mode
- TTL–Compatible Inputs and Outputs
- RAS–Only Refresh
- CAS Before RAS Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM54100A = 16 ms
- Fast Access Time ($t_{RAC}$):
  MCM54100A–60 and MCM5L4100A–60 = 60 ns (Max)
  MCM54100A–70 and MCM5L4100A–70 = 70 ns (Max)
  MCM54100A–80 and MCM5L4100A–80 = 80 ns (Max)
- Low Active Power:
  MCM54100A–60 and MCM5L4100A–60 = 660 mW (Max)
  MCM54100A–70 and MCM5L4100A–70 = 550 mW (Max)
  MCM54100A–80 and MCM5L4100A–80 = 468 mW (Max)
- Low Standby Power Dissipation:
  MCM54100A and MCM5L400A = 11 mW (Max, TTL Levels)
  MCM54100A = 5.5 mW (Max, CMOS Levels)
  MCM5L4100A = 1.1 mW (Max, CMOS Levels)

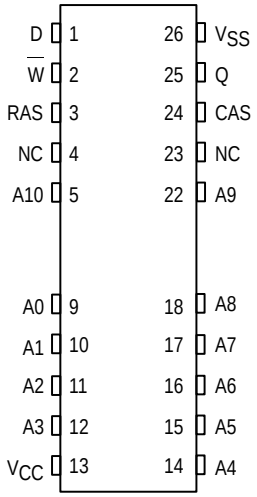


**N PACKAGE**
**300 MIL SOJ**
**CASE 822–03**



**T PACKAGE**
**300 MIL TSOP**
**CASE 892–01**

**PIN ASSIGNMENT**




**PIN NAMES**

| | |
|---|---|
| A0 – A10 | Address Input |
| D | Data Input |
| Q | Data Output |
| W | Read/Write Enable |
| RAS | Row Address Strobe |
| CAS | Column Address Strobe |
| $V_{CC}$ | Power Supply (+ 5 V) |
| $V_{SS}$ | Ground |
| NC | No Connection |

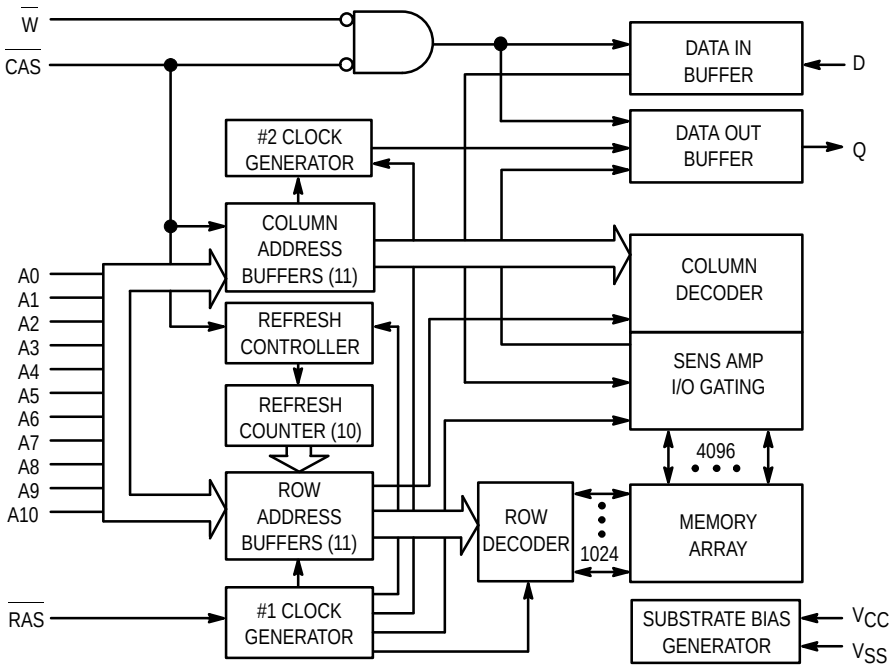
This document contains information on a new product. Specifications and information herein are subject to change without notice.

**REV 4**
**10/95**



MOTOROLA

## BLOCK DIAGRAM




**ABSOLUTE MAXIMUM RATINGS** (See Note)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | – 1 to + 7 | V |
| Voltage Relative to $V_{SS}$ for Any Pin Except $V_{CC}$ | $V_{in}$, $V_{out}$ | – 1 to + 7 | V |
| Data Output Current | $I_{out}$ | 50 | mA |
| Power Dissipation | $P_D$ | 700 | mW |
| Operating Temperature Range | $T_A$ | 0 to + 70 | °C |
| Storage Temperature Range | $T_{stg}$ | – 55 to + 150 | °C |

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}$ = 5.0 V ± 10%, $T_A$ = 0 to 70°C, Unless Otherwise Noted)

**RECOMMENDED OPERATING CONDITIONS** (All voltages referenced to $V_{SS}$)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage (Operating Voltage Range) | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| | $V_{SS}$ | 0 | 0 | 0 | |
| Logic High Voltage, All Inputs | $V_{IH}$ | 2.4 | — | 6.5 | V |
| Logic Low Voltage, All Inputs | $V_{IL}$ | – 1.0 | — | 0.8 | V |

**DC CHARACTERISTICS**

| Characteristic | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $V_{CC}$ Power Supply Current | $I_{CC1}$ | | | mA | 1, 2 |
| MCM54100A–60 and MCM5L4100A–60, $t_{RC}$ = 110 ns | | — | 120 | | |
| MCM54100A–70 and MCM5L4100A–70, $t_{RC}$ = 130 ns | | — | 100 | | |
| MCM54100A–80 and MCM5L4100A–80, $t_{RC}$ = 150 ns | | — | 85 | | |
| $V_{CC}$ Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = $V_{IH}$) | $I_{CC2}$ | — | 2.0 | mA | |
| $V_{CC}$ Power Supply Current During RAS Only Refresh Cycles ($\overline{CAS}$ = $V_{IH}$) | $I_{CC3}$ | | | mA | 1, 2 |
| MCM54100A–60 and MCM5L4100A–60, $t_{RC}$ = 110 ns | | — | 120 | | |
| MCM54100A–70 and MCM5L4100A–70, $t_{RC}$ = 130 ns | | — | 100 | | |
| MCM54100A–80 and MCM5L4100A–80, $t_{RC}$ = 150 ns | | — | 85 | | |
| $V_{CC}$ Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = $V_{IL}$) | $I_{CC4}$ | | | mA | 1, 2 |
| MCM54100A–60 and MCM5L4100A–60, $t_{PC}$ = 45 ns | | — | 70 | | |
| MCM54100A–70 and MCM5L4100A–70, $t_{PC}$ = 45 ns | | — | 70 | | |
| MCM54100A–80 and MCM5L4100A–80, $t_{PC}$ = 50 ns | | — | 60 | | |
| $V_{CC}$ Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = $V_{CC}$ – 0.2 V) | $I_{CC5}$ | | | | |
| MCM54100A | | — | 1.0 | mA | |
| MCM5L4100A | | — | 200 | µA | |
| $V_{CC}$ Power Supply Current During CAS Before RAS Refresh Cycle | $I_{CC6}$ | | | mA | 1 |
| MCM54100A–60 and MCM5L4100A–60, $t_{RC}$ = 110 ns | | — | 120 | | |
| MCM54100A–70 and MCM5L4100A–70, $t_{RC}$ = 130 ns | | — | 100 | | |
| MCM54100A–80 and MCM5L4100A–80, $t_{RC}$ = 150 ns | | — | 85 | | |
| $V_{CC}$ Power Supply Current, Battery Backup Mode — MCM5L4100A Only ($t_{RC}$ = 125 µs; $\overline{CAS}$ = CAS Before RAS Cycling or 0.2 V; W = $V_{CC}$ – 0.2 V; $D_{in}$ = $V_{CC}$ – 0.2 V or 0.2 V or OPEN; A0 – A10 = $V_{CC}$ – 0.2 V or 0.2 V) | $I_{CC7}$ | | | µA | 1, 3 |
| $t_{RAS}$ = 300 ns to 1 µs | | — | 400 | | |
| $t_{RAS}$ = Min to 300 ns | | — | 300 | | |
| Input Leakage Current (0 V ≤ $V_{in}$ ≤ 6.5 V) | $I_{lkg(I)}$ | – 10 | 10 | µA | |
| Output Leakage Current ($\overline{CAS}$ = $V_{IH}$, 0 V ≤ $V_{out}$ ≤ 5.5 V) | $I_{lkg(O)}$ | – 10 | 10 | µA | |
| Output High Voltage ($I_{OH}$ = – 5 mA) | $V_{OH}$ | 2.4 | — | V | |
| Output Low Voltage ($I_{OL}$ = 4.2 mA) | $V_{OL}$ | — | 0.4 | V | |

NOTES:
1. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = $V_{IL}$ and $\overline{CAS}$ = $V_{IH}$.
3. $t_{RAS}$ (max) = 1 µs is only applied to refresh of battery–back up. $t_{RAS}$ (max) = 10 µs is applied to functional operating

**CAPACITANCE** (f = 1.0 MHz, $T_A$ = 25°C, $V_{CC}$ = 5 V, Periodically Sampled Rather Than 100% Tested)

| Characteristic | | Symbol | Max | Unit |
|---|---|---|---|---|
| Input Capacitance | A0 – A10, D | $C_{in}$ | 5 | pF |
| | $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$ | | 7 | |
| I/O Capacitance ($\overline{CAS}$ = $V_{IH}$ to Disable Output) | Q | $C_{out}$ | 7 | pF |

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

## AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}$ = 5.0 V ± 10%, $T_A$ = 0 to 70°C, Unless Otherwise Noted)

**READ, WRITE, AND READ–WRITE CYCLES** (See Notes 1, 2, 3, and 4)

| Parameter | Symbol | | MCM54100A–60 MCM5L4100A–60 | | MCM54100A–70 MCM5L4100A–70 | | MCM54100A–80 MCM5L4100A–80 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | Std | Alt | Min | Max | Min | Max | Min | Max | | |
| Random Read or Write Cycle Time | $t_{RELREL}$ | $t_{RC}$ | 110 | — | 130 | — | 150 | — | ns | 5 |
| Read–Write Cycle Time | $t_{RELREL}$ | $t_{RWC}$ | 140 | — | 155 | — | 175 | — | ns | 5 |
| Fast Page Mode Cycle Time | $t_{CELCEL}$ | $t_{PC}$ | 45 | — | 45 | — | 50 | — | ns | |
| Fast Page Mode Read–Write Cycle Time | $t_{CELCEL}$ | $t_{PRWC}$ | 65 | — | 70 | — | 75 | — | ns | |
| Access Time from RAS | $t_{RELQV}$ | $t_{RAC}$ | — | 60 | — | 70 | — | 80 | ns | 6, 7 |
| Access Time from CAS | $t_{CELQV}$ | $t_{CAC}$ | — | 20 | — | 20 | — | 20 | ns | 6, 8 |
| Access Time from Column Address | $t_{AVQV}$ | $t_{AA}$ | — | 30 | — | 35 | — | 40 | ns | 6, 9 |
| Access Time from Precharge CAS | $t_{CEHQV}$ | $t_{CPA}$ | — | 40 | — | 40 | — | 45 | ns | 6 |
| CAS to Output in Low–Z | $t_{CELQX}$ | $t_{CLZ}$ | 0 | — | 0 | — | 0 | — | ns | 6 |
| Output Buffer and Turn–Off Delay | $t_{CEHQZ}$ | $t_{OFF}$ | 0 | 20 | 0 | 20 | 0 | 20 | ns | 10 |
| Transition Time (Rise and Fall) | $t_T$ | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns | |
| RAS Precharge Time | $t_{REHREL}$ | $t_{RP}$ | 45 | — | 50 | — | 60 | — | ns | |
| RAS Pulse Width | $t_{RELREH}$ | $t_{RAS}$ | 60 | 10 k | 70 | 10 k | 80 | 10 k | ns | |
| RAS Pulse Width (Fast Page Mode) | $t_{RELREH}$ | $t_{RASP}$ | 60 | 200 k | 70 | 200 k | 80 | 200 k | ns | |
| RAS Hold Time | $t_{CELREH}$ | $t_{RSH}$ | 20 | — | 20 | — | 20 | — | ns | |
| CAS Hold Time | $t_{RELCEH}$ | $t_{CSH}$ | 60 | — | 70 | — | 80 | — | ns | |
| CAS Precharge to RAS Hold Time | $t_{CEHREH}$ | $t_{RHCP}$ | 40 | — | 40 | — | 45 | — | ns | |
| CAS Pulse Width | $t_{CELCEH}$ | $t_{CAS}$ | 20 | 10 k | 20 | 10 k | 20 | 10 k | ns | |
| RAS to CAS Delay Time | $t_{RELCEL}$ | $t_{RCD}$ | 20 | 40 | 20 | 50 | 20 | 60 | ns | 11 |
| RAS to Column Address Delay Time | $t_{RELAV}$ | $t_{RAD}$ | 15 | 30 | 15 | 35 | 15 | 40 | ns | 12 |
| CAS to RAS Precharge Time | $t_{CEHREL}$ | $t_{CRP}$ | 5 | — | 5 | — | 5 | — | ns | |
| CAS Precharge Time | $t_{CEHCEL}$ | $t_{CP}$ | 10 | — | 10 | — | 10 | — | ns | |
| Row Address Setup Time | $t_{AVREL}$ | $t_{ASR}$ | 0 | — | 0 | — | 0 | — | ns | |
| Row Address Hold Time | $t_{RELAX}$ | $t_{RAH}$ | 10 | — | 10 | — | 10 | — | ns | |

NOTES: (continued)

1. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$.
2. An initial pause of 200 µs is required after power–up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
4. AC measurements $t_T$ = 5.0 ns.
5. The specification for $t_{RC}$ (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ $T_A$ ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at $V_{OH}$ = 2.0 V and $V_{OL}$ = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. $t_{OFF}$ (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the $t_{RCD}$ (max) limit ensures that $t_{RAC}$ (max) can be met. $t_{RCD}$ (max) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled exclusively by $t_{CAC}$.
12. Operation within the $t_{RAD}$ (max) limit ensures that $t_{RAC}$ (max) can be met. $t_{RAD}$ (max) is specified as a reference point only; if $t_{RAD}$ is greater than the specified $t_{RAD}$ (max), then access time is controlled exclusively by $t_{AA}$.

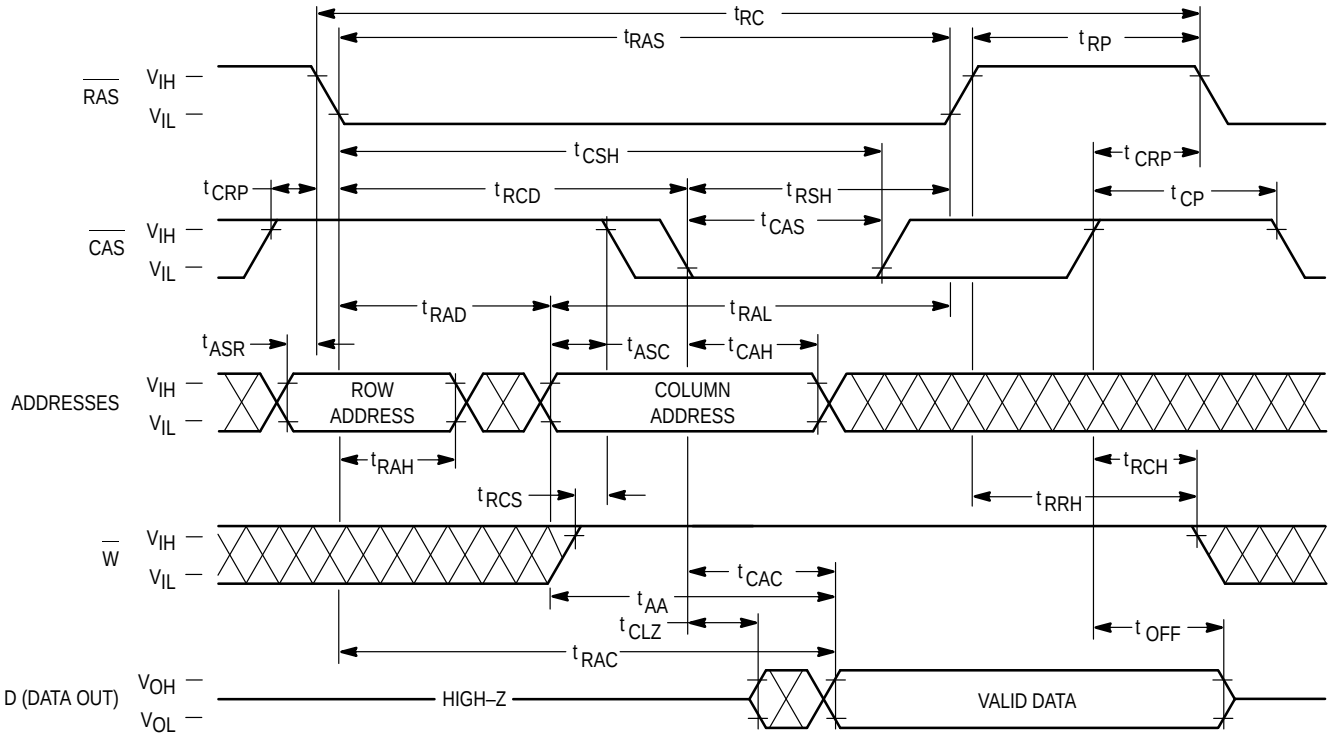
**READ, WRITE, AND READ–WRITE CYCLES** (Continued)

| Parameter | Symbol | | MCM54100A–60 MCM5L4100A–60 | | MCM54100A–70 MCM5L4100A–70 | | MCM54100A–80 MCM5L4100A–80 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | Std | Alt | Min | Max | Min | Max | Min | Max | | |
| Column Address Setup Time | $t_{AVCEL}$ | $t_{ASC}$ | 0 | — | 0 | — | 0 | — | ns | |
| Column Address Hold Time | $t_{CELAX}$ | $t_{CAH}$ | 15 | — | 15 | — | 15 | — | ns | |
| Column Address to RAS Lead Time | $t_{AVREH}$ | $t_{RAL}$ | 30 | — | 35 | — | 40 | — | ns | |
| Read Command Setup Time | $t_{WHCEL}$ | $t_{RCS}$ | 0 | — | 0 | — | 0 | — | ns | |
| Read Command Hold Time Referenced to CAS | $t_{CEHWX}$ | $t_{RCH}$ | 0 | — | 0 | — | 0 | — | ns | 13 |
| Read Command Hold Time Referenced to RAS | $t_{REHWX}$ | $t_{RRH}$ | 0 | — | 0 | — | 0 | — | ns | 13 |
| Write Command Hold Time Referenced to CAS | $t_{CELWH}$ | $t_{WCH}$ | 10 | — | 15 | — | 15 | — | ns | |
| Write Command Pulse Width | $t_{WLWH}$ | $t_{WP}$ | 10 | — | 15 | — | 15 | — | ns | |
| Write Command to RAS Lead Time | $t_{WLREH}$ | $t_{RWL}$ | 20 | — | 20 | — | 20 | — | ns | |
| Write Command to CAS Lead Time | $t_{WLCEH}$ | $t_{CWL}$ | 20 | — | 20 | — | 20 | — | ns | |
| Data in Setup Time | $t_{DVCEL}$ | $t_{DS}$ | 0 | — | 0 | — | 0 | — | ns | 14 |
| Data in Hold Time | $t_{CELDX}$ | $t_{DH}$ | 15 | — | 15 | — | 15 | — | ns | 14 |
| Refresh Period MCM54100A<br>MCM5L4100A | $t_{RVRV}$ | $t_{RFSH}$ | —<br>— | 16<br>128 | —<br>— | 16<br>128 | —<br>— | 16<br>128 | ms | |
| Write Command Setup Time | $t_{WLCEL}$ | $t_{WCS}$ | 0 | — | 0 | — | 0 | — | ns | 15 |
| CAS to Write Delay | $t_{CELWL}$ | $t_{CWD}$ | 20 | — | 20 | — | 20 | — | ns | 15 |
| RAS to Write Delay | $t_{RELWL}$ | $t_{RWD}$ | 60 | — | 70 | — | 80 | — | ns | 15 |
| Column Address to Write Delay Time | $t_{AVWL}$ | $t_{AWD}$ | 30 | — | 35 | — | 40 | — | ns | 15 |
| CAS Precharge to Write Delay Time (Page Mode) | $t_{CEHWL}$ | $t_{CPWD}$ | 40 | — | 40 | — | 40 | — | ns | 15 |
| CAS Setup Time for CAS Before RAS Refresh | $t_{RELCEL}$ | $t_{CSR}$ | 5 | — | 5 | — | 5 | — | ns | |
| CAS Hold Time for CAS Before RAS Refresh | $t_{RELCEH}$ | $t_{CHR}$ | 15 | — | 15 | — | 15 | — | ns | |
| RAS Precharge to CAS Active Time | $t_{REHCEL}$ | $t_{RPC}$ | 0 | — | 0 | — | 0 | — | ns | |
| CAS Precharge Time for CAS Before RAS Counter Time | $t_{CEHCEL}$ | $t_{CPT}$ | 30 | — | 40 | — | 40 | — | ns | |
| Write Command Setup Time (Test Mode) | $t_{WLREL}$ | $t_{WTS}$ | 10 | — | 10 | — | 10 | — | ns | |
| Write Command Hold Time (Test Mode) | $t_{RELWH}$ | $t_{WTH}$ | 10 | — | 10 | — | 10 | — | ns | |
| Write to RAS Precharge Time (CAS Before RAS Refresh) | $t_{WHREL}$ | $t_{WRP}$ | 10 | — | 10 | — | 10 | — | ns | |
| Write to RAS Hold Time (CAS Before RAS Refresh) | $t_{RELWL}$ | $t_{WRH}$ | 10 | — | 10 | — | 10 | — | ns | |

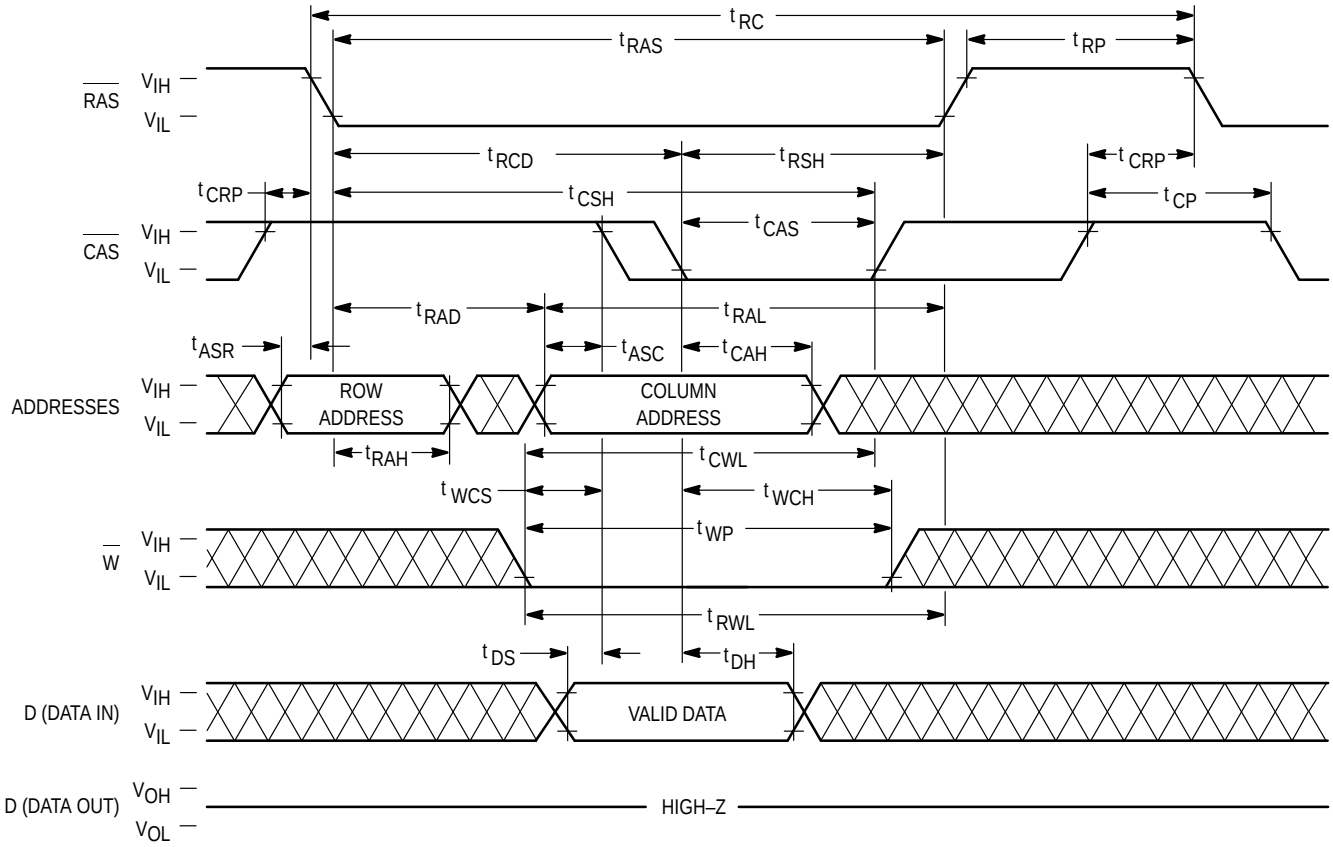
NOTES:

13. Either $t_{RRH}$ or $t_{RCH}$ must be satisfied for a read cycle.
14. These parameters are referenced to CAS leading edge in early write cycles and to $\overline{W}$ leading edge in read–write cycles.
15. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{AWD}$, and $t_{CPWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read–write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

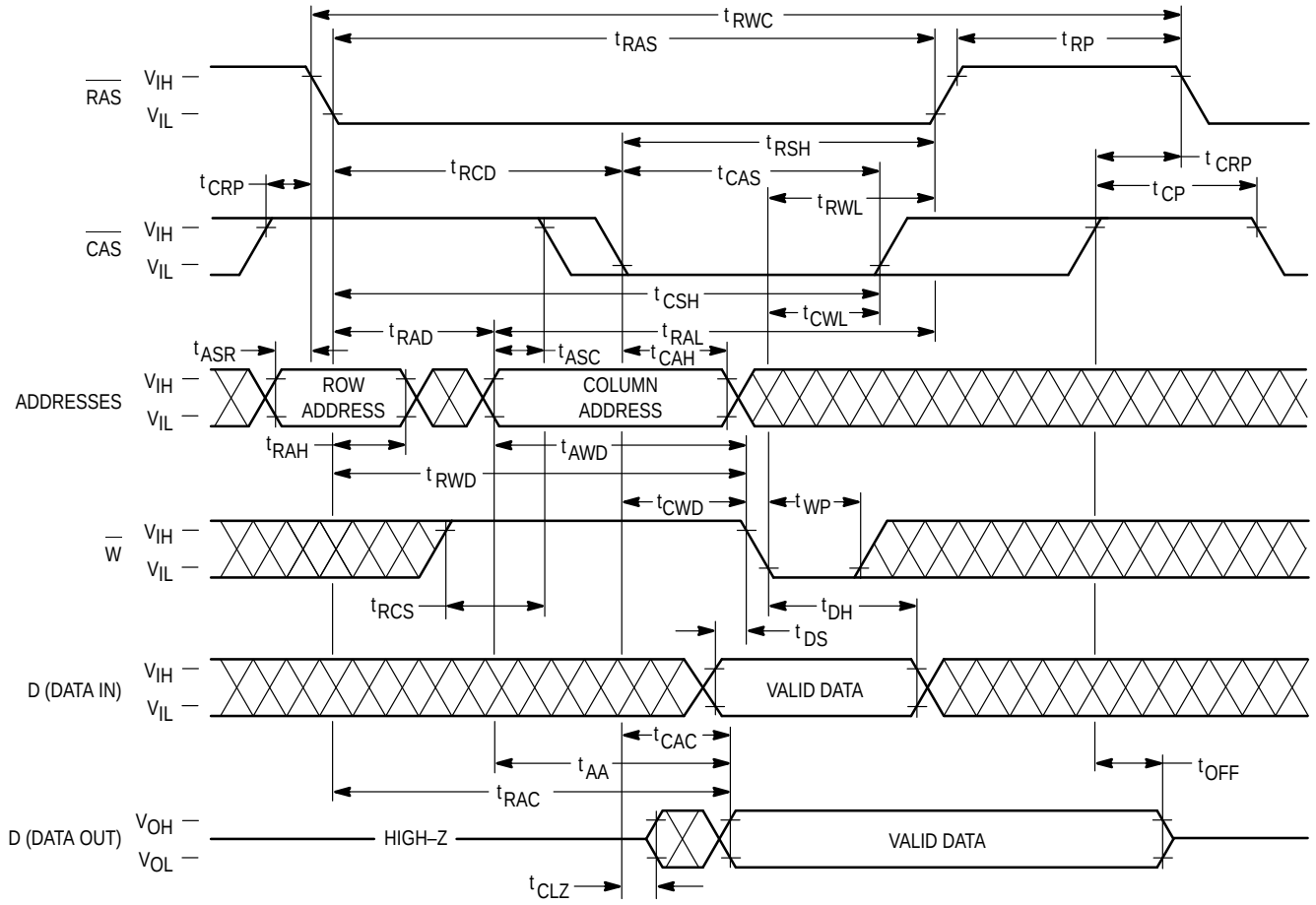
## READ CYCLE



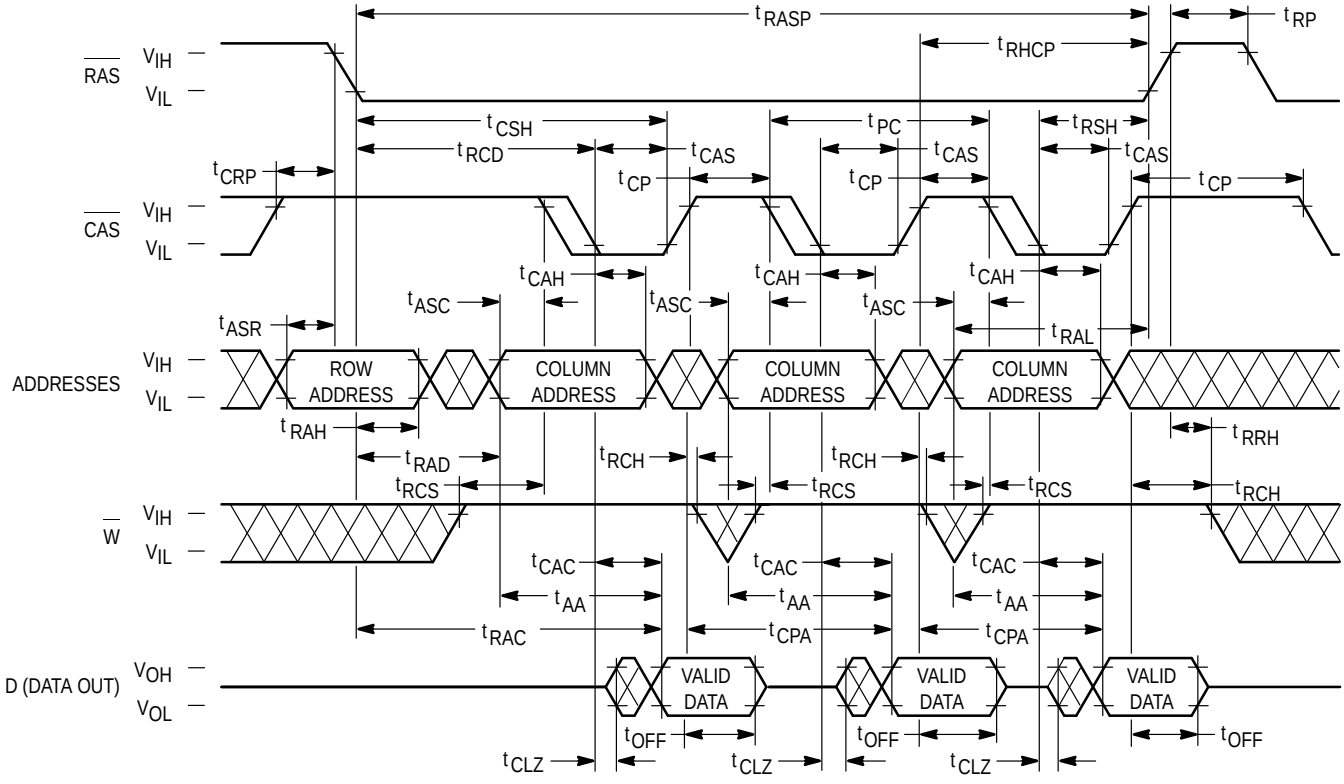

## EARLY WRITE CYCLE



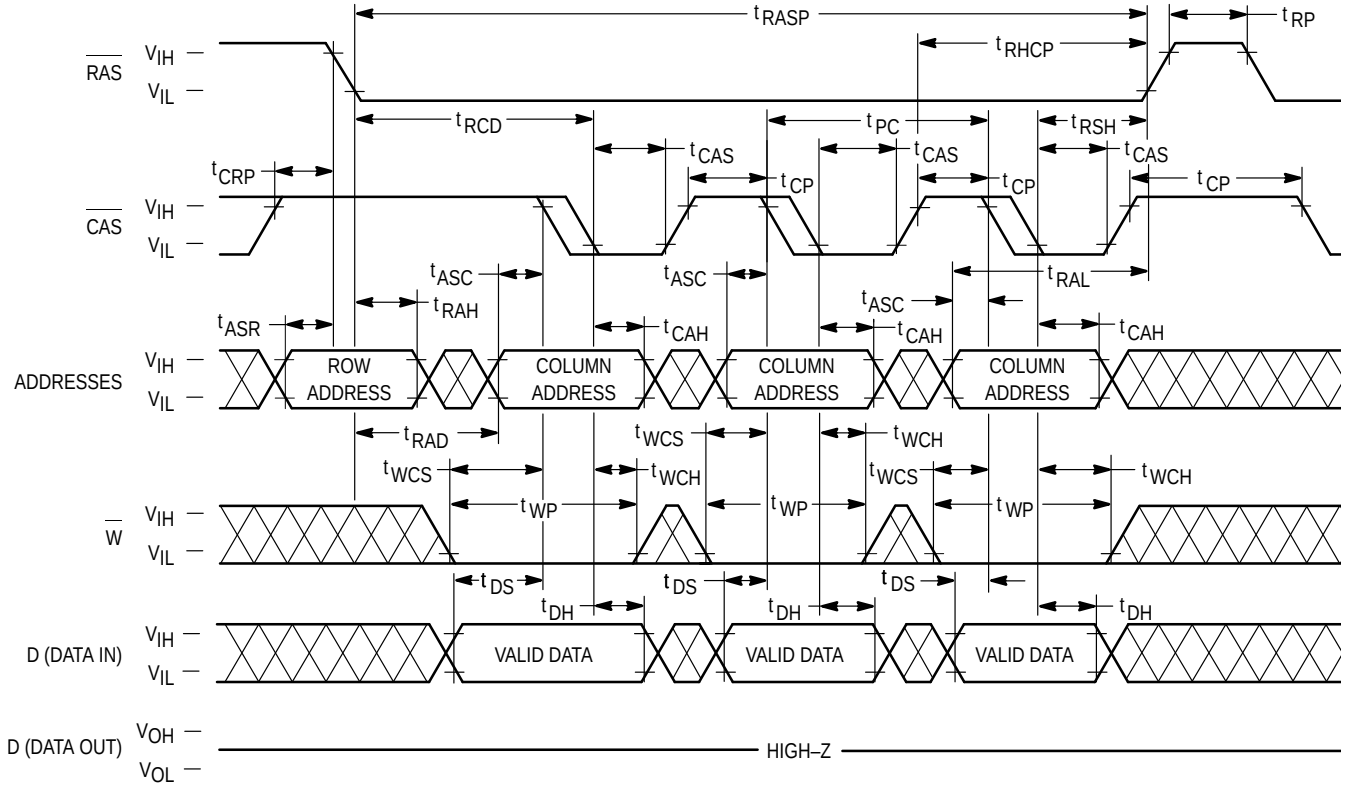
## READ–WRITE CYCLE



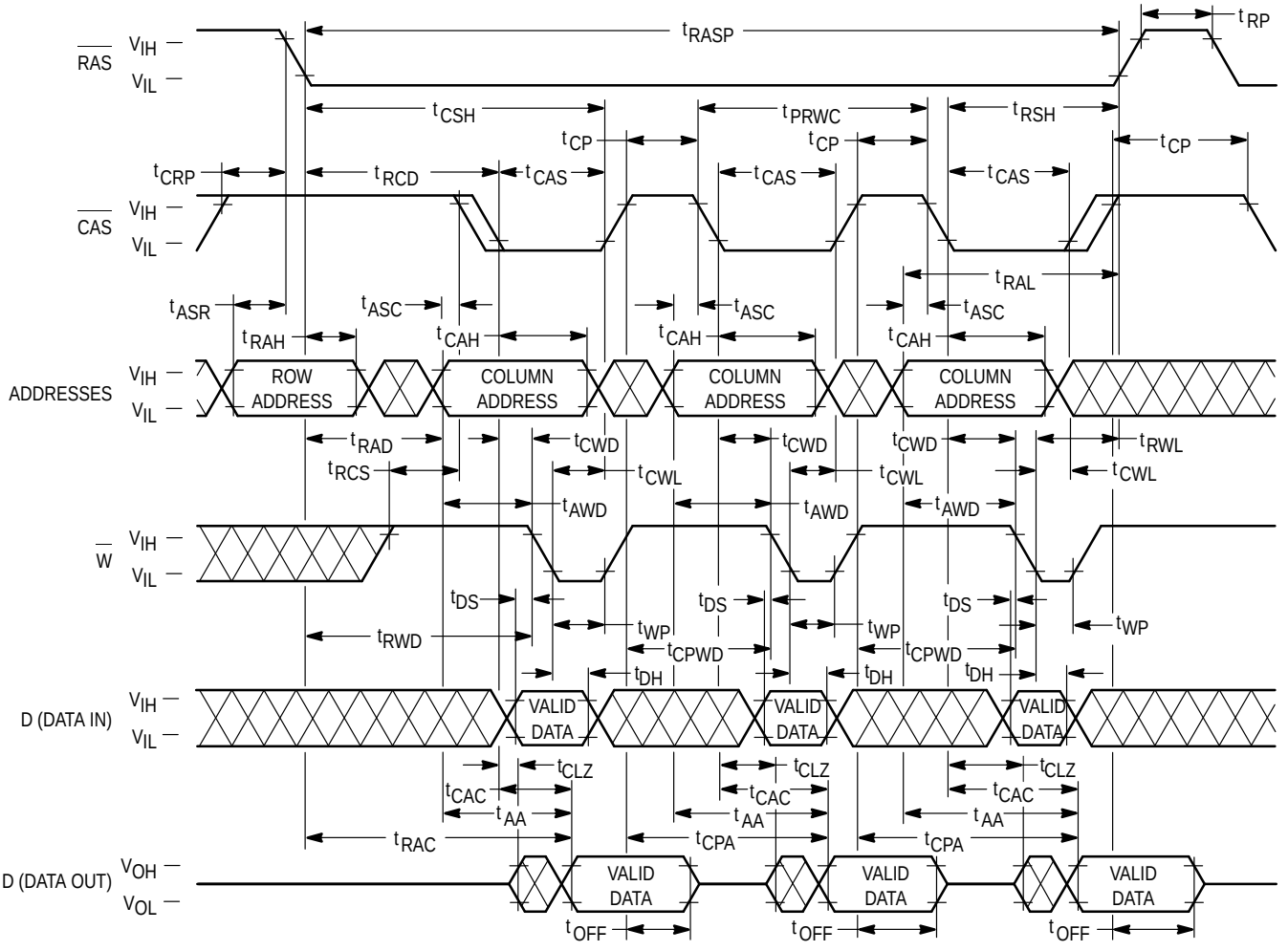

## FAST PAGE MODE READ CYCLE



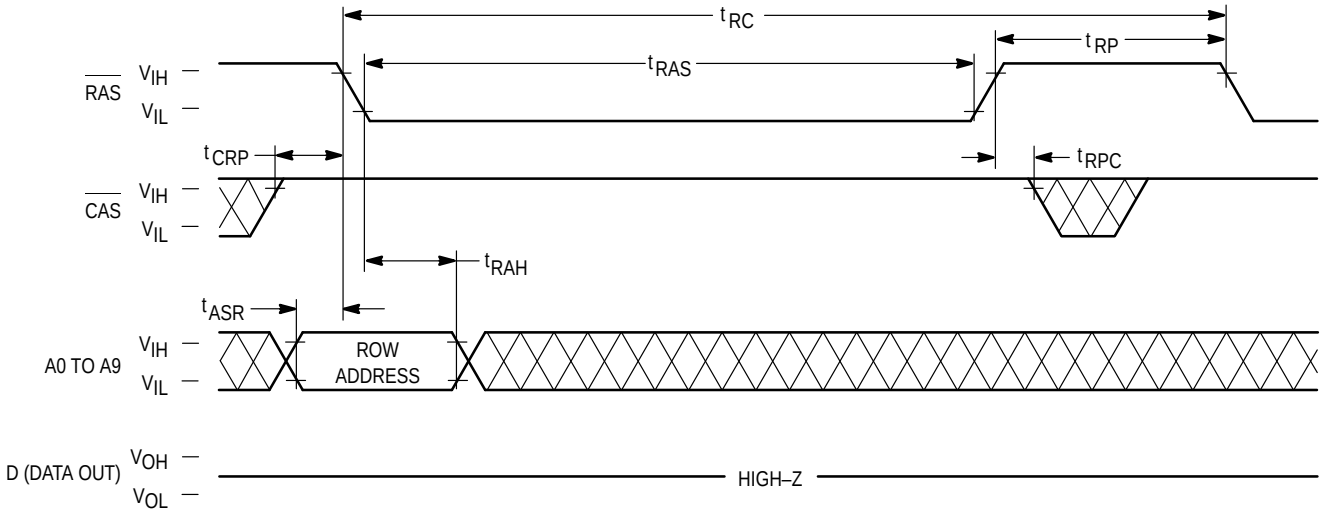
## FAST PAGE MODE EARLY WRITE CYCLE



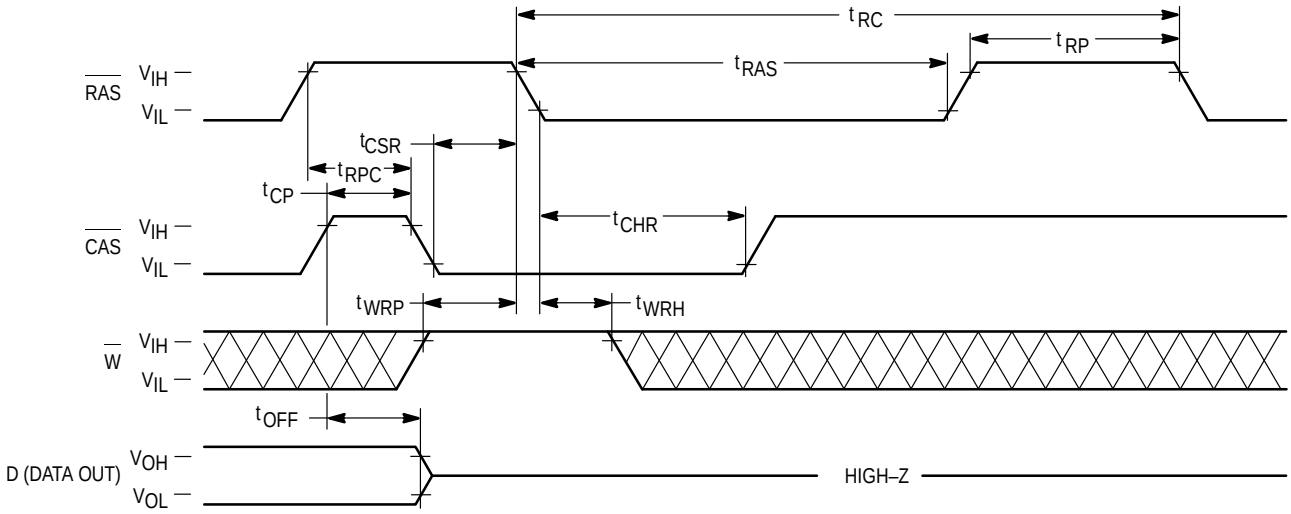

## FAST PAGE MODE READ–WRITE CYCLE



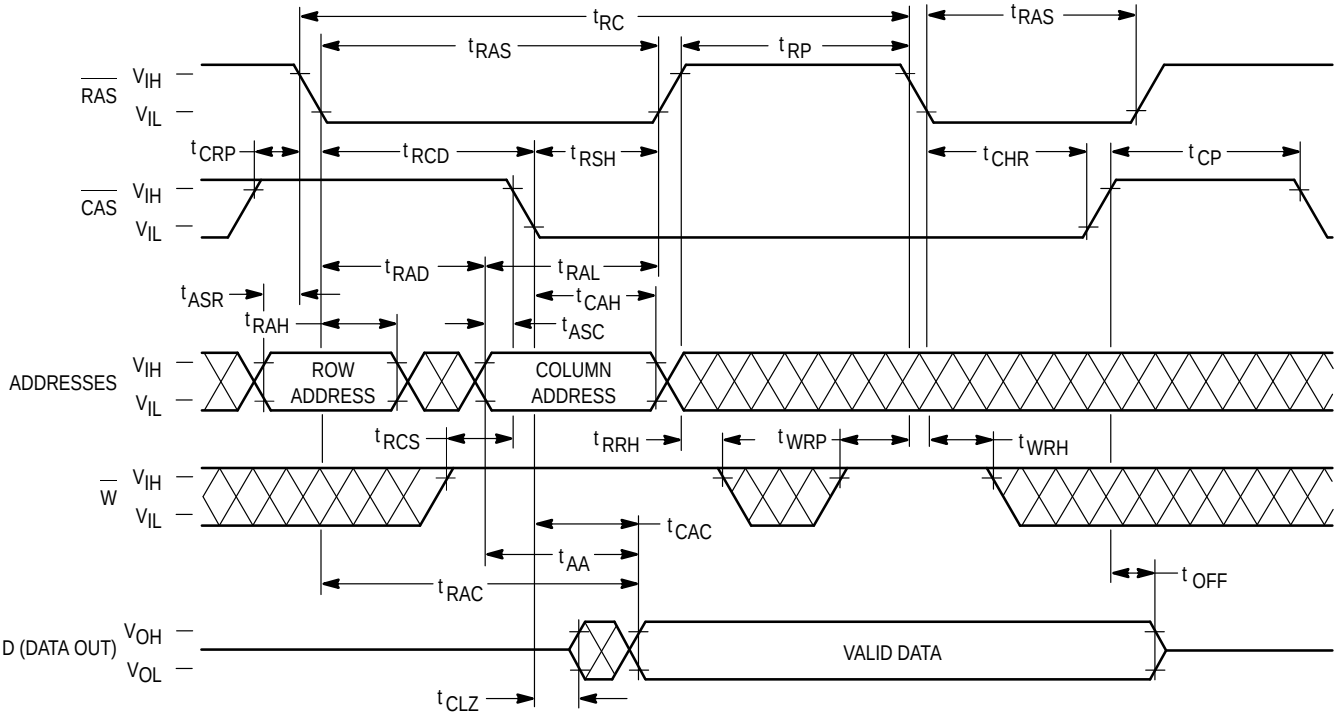
## $\overline{\text{RAS}}$ ONLY REFRESH CYCLE
**(W and A10 are Don't Care)**



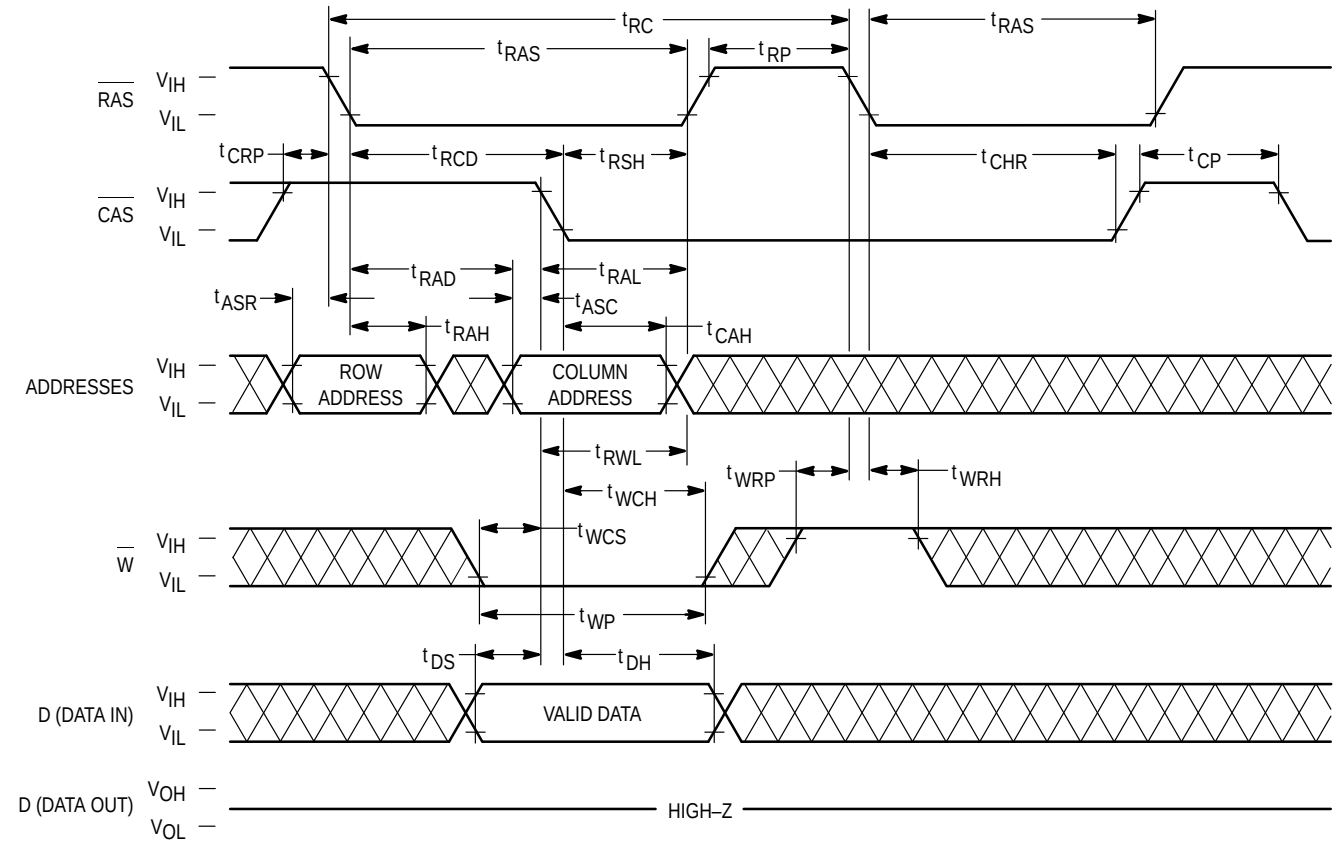

## $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
**(A0 – A10 are Don't Care)**



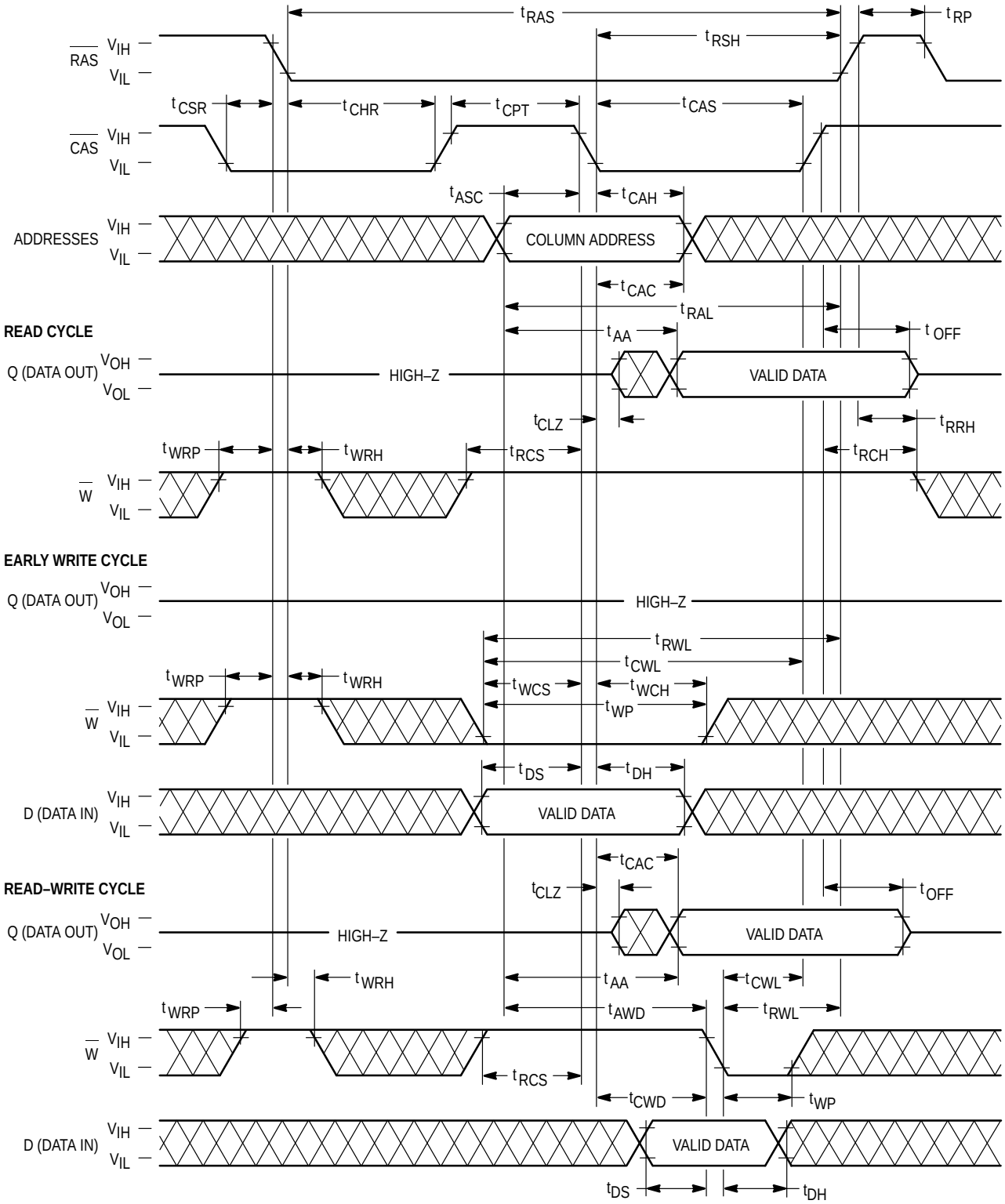
## HIDDEN REFRESH CYCLE (READ)




## HIDDEN REFRESH CYCLE (EARLY WRITE)



## $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



## DEVICE INITIALIZATION

On power–up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds or 128 milliseconds in case of low power device, with the device powered up), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

## ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe (RAS) and column address strobe (CAS), into two separate 11–bit address fields. A total of twenty–two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 bit locations in the device. RAS active transition is followed by CAS active transition (active = $V_{IL}$, $t_{RCD}$ minimum) for all read or write cycles. The delay between RAS and CAS active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external CAS signal is ignored until an internal RAS signal is available. This "gate" feature on the external CAS clock enables the internal CAS line as soon as the row address hold time ($t_{RAH}$) specification is met (and defines $t_{RCD}$ minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the CAS clock.

There are three other variations in addressing the 4M RAM: **RAS only refresh cycle, CAS before RAS refresh cycle,** and **page mode**.

## READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read–write cycle, and page mode read–write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with RAS and CAS active transitions latching the desired bit location. The write (W) input level must be high ($V_{IH}$), $t_{RCS}$ (minimum) before the CAS active transition, to enable read mode.

Both the RAS and CAS clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window; however, CAS must be active before or at $t_{RCD}$ maximum to guarantee valid data out (Q) at $t_{RAC}$ (access time from RAS active transition). If the $t_{RCD}$ maximum is exceeded, read access time is determined by the CAS clock active transition ($t_{CAC}$).

The RAS and CAS clocks must remain active for a minimum time of $t_{RAS}$ and $t_{CAS}$, respectively, to complete the read cycle. W must remain high throughout the cycle, and for time $t_{RRH}$ or $t_{RCH}$ after RAS or CAS inactive transition, respectively, to maintain the data at that bit location. Once RAS transitions to inactive, it must remain inactive for a minimum time of $t_{RP}$ to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the CAS clock is active. When the CAS clock transitions to inactive, the output will switch to High–Z (three–state).

## WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read–write. Early and late write modes are discussed here, while page mode write operations are covered elsewhere.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of W to active ($V_{IL}$). Early and late write modes are distinguished by the active transition of W, with respect to CAS. Minimum active time $t_{RAS}$ and $t_{CAS}$, and precharge time $t_{RP}$ apply to write mode, as in the read mode.

An early write cycle is characterized by W active transition at minimum time $t_{WCS}$ before CAS active transition. Data in (D) is referenced to CAS in an early write cycle. RAS and CAS clocks must stay active for $t_{RWL}$ and $t_{CWL}$, respectively, after the start of the early write operation to complete the cycle.

Q remains in three–state condition throughout an early write cycle because W active transition precedes or coincides with CAS active transition, keeping data–out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when W active transition is made after CAS active transition. W active transition could be delayed for almost 10 microseconds after CAS active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T$) ≤ $t_{RAS}$, if other timing minimums ($t_{RCD}$, $t_{RWL}$, and $t_T$) are maintained. D is referenced to W active transition in a late write cycle. Output buffers are enabled by CAS active transition but Q may be indeterminate; see note 15 of AC Operating Conditions table. RAS and CAS must remain active for $t_{RWL}$ and $t_{CWL}$, respectively, after W active transition to complete the write cycle.

## READ–WRITE CYCLE

A read–write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except W must remain high for $t_{CWD}$ minimum after the CAS active transition, to guarantee valid Q before writing the bit.

## PAGE MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the 4M dynamic RAM. Read access time in page mode ($t_{CAC}$) is typically half the regular RAS clock access time, $t_{RAC}$. Page mode operation consists of keeping RAS active while toggling CAS between $V_{IH}$ and $V_{IL}$. The row is latched by RAS active transition, while each CAS active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read–write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, CAS transitions to inactive for minimum of $t_{CP}$, while RAS remains low ($V_{IL}$). The second CAS active transition while RAS is low initiates the first page mode cycle ($t_{PC}$ or $t_{PRWC}$). Either a read, write, or read–write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed

in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by $t_{RASP}$. Page mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

## REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM54100A require refresh every 16 milliseconds, while refresh time for the MCM5L4100A is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM54100A, and 124.8 microseconds for the MCM5L4100A. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM54100A and 128 milliseconds on the MCM5L4100A.

A normal read, write, or read–write operation to the RAM will refresh all the bits (4096) associated with the particular row decoded. Three other methods of refresh, **RAS–only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

### $\overline{\text{RAS}}$–Only Refresh

$\overline{\text{RAS}}$–only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while CAS remains high ($V_{IH}$) throughout the cycle. An external counter is employed to ensure that all rows are refreshed within the specified limit.

### $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). W must be inactive for time $t_{WRP}$ before and time $t_{WRH}$ after RAS active transition to prevent switching the device into **test mode**.

### Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for $t_{RP}$ and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode entry) as in CAS before RAS refresh.

### $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This test is performed with a read–write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed after a minimum of 8 **CAS before RAS** initialization cycles. Test procedure:

1. Write 0s into all memory cells with normal write mode.
2. Select a column address, read 0 out and write 1 into the cell by performing the **CAS before RAS refresh counter test, read–write cycle**. Repeat this operation 1024 times.
3. Read the 1s which were written in step two in normal read mode.
4. Using the same starting column address as in step two, read 1 out and write 0 into the cell by performing the **CAS before RAS refresh counter test, read–write cycle**. Repeat this operation 1024 times.
5. Read 0s which were written in step four in normal read mode.
6. Repeat steps one through five using complement data.

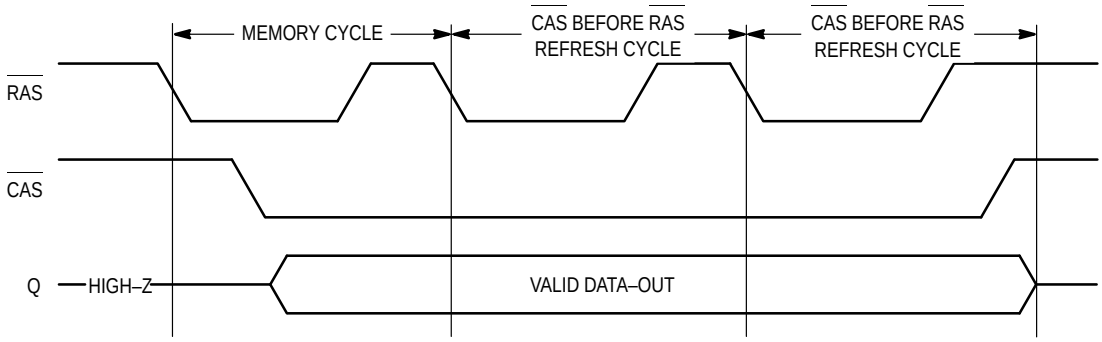



**Figure 1. Hidden Refresh Cycle**

## TEST MODE

The internal organization of this device (512K x 8) allows it to be tested as if it were a 512K x 1 DRAM. Nineteen of the twenty–two addresses are used when operating the device in test mode. Row address A0, and column addresses A0 and A10 are ignored by the device in test mode. A test mode cycle reads and/or writes data to a bit in each of eight 512K blocks (B0 – B7) in parallel. External data out is determined by the internal test mode logic of the device. See the following truth table and test mode block diagram.

W, CAS before RAS timing puts the device in **"Test Mode"** as shown in the test mode timing diagram. A **CAS before RAS** or a **RAS only** refresh cycle puts the device back into normal mode. Refresh is performed in test mode by using a **W, CAS before RAS** refresh cycle which uses internal refresh address counter.

**TEST MODE TRUTH TABLE**

| D | B0 | B1 | B2 | B3 | B4 | B5 | B6 | B7 | Q |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| — | Any Other | | | | | | | | 0 |

## TEST MODE
## AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}$ = 5.0 V ± 10%, $T_A$ = 0 to 70°C, Unless Otherwise Noted)

**READ, WRITE, AND READ–WRITE CYCLES** (See Notes 1, 2, 3, and 4)

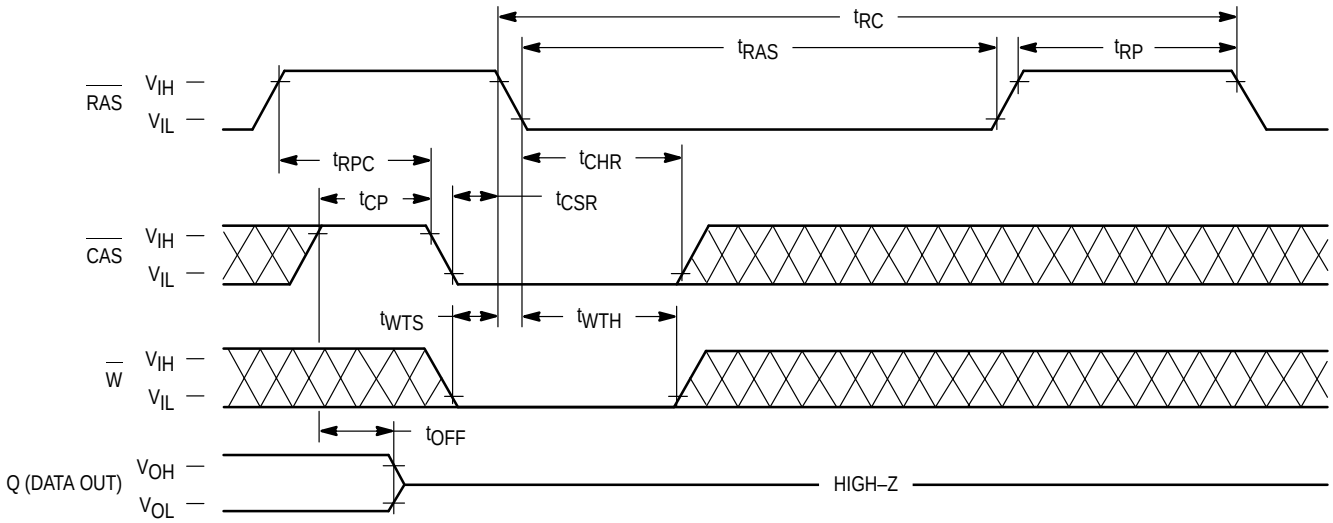
| Parameter | Symbol | | MCM54100A–60 MCM5L4100A–60 | | MCM54100A–70 MCM5L4100A–70 | | MCM54100A–80 MCM5L4100A–80 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | Std | Alt | Min | Max | Min | Max | Min | Max | | |
| Random Read or Write Cycle Time | $t_{RELREL}$ | $t_{RC}$ | 115 | — | 135 | — | 155 | — | ns | 5 |
| Fast Page Mode Cycle Time | $t_{CELCEL}$ | $t_{PC}$ | 50 | — | 50 | — | 55 | — | ns | |
| Access Time from RAS | $t_{RELQV}$ | $t_{RAC}$ | — | 65 | — | 75 | — | 85 | ns | 6, 7 |
| Access Time from CAS | $t_{CELQV}$ | $t_{CAC}$ | — | 25 | — | 25 | — | 25 | ns | 6, 8 |
| Access Time from Column Address | $t_{AVQV}$ | $t_{AA}$ | — | 35 | — | 40 | — | 45 | ns | 6, 9 |
| Access Time from Precharge CAS | $t_{CEHQV}$ | $t_{CPA}$ | — | 45 | — | 45 | — | 50 | ns | 6 |
| RAS Pulse Width | $t_{RELREH}$ | $t_{RAS}$ | 65 | 10 k | 75 | 10 k | 85 | 10 k | ns | |
| RAS Pulse Width (Fast Page Mode) | $t_{RELREH}$ | $t_{RASP}$ | 65 | 200 k | 75 | 200 k | 85 | 200 k | ns | |
| RAS Hold Time | $t_{CELREH}$ | $t_{RSH}$ | 25 | — | 25 | — | 25 | — | ns | |
| CAS Hold Time | $t_{RELCEH}$ | $t_{CSH}$ | 65 | — | 75 | — | 85 | — | ns | |
| CAS Precharge to RAS Hold Time | $t_{CEHREH}$ | $t_{RHCP}$ | 45 | — | 45 | — | 50 | — | ns | |
| CAS Pulse Width | $t_{CELCEH}$ | $t_{CAS}$ | 25 | 10 k | 25 | 10 k | 25 | 10 k | ns | |
| Column Address to RAS Lead Time | $t_{AVREH}$ | $t_{RAL}$ | 35 | — | 40 | — | 45 | — | ns | |

NOTES:

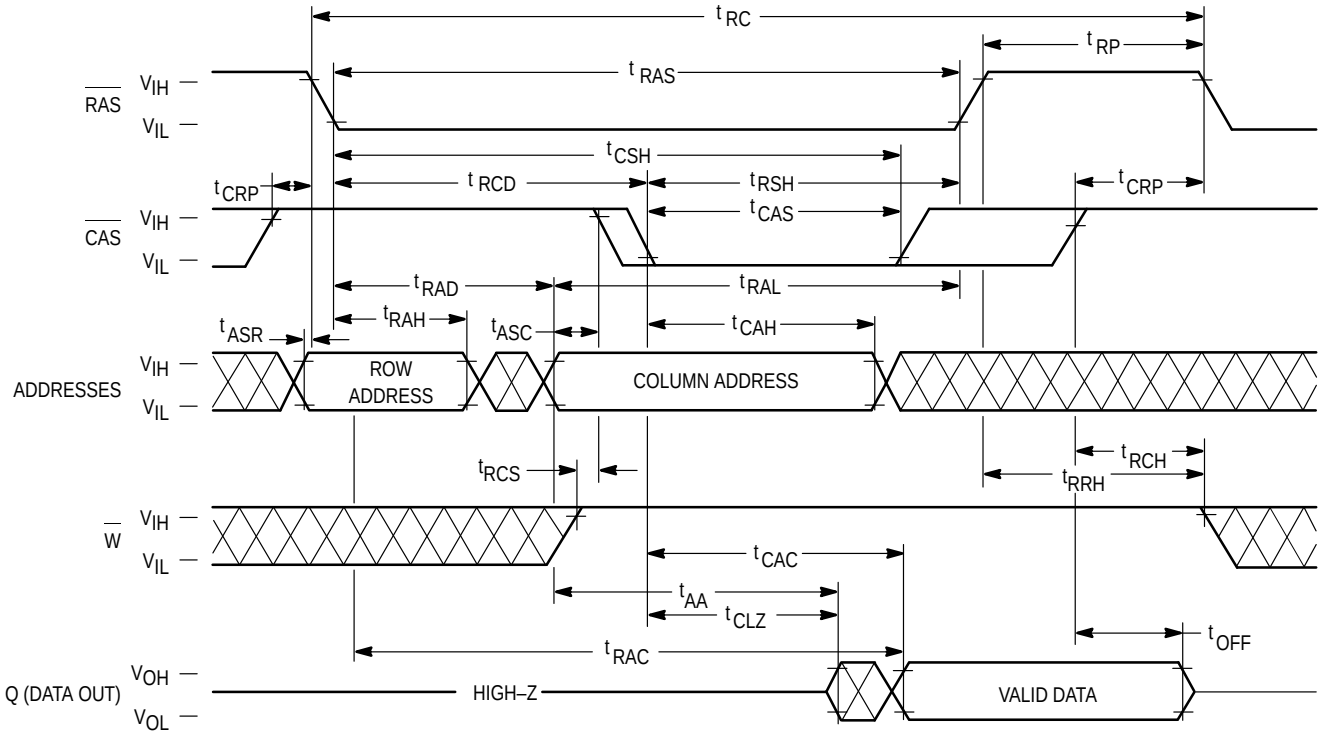
1. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$.
2. An initial pause of 200 µs is required after power–up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
5. The specifications for $t_{RC}$ (min) and $t_{RWC}$ (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ $T_A$ ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at $V_{OH}$ = 2.0 V and $V_{OL}$ = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).

## WRITE, CAS BEFORE RAS REFRESH CYCLE (TEST MODE ENTRY)

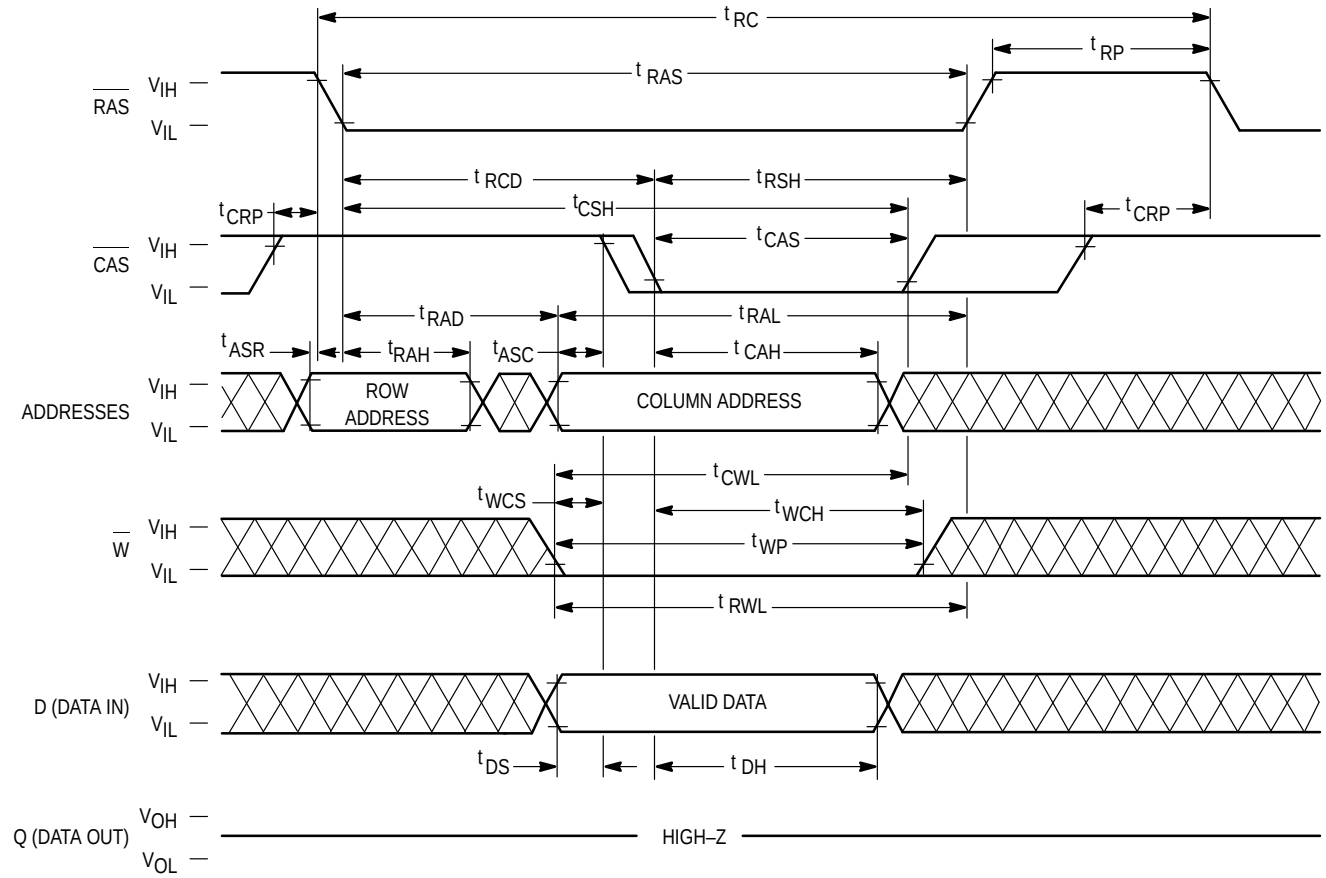
**(D and A0 – A10 are Don't Care)**



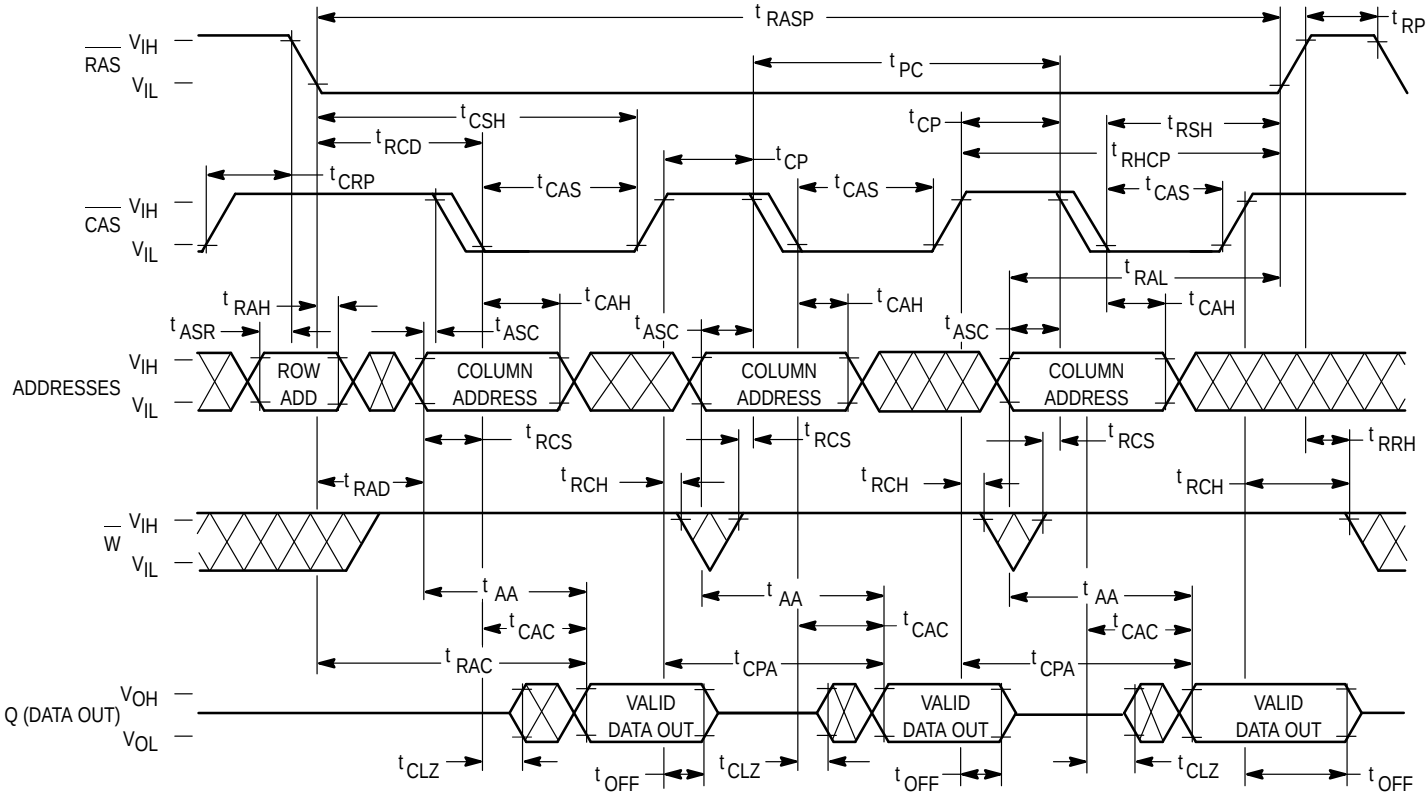
## TEST MODE — READ CYCLE



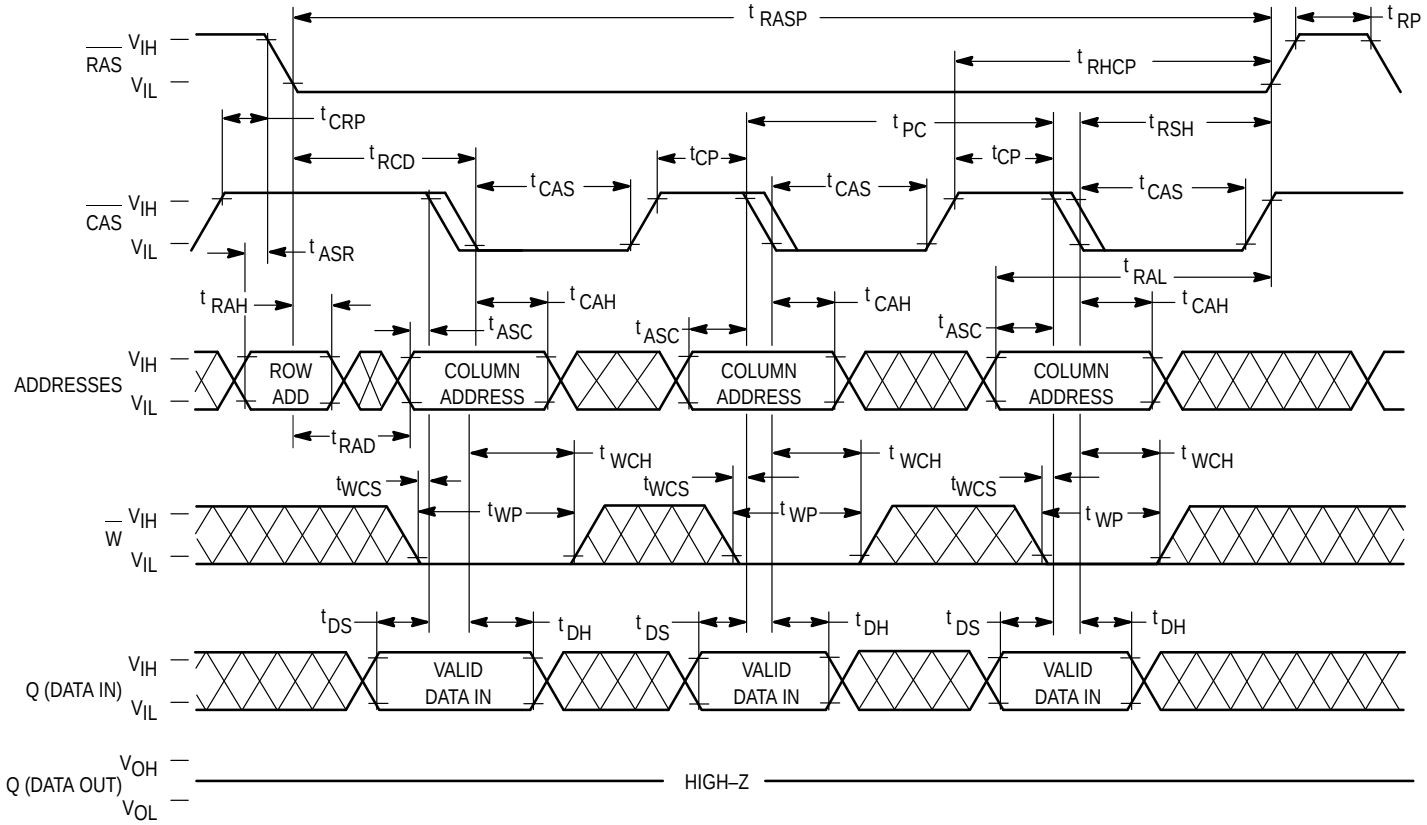

## TEST MODE — EARLY WRITE CYCLE



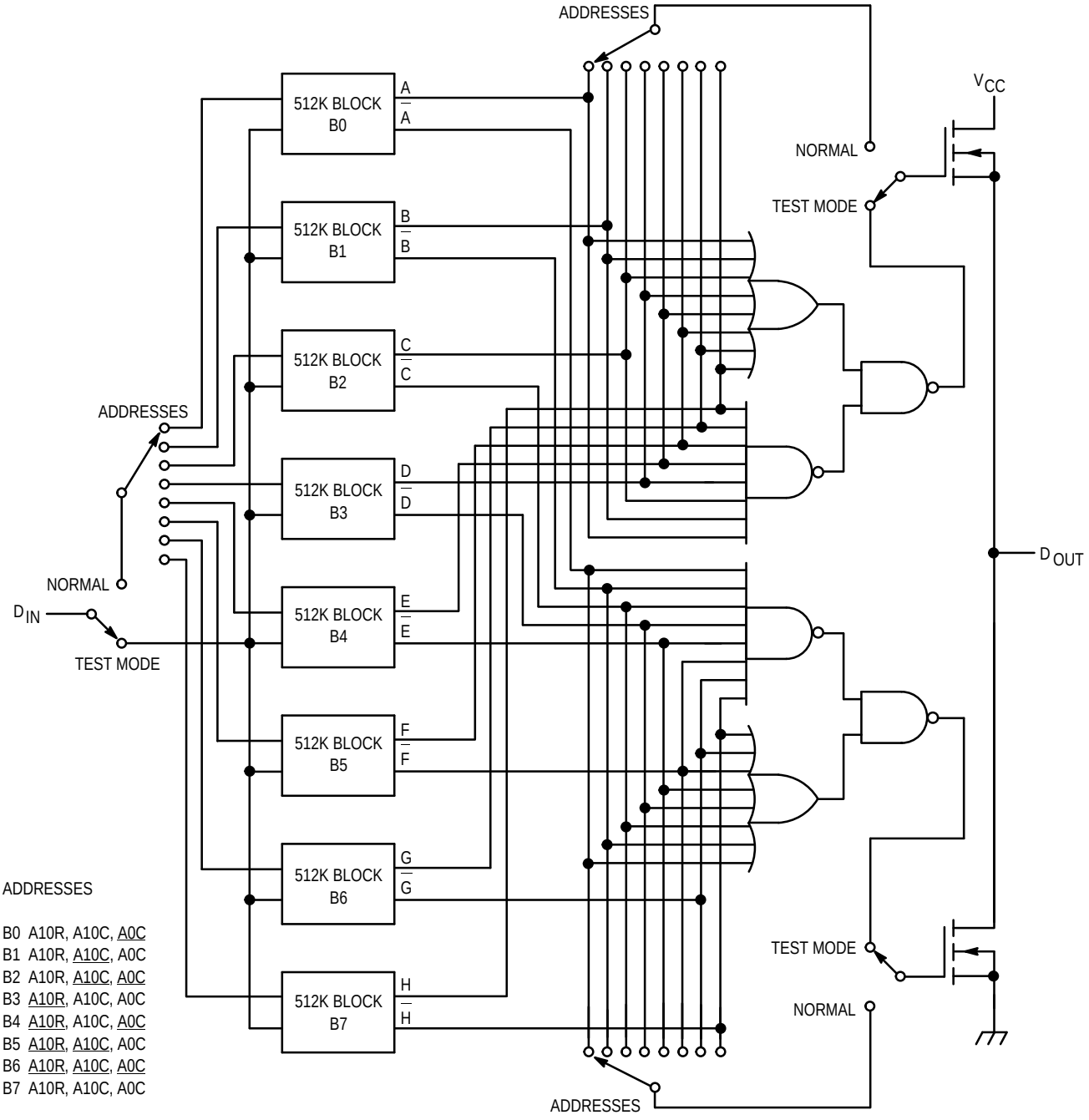
## TEST MODE — FAST PAGE MODE READ CYCLE




## TEST MODE — FAST PAGE MODE EARLY WRITE CYCLE



## TEST MODE BLOCK DIAGRAM




## ORDERING INFORMATION

**(Order by Full Part Number)**

**MCM 54100A or 5L4100A X XX XX**

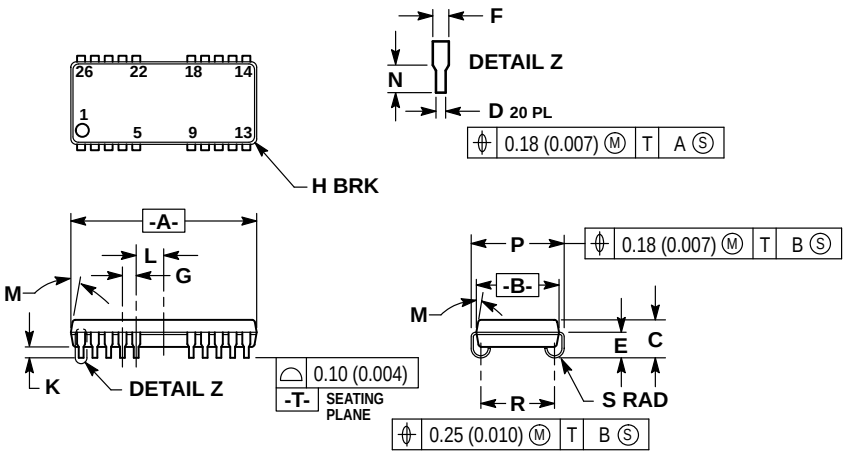
- MCM — Motorola Memory Prefix
- 54100A or 5L4100A — Part Number
- X — Package (N = 300 mil SOJ, T = 300 mil TSOP)
- XX — Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers —

| | | | |
|---|---|---|---|
| MCM54100AN60 | MCM54100AN60R2 | MCM54100AT60 | MCM54100AT60R2 |
| MCM54100AN70 | MCM54100AN70R2 | MCM54100AT70 | MCM54100AT70R2 |
| MCM54100AN80 | MCM54100AN80R2 | MCM54100AT80 | MCM54100AT80R2 |
| MCM5L4100AN60 | MCM5L4100AN60R2 | MCM5L4100AT60 | MCM5L4100AT60R2 |
| MCM5L4100AN70 | MCM5L4100AN70R2 | MCM5L4100AT70 | MCM5L4100AT70R2 |
| MCM5L4100AN80 | MCM5L4100AN80R2 | MCM5L4100AT80 | MCM5L4100AT80R2 |

## PACKAGE DIMENSIONS

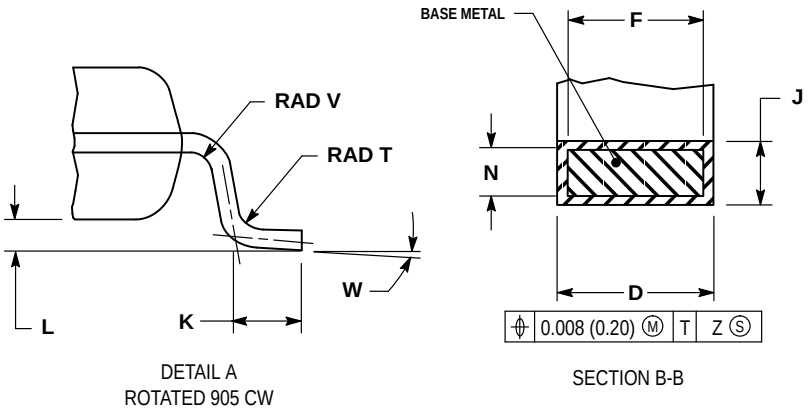
**N PACKAGE**
**300 MIL SOJ**
**CASE 822–03**

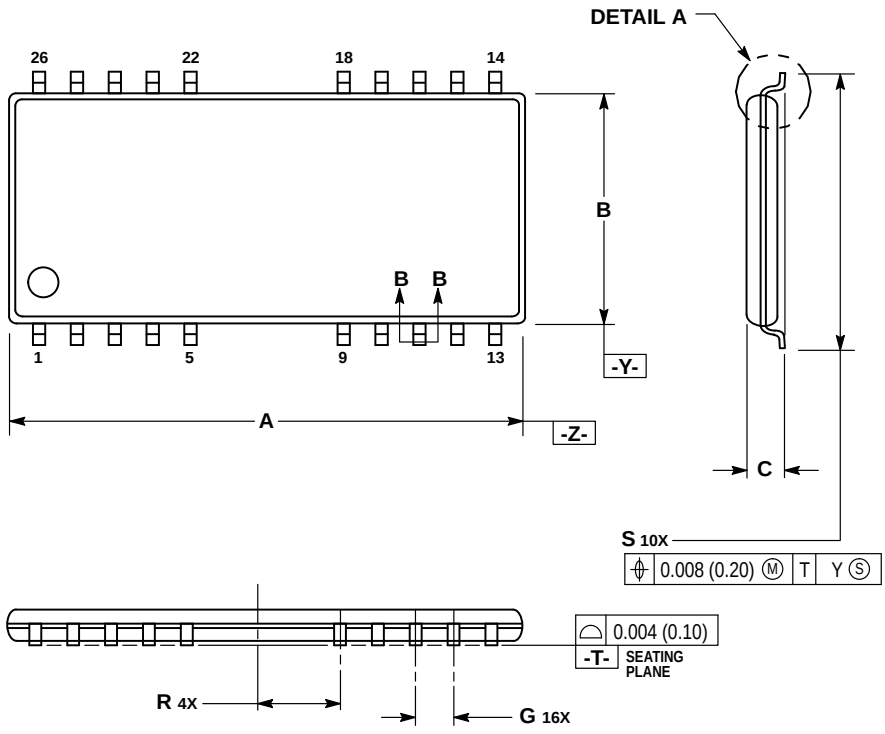



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIM R TO BE DETERMINED AT DATUM -T-.
5. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 6, 7, 8, 19, 20, & 21 ARE NOT USED.
6. 822-01 AND -02 OBSOLETE, NEW STANDARD 822-03.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 17.02 | 17.27 | 0.670 | 0.680 |
| B | 7.50 | 7.74 | 0.295 | 0.305 |
| C | 3.26 | 3.75 | 0.128 | 0.148 |
| D | 0.39 | 0.50 | 0.015 | 0.020 |
| E | 2.24 | 2.48 | 0.088 | 0.098 |
| F | 0.67 | 0.81 | 0.026 | 0.032 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | — | 0.50 | — | 0.020 |
| K | 0.89 | 1.14 | 0.035 | 0.045 |
| L | 2.54 BSC | | 0.100 BSC | |
| M | 0° | 10° | 0° | 10° |
| N | 0.89 | 1.14 | 0.035 | 0.045 |
| P | 8.39 | 8.63 | 0.330 | 0.340 |
| R | 6.61 | 6.98 | 0.260 | 0.275 |
| S | 0.77 | 1.01 | 0.030 | 0.040 |

**T PACKAGE**
**300 MIL TSOP**
**CASE 892–01**




NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.006 (0.15) PER SIDE.
4. DIMENSION D DOES NOT INCLUDE DAM BAR PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.007 (0.18), TOTAL, IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 17.05 | 17.25 | 0.671 | 0.679 |
| B | 7.52 | 7.72 | 0.296 | 0.304 |
| C | — | 1.27 | — | 0.050 |
| D | 0.33 | 0.48 | 0.013 | 0.019 |
| F | 0.33 | 0.43 | 0.013 | 0.017 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.12 | 0.20 | 0.005 | 0.008 |
| K | 0.41 | 0.58 | 0.016 | 0.023 |
| L | 0.02 | 0.18 | 0.001 | 0.007 |
| N | 0.11 | 0.16 | 0.004 | 0.006 |
| R | 2.54 BSC | | 0.100 BSC | |
| S | 9.05 | 9.39 | 0.356 | 0.370 |
| T | 0.10 REF | | 0.004 REF | |
| V | 0.10 REF | | 0.004 REF | |
| W | 0° | 5° | 0° | 5° |



**How to reach us:**
**USA / EUROPE**: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

**MFAX**: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
**INTERNET**: http://Design–NET.com

**JAPAN**: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

**HONG KONG**: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298