

Advance Information

16M CMOS Wide DRAM Family

EDO, 1M x 16, 1K, and 4K Refresh

The family of 16M Dynamic RAMs is fabricated using 0.50 μ CMOS high-speed silicon-gate process technology. It includes devices organized as 1,048,576 sixteen-bit words. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The x16 with 4096 cycle refresh (MCM516165B) require 12 address lines (12 rows, 8 columns), while the x16 device with 1024 cycle refresh (MCM518165B) require only 10 address lines (10 rows, 10 columns).

These devices are packaged in a standard 400 mil J-lead small outline package (SOJ) and a standard 400 mil thin-small-outline package (TSOP).

- Single 5 V $\pm$ 10% Power Supply
- Three-State Data Outputs, x16 Configuration
- Extended Data Out (EDO)
- TTL-Compatible Inputs and Outputs
- RAS-Only Refresh
- CAS Before RAS Refresh
- Hidden Refresh
- 4096 Cycle Refresh:
MCM516165B = 64 ms
- 1024 Cycle Refresh:
MCM518165B = 16 ms
- Fast Access Time (t_{RAC}):
MCM51xxxxB-60 = 60 ns (Max)
MCM51xxxxB-70 = 70 ns (Max)
- Low Active Power Dissipation:
MCM516165B-60 = 523 mW (Max)
MCM516165B-70 = 440 mW (Max)
MCM518165B-60 = 1018 mW (Max)
MCM518165B-70 = 853 mW (Max)
- Low Standby Power Dissipation:
All Devices = 11 mW (Max, TTL Levels)
All Devices = 5.5 mW (Max, CMOS Levels)

1M x 16

MCM516165B

EDO

4096 Cycle Refresh

MCM518165B

EDO

1024 Cycle Refresh



J PACKAGE
400 MIL SOJ
CASE 986A-01



T PACKAGE
400 MIL TSOP II
CASE 985A-01

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PIN ASSIGNMENTS

400 MIL SOJ

V _{CC}	1	42	V _{SS}
DQ0	2	41	DQ15
DQ1	3	40	DQ14
DQ2	4	39	DQ13
DQ3	5	38	DQ12
V _{CC}	6	37	V _{SS}
DQ4	7	36	DQ11
DQ5	8	35	DQ10
DQ6	9	34	DQ9
DQ7	10	33	DQ8
NC	11	32	NC
NC	12	31	LCAS
$\overline{W}$	13	30	UCAS
RAS	14	29	G
A11R/NC*	15	28	A9R/A9*
A10R/NC*	16	27	A8R/A8*
A0	17	26	A7
A1	18	25	A6
A2	19	24	A5
A3	20	23	A4
V _{CC}	21	22	V _{SS}

400 MIL TSOP

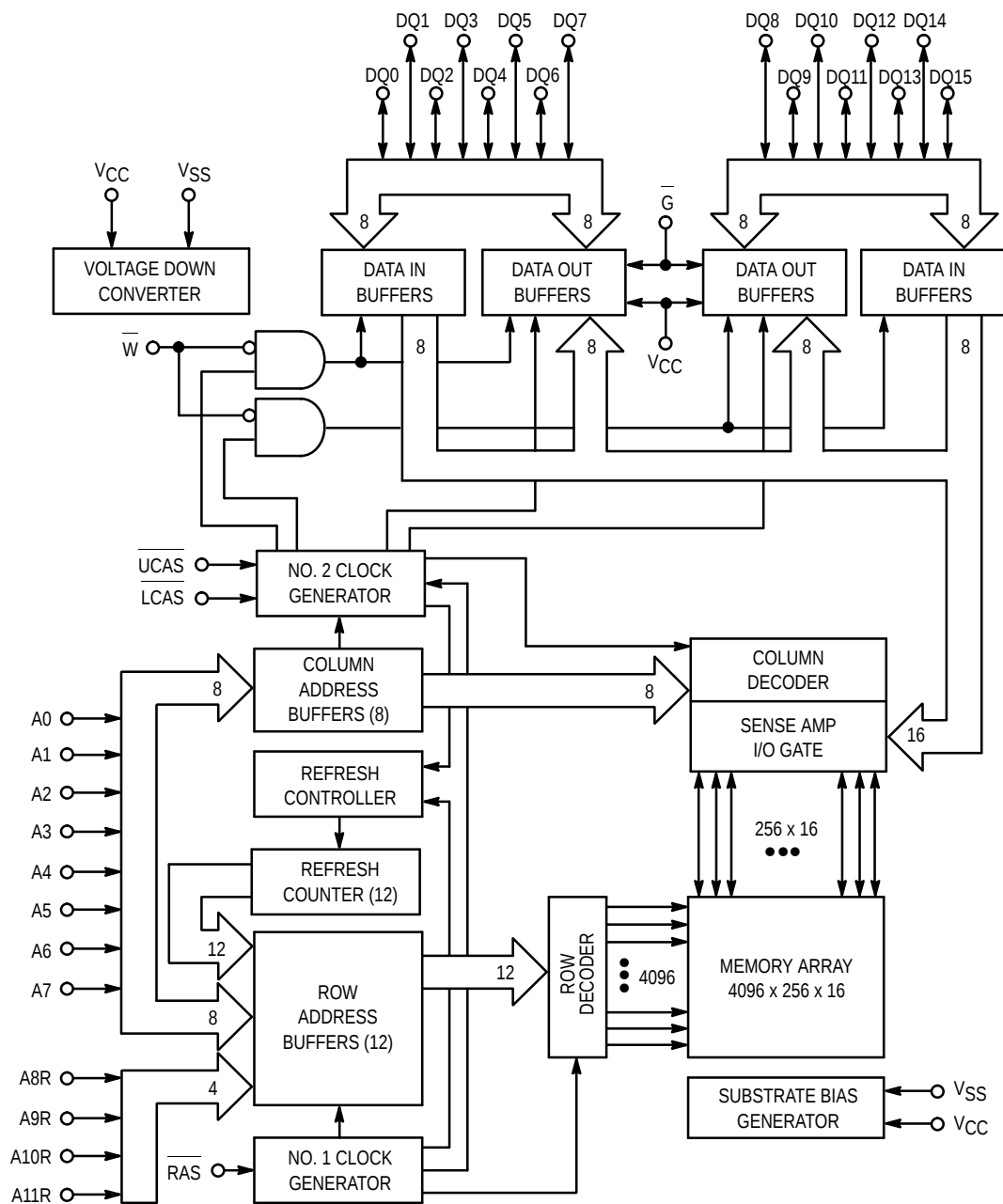
V _{CC}	1	50	V _{SS}
DQ0	2	49	DQ15
DQ1	3	48	DQ14
DQ2	4	47	DQ13
DQ3	5	46	DQ12
V _{CC}	6	45	V _{SS}
DQ4	7	44	DQ11
DQ5	8	43	DQ10
DQ6	9	42	DQ9
DQ7	10	41	DQ8
NC	11	40	NC
NC	15	36	NC
NC	16	35	LCAS
$\overline{W}$	17	34	UCAS
RAS	18	33	G
A11R/NC*	19	32	A9R/A9*
A10R/NC*	20	31	A8R/A8*
A0	21	30	A7
A1	22	29	A6
A2	23	28	A5
A3	24	27	A4
V _{CC}	25	26	V _{SS}

*4096 Cycle Refresh or 1024 Cycle Refresh (R Suffix = Row Address)

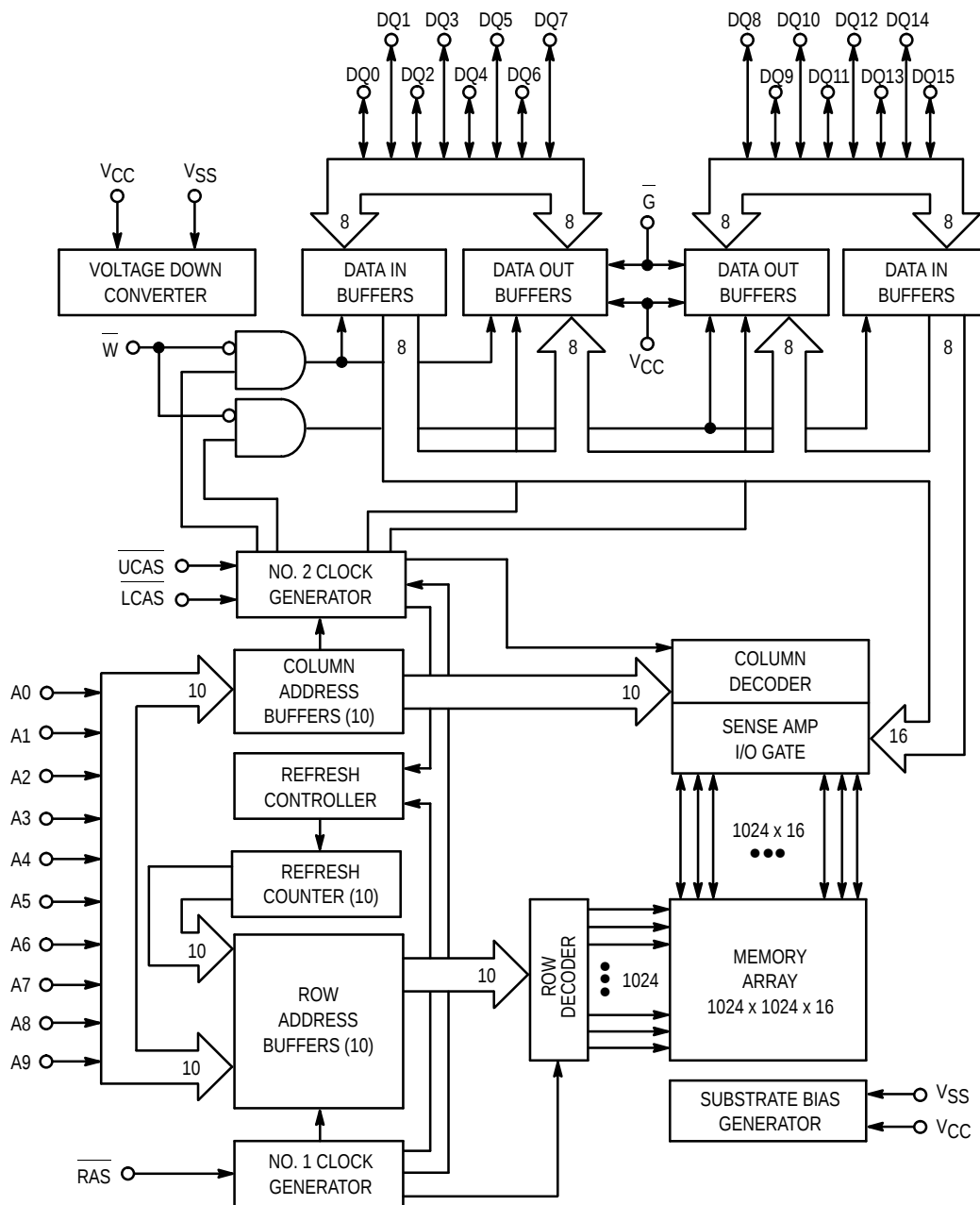
PIN NAMES	
A0 – A11	Address Input
DQ0 – DQ15	Data Input/Output
G	Output Enable
$\overline{W}$	Read/Write Enable
RAS	Row Address Strobe
LCAS	Column Address Strobe
UCAS	Column Address Strobe
V _{CC}	Power Supply (+ 5 V)
V _{SS}	Ground
NC	No Connection

BLOCK DIAGRAMS

MCM516165B BLOCK DIAGRAM
1M x 16, 4096 CYCLE REFRESH



MCM518165B BLOCK DIAGRAM
1M x 16, 1024 CYCLE REFRESH



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	- 0.5 to + 7	V
Voltage Relative to V_{SS} , Any Pin Except V_{CC}	V_{in}, V_{out}	- 0.5 to $V_{CC} + 0.5$	V
Data Out Current	I_{out}	50	mA
Soldering Temperature x Time	T_{solder}	260 x 10	°C x s
Power Dissipation	P_D	1.0 1.3	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	- 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $T_A = 0 \text{ to } 70^\circ\text{C}$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	$V_{CC} + 0.5^*$	V
Logic Low Voltage, All Inputs	V_{IL}	- 0.5**	—	0.8	V

* $V_{CC} + 2.0 \text{ V}$ at pulse width $\leq 20 \text{ ns}$.

** -2.0 V at pulse width $\leq 20 \text{ ns}$.

DC CHARACTERISTICS AND SUPPLY CURRENTS (All voltages referenced to V_{SS})

Characteristic	Symbol	MCM516165B-60 MCM518165B-60		MCM516165B-70 MCM518165B-70		Unit	Notes
		Min	Max	Min	Max		
V_{CC} Power Supply Current ($t_{RC} = t_{RC} \text{ Min}$) MCM516165B-xx MCM518165B-xx	I_{CC1}	—	95 185	—	80 155	mA	1, 2
V_{CC} Power Supply Current (Standby) (RAS = UCAS = LCAS = V_{IH})	I_{CC2}	—	2	—	2	mA	
V_{CC} Power Supply Current During RAS Only Refresh Cycles (UCAS = LCAS = V_{IH} , $t_{RC} = t_{RC} \text{ Min}$) MCM516165B-xx MCM518165B-xx	I_{CC3}	—	95 185	—	80 155	mA	1, 2
V_{CC} Power Supply Current During Extended Data Out Cycle (RAS = V_{IL})	I_{CC4}	—	90 120	—	80 110	mA	1, 2
V_{CC} Power Supply Current (Standby) (RAS = UCAS = LCAS = $V_{CC} - 0.2 \text{ V}$)	I_{CC5}	—	1	—	1	mA	
V_{CC} Power Supply Current During CAS Before RAS Refresh Cycle ($t_{RC} = t_{RC} \text{ Min}$) MCM516165B-xx MCM518165B-xx	I_{CC6}	—	95 185	—	80 155	mA	1, 2
Input Leakage Current ($0 \text{ V} \leq V_{in} \leq V_{CC}$)	$I_{kg(I)}$	-10	10	-10	10	μA	
Output Leakage Current ($0 \text{ V} \leq V_{out} \leq V_{CC}$, Output Disable)	$I_{kg(O)}$	-10	10	-10	10	μA	
Output High Voltage ($I_{OH} = -2 \text{ mA}$)	V_{OH}	2.4	—	2.4	—	V	
Output Low Voltage ($I_{OL} = 2 \text{ mA}$)	V_{OL}	—	0.4	—	0.4	V	

NOTES:

- Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
- Address may be changed once or less while RAS = V_{IL} . In the case of I_{CC4} , it can be changed once or less during t_{EPC} .

CAPACITANCE (f = 1.0 MHz, $T_A = 25^\circ\text{C}$, $V_{CC} = 5 \text{ V}$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Max	Unit
Input Capacitance A0 - A11 G, RAS, UCAS, LCAS, W	C_{in}	5	pF
		7	
Input/Output Capacitance (UCAS, LCAS = V_{IH} to Disable Output) DQ0 - DQ15	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I \Delta t / \Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

ALL DEVICES: READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM516165B-60 MCM518165B-60		MCM516165B-70 MCM518165B-70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t _{RELREL}	t _{RC}	104	—	124	—	ns	5
Read-Write Cycle Time	t _{RELREL}	t _{RWC}	135	—	157	—	ns	5
Access Time from RAS	t _{RELQV}	t _{RAC}	—	60	—	70	ns	6, 7, 11, 12
Access Time from CAS	t _{CELQV}	t _{CAC}	—	17	—	20	ns	6, 8, 11
Access Time from Column Address	t _{AVQV}	t _{AA}	—	30	—	35	ns	6, 9, 12
Access Time from Precharge CAS	t _{CEHQV}	t _{CPA}	—	35	—	40	ns	6
CAS to Output in Low-Z	t _{CELQX}	t _{CLZ}	0	—	0	—	ns	
Output Buffer and Turn-Off Delay	t _{CEHQZ}	t _{OFF}	0	15	0	15	ns	10, 16
Transition Time (Rise and Fall)	t _T	t _T	1	50	1	50	ns	1
RAS Precharge Time	t _{REHREL}	t _{RP}	40	—	50	—	ns	
RAS Pulse Width	t _{RELREH}	t _{RAS}	60	10 k	70	10 k	ns	
RAS Hold Time	t _{CELREH}	t _{RSH}	10	—	12	—	ns	
CAS Hold Time	t _{RELCEH}	t _{CSH}	40	—	50	—	ns	
CAS Pulse Width	t _{CELCEH}	t _{CAS}	10	10 k	12	10 k	ns	
RAS to CAS Delay Time	t _{RELCEL}	t _{RCD}	14	43	14	50	ns	11
RAS to Column Address Delay Time	t _{RELAV}	t _{RAD}	12	30	12	35	ns	12
CAS to RAS Precharge Time	t _{CEHREL}	t _{CRP}	5	—	5	—	ns	
CAS Precharge Time	t _{CEHCEL}	t _{CP}	10	—	10	—	ns	
Row Address Setup Time	t _{AVREL}	t _{ASR}	0	—	0	—	ns	
Row Address Hold Time	t _{RELAX}	t _{RAH}	10	—	10	—	ns	
Column Address Setup Time	t _{AVCEL}	t _{ASC}	0	—	0	—	ns	
Column Address Hold Time	t _{CELAX}	t _{CAH}	10	—	12	—	ns	
Column Address to RAS Lead Time	t _{AVREH}	t _{RAL}	30	—	35	—	ns	
Read Command Setup Time	t _{WHCEL}	t _{RCS}	0	—	0	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 RAS cycles before proper device operation is guaranteed. If using the internal refresh counter, a minimum of 8 CAS before RAS refresh cycles, instead of 8 RAS only refresh cycles are required.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min), t_{RWC} (min), and t_{EPC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that t_{RCD} ≤ t_{RCD} (max).
8. Assumes that t_{RCD} ≥ t_{RCD} (max).
9. Assumes that t_{RAD} ≥ t_{RAD} (max).
10. t_{OFF} (max), t_{REZ} (max), t_{WEZ} (max), and t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

ALL DEVICES: READ, WRITE, AND READ-WRITE CYCLES (Continued)

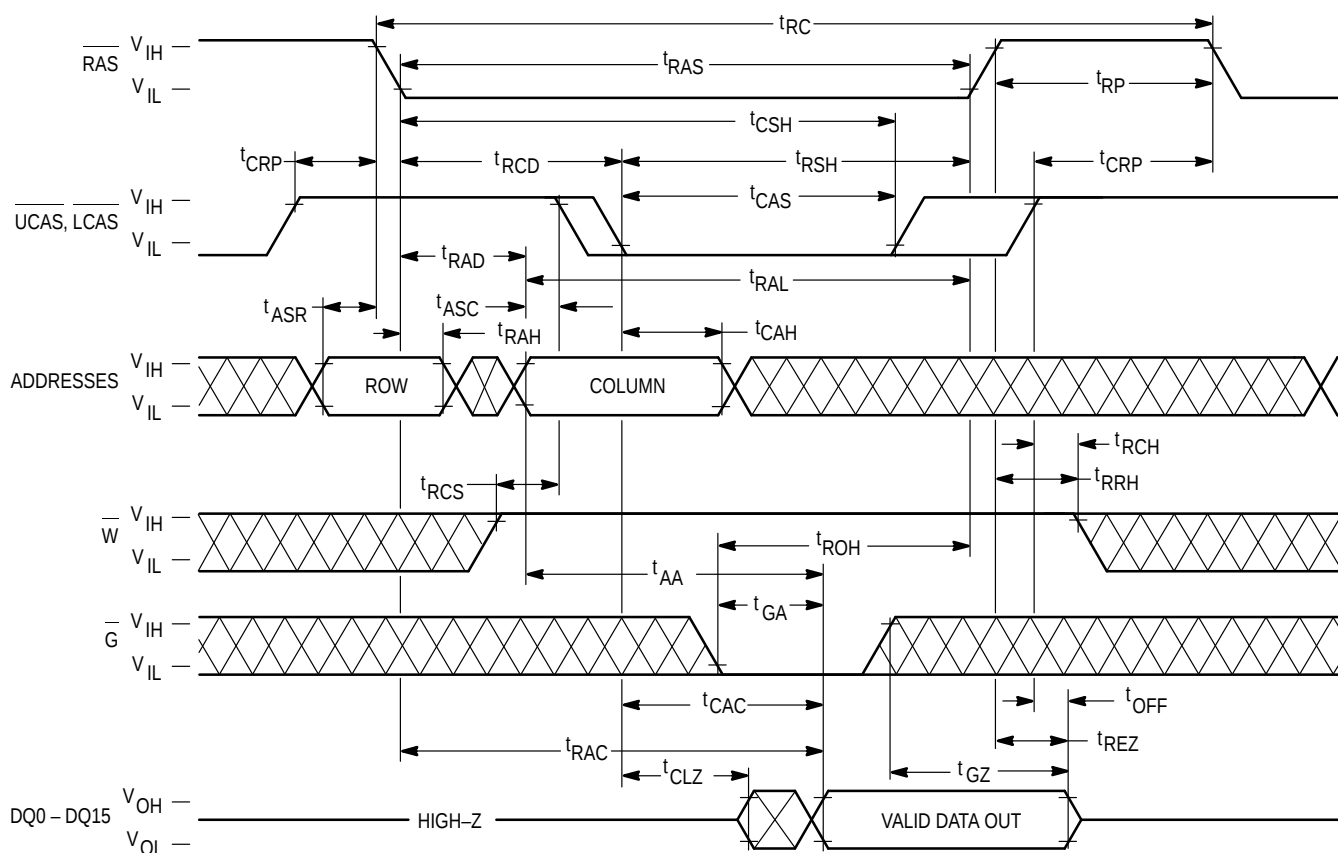
Parameter	Symbol		MCM516165B-60 MCM518165B-60		MCM516165B-70 MCM518165B-70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Read Command Hold Time Referenced to CAS	t _{CEHWX}	t _{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to RAS	t _{REHWX}	t _{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to CAS	t _{CELWH}	t _{WCH}	10	—	12	—	ns	
Write Command Pulse Width	t _{WLWH}	t _{WP}	10	—	12	—	ns	
Write Command to RAS Lead Time	t _{WLREH}	t _{RWL}	10	—	12	—	ns	
Write Command to CAS Lead Time	t _{WLCEH}	t _{CWL}	10	—	12	—	ns	
Data In Setup Time	t _{DVCEL}	t _{DS}	0	—	0	—	ns	14
Data In Hold Time	t _{CELDX}	t _{DH}	10	—	12	—	ns	14
Refresh Period	MCM516165B MCM518165B	t _{RVRV}	t _{RFSH}	— 64 16	— 64 16	— 64 16	ms	
Write Command Setup Time	t _{WLCEL}	t _{WCS}	0	—	0	—	ns	15
CAS to Write Delay	t _{CELWL}	t _{CWD}	36	—	39	—	ns	15
RAS to Write Delay	t _{RELWL}	t _{RWD}	79	—	89	—	ns	15
Column Address to Write Delay	t _{AVWL}	t _{AWD}	49	—	54	—	ns	15
CAS Precharge to Write Delay	t _{CEHWL}	t _{CPWD}	54	—	59	—	ns	15
CAS Setup Time for CAS Before RAS Refresh	t _{CELCEL}	t _{CSR}	5	—	5	—	ns	
CAS Hold Time for CAS Before RAS Refresh	t _{RELCEH}	t _{CHR}	10	—	15	—	ns	
RAS Precharge to CAS Active Time	t _{REHCEL}	t _{RPC}	5	—	5	—	ns	
CAS Precharge Time for CAS Before RAS Counter Test	t _{CEHCEL}	t _{CPT}	20	—	20	—	ns	
RAS Hold Time Referenced to G	t _{GLREH}	t _{ROH}	10	—	10	—	ns	
G Access Time	t _{GLQV}	t _{GA}	—	15	—	20	ns	6
G to Data Delay	t _{GLHDX}	t _{GD}	15	—	15	—	ns	
Output Buffer Turn-Off Delay from G	t _{GHQZ}	t _{GZ}	0	15	0	15	ns	10
G Command Hold Time	t _{WLGL}	t _{GH}	10	—	12	—	ns	
Output Disable Setup Time	t _{GHCEL}	t _{GDS}	0	—	0	—	ns	
RAS Hold Time from CAS Precharge (Extended Data Out)	t _{CEHREH}	t _{RHCP}	35	—	40	—	ns	
RAS Pulse Width (Extended Data Out)	t _{RELREH}	t _{RASP}	60	100 k	70	100 k	ns	
RAS to Next CAS Delay (Extended Data Out)	t _{RELCEL}	t _{RNCD}	60	—	70	—	ns	
Extended Data Out Cycle Time	t _{CELCEL}	t _{EPC}	25	—	30	—	ns	
Extended Data Out Read-Write Cycle Time	t _{CELCEL}	t _{ERWC}	68	—	75	—	ns	
Output Data Hold Time	t _{CELQZ}	t _{COH}	5	—	5	—	ns	
Output Buffer Turn-Off Delay from RAS	t _{REHQZ}	t _{REZ}	0	15	0	15	ns	10, 16
Output Buffer Turn-Off Delay from WE	t _{WLQZ}	t _{WEZ}	0	15	0	15	ns	10
WE to Data Delay	t _{WLDV}	t _{WED}	15	—	15	—	ns	
G to Pulse Width	t _{GLGH}	t _G	15	—	20	—	ns	
G Precharge Time	t _{GHGL}	t _{GP}	10	—	12	—	ns	
CAS to G Precharge Time	t _{CEHGL}	t _{CPG}	5	—	5	—	ns	

NOTES:

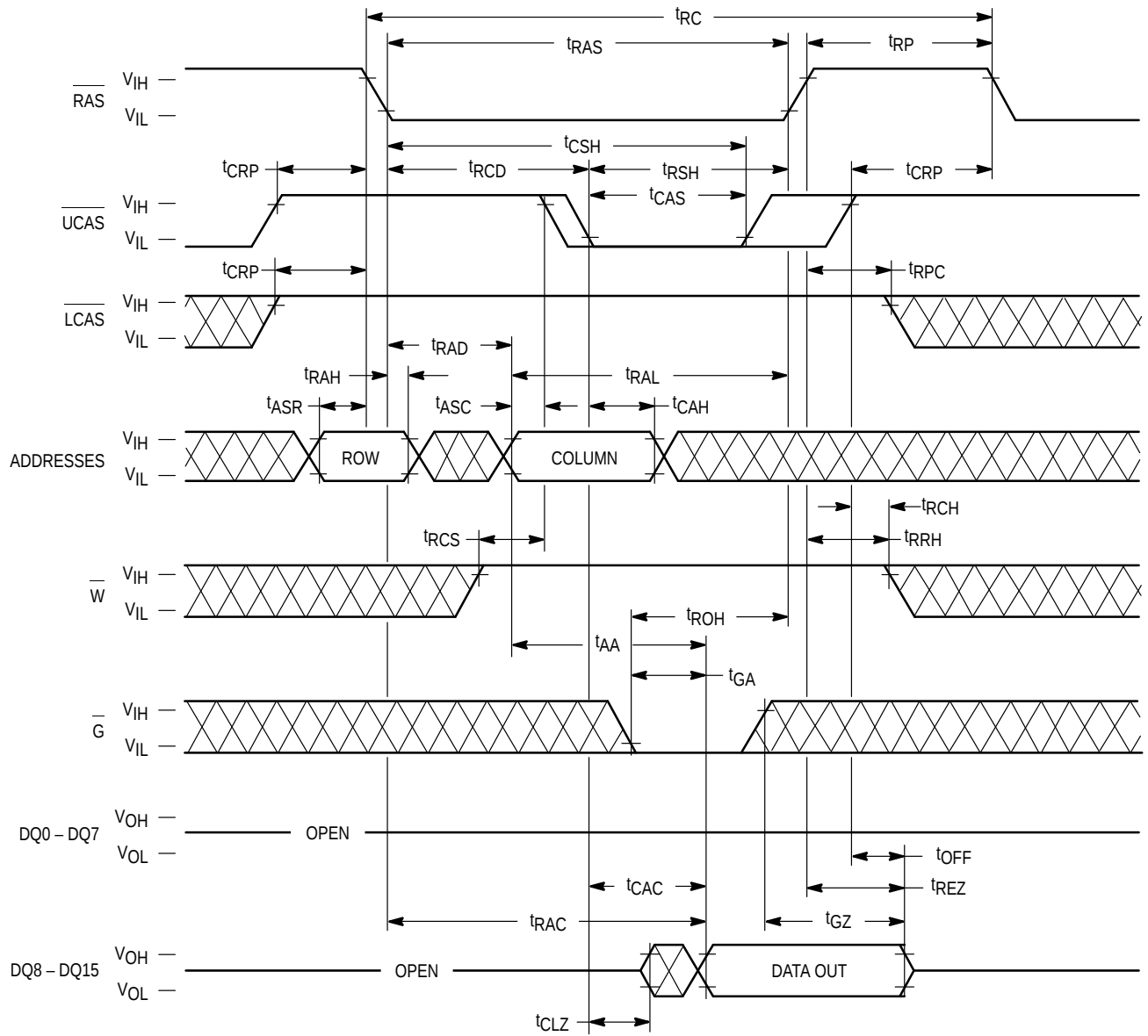
- Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
- These parameters are referenced to UCAS or LCAS leading edge in early write cycles and to W leading edge in late write or read-write cycles.
- t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if t_{WCS} ≥ t_{WCS} (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if t_{CWD} ≥ t_{CWD} (min), t_{RWD} ≥ t_{RWD} (min), t_{AWD} ≥ t_{AWD} (min), and t_{CPWD} ≥ t_{CPWD} (min) (extended data out), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
- If RAS goes high before CAS goes high, the open circuit condition is controlled by CAS going high (t_{OFF}). If CAS goes high before RAS goes high, the open circuit condition is controlled by RAS going high (t_{REZ}).

TIMING DIAGRAMS

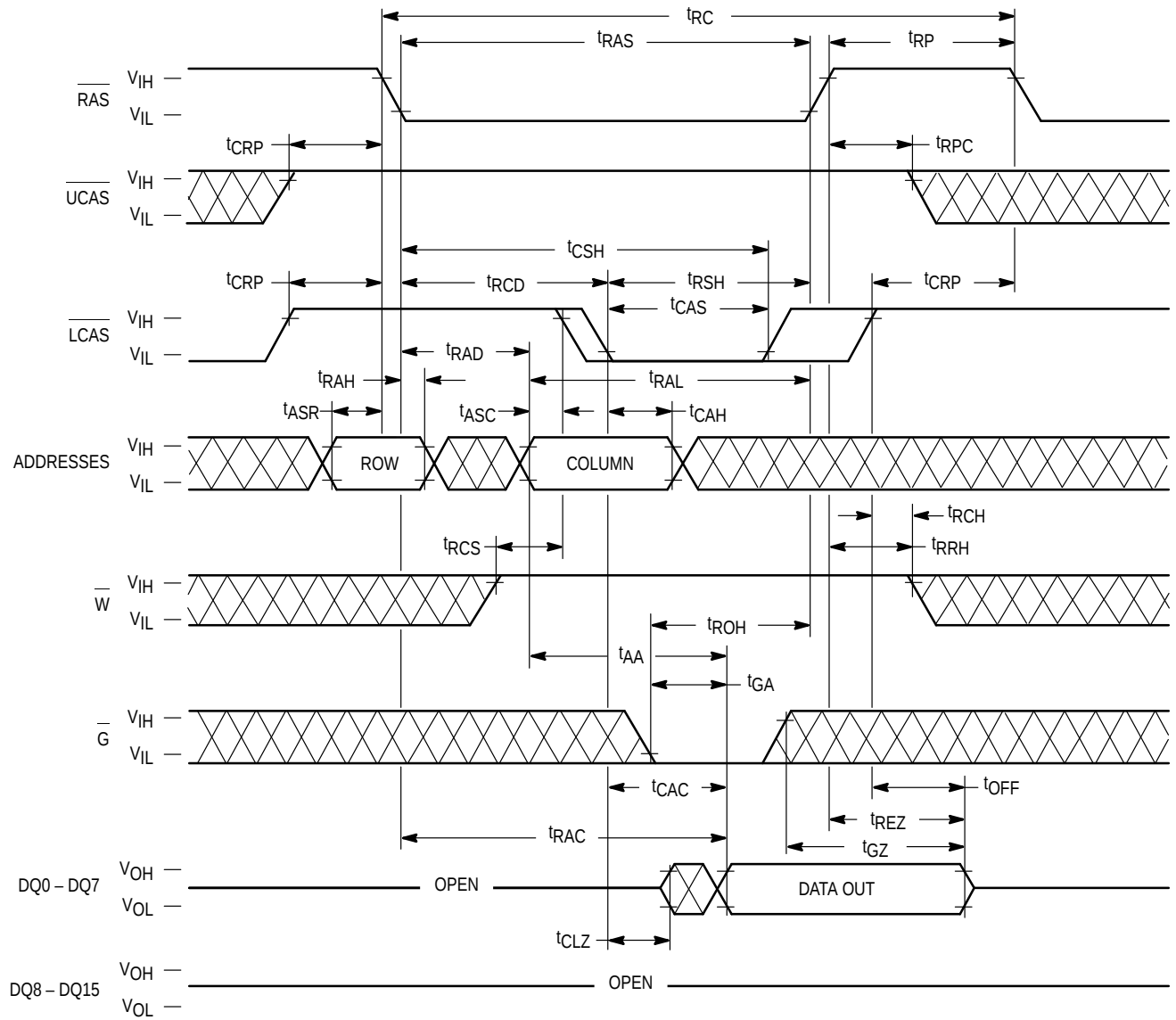
READ CYCLE



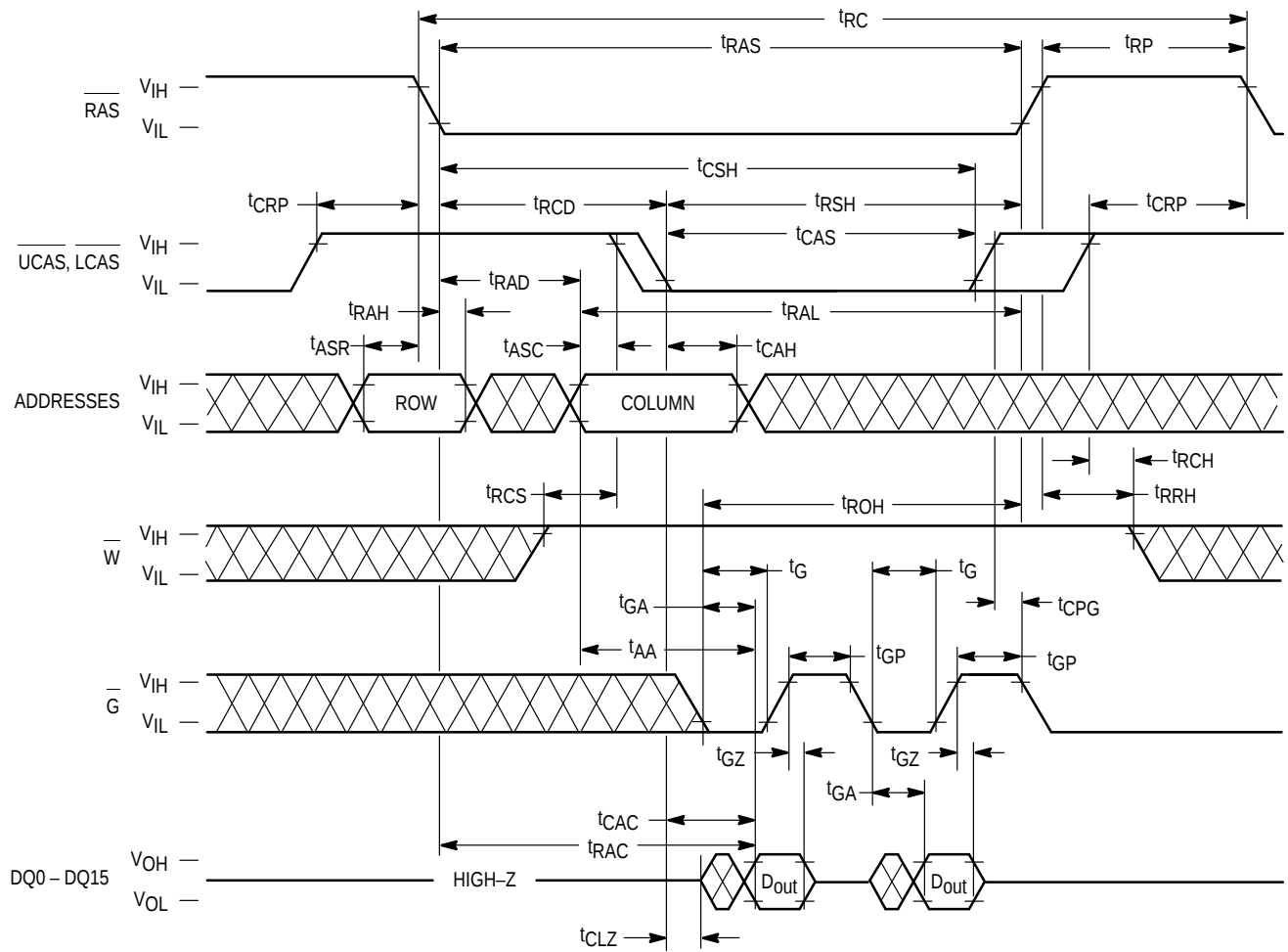
UPPER BYTE READ CYCLE



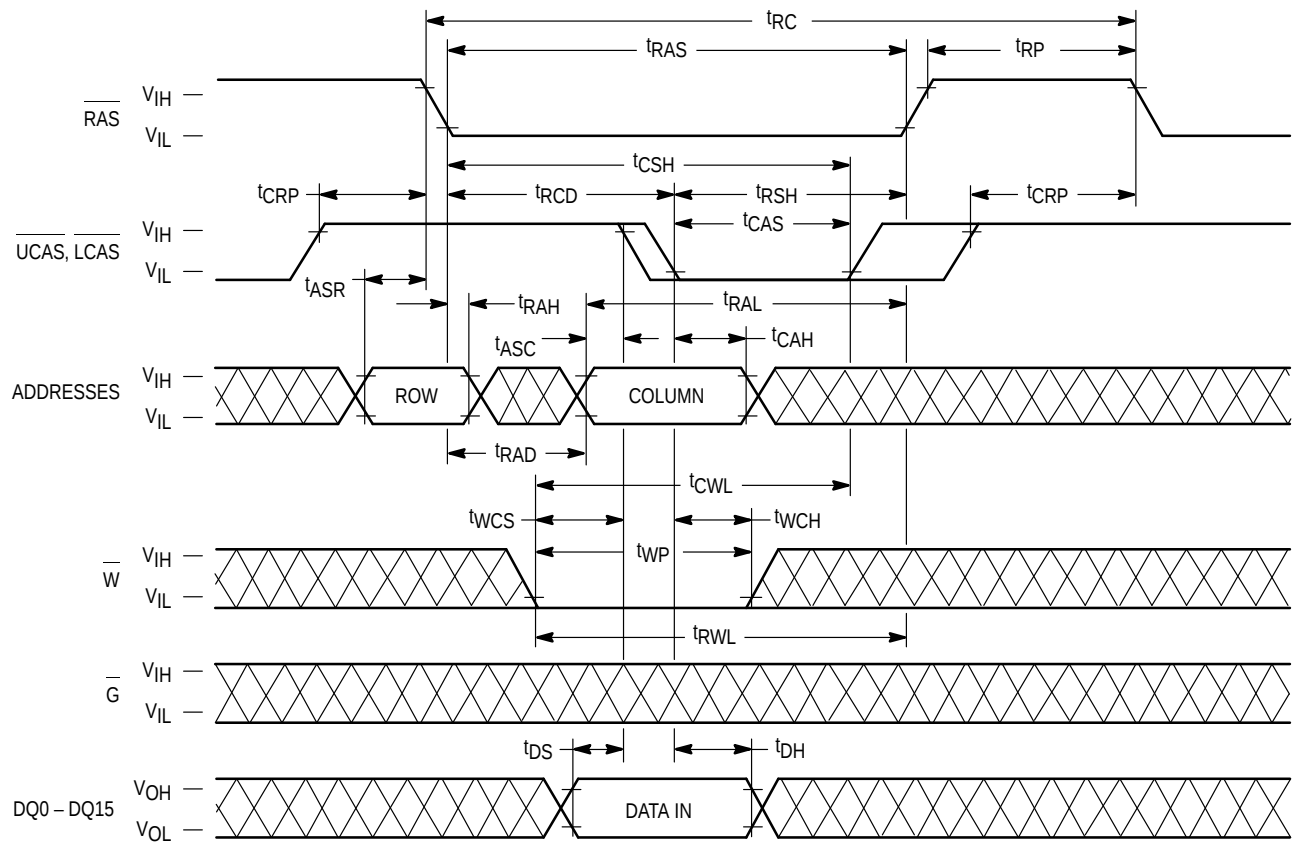
LOWER BYTE READ CYCLE



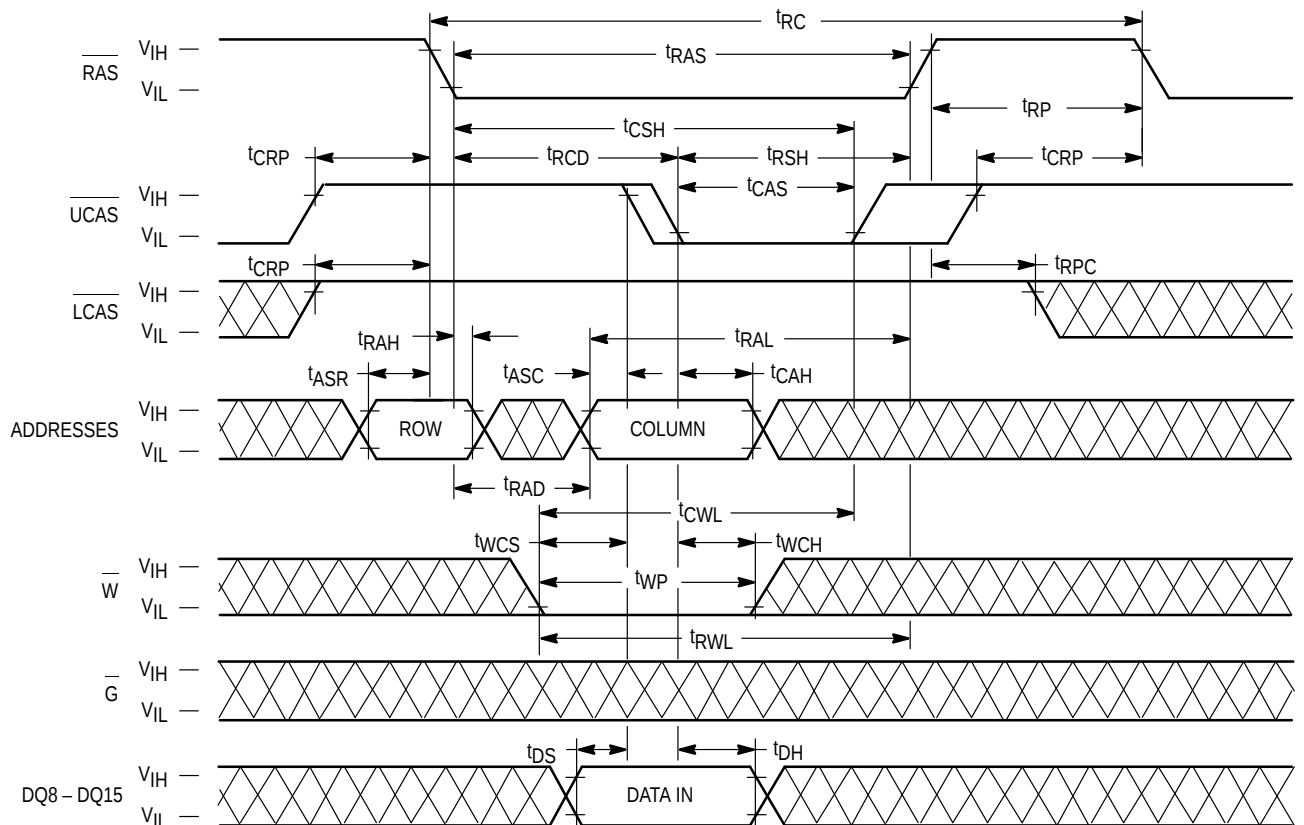
READ CYCLE ($\overline{G}$ CONTROLLED READ)



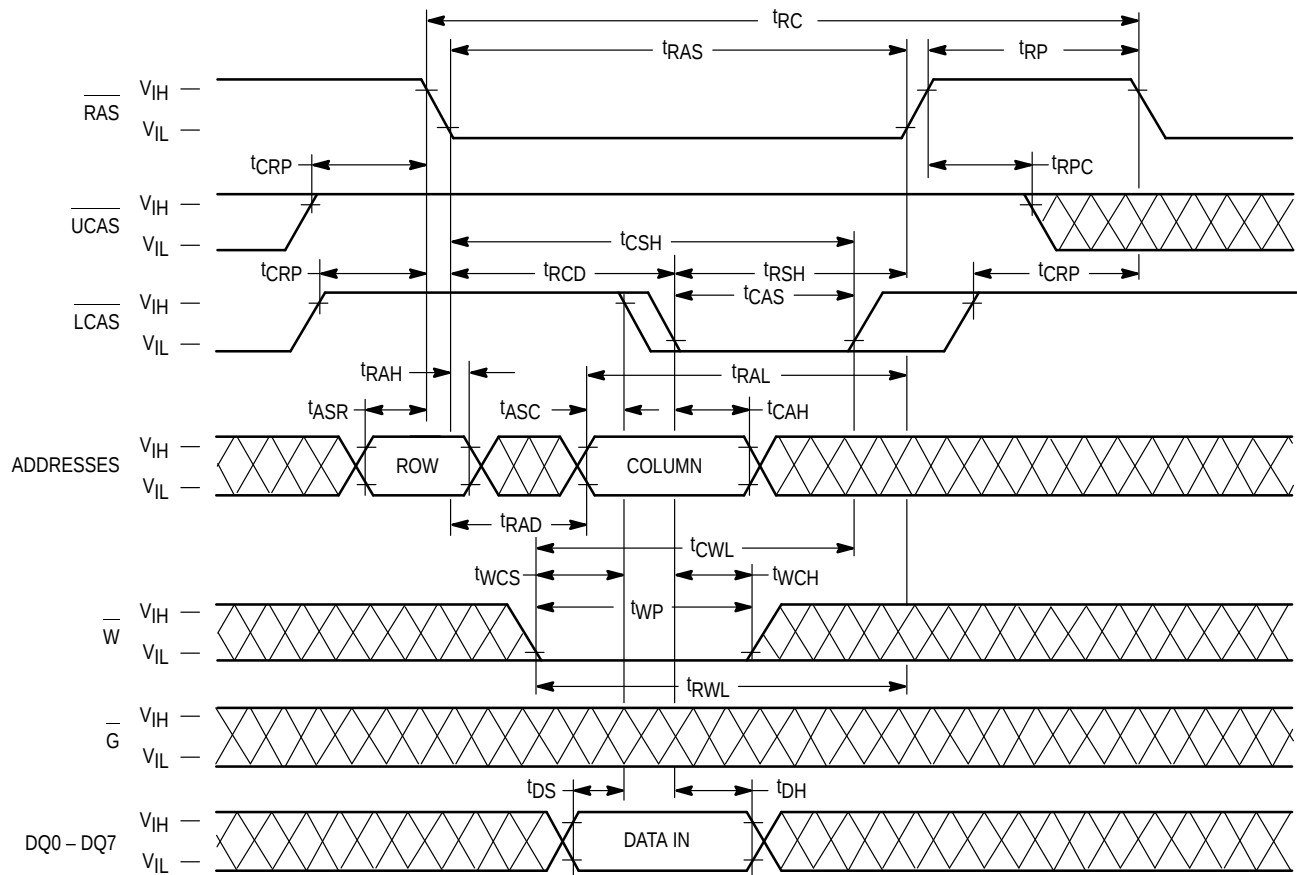
WRITE CYCLE (EARLY WRITE)



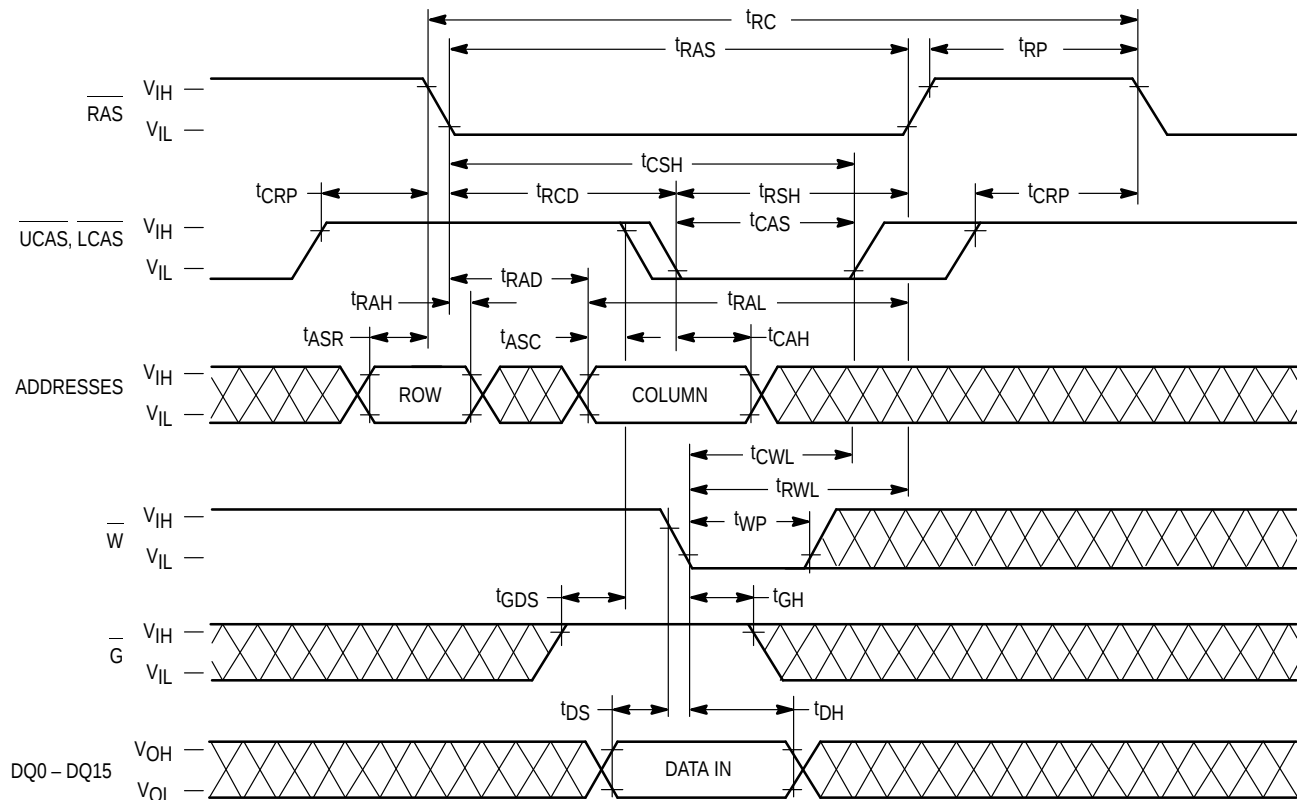
UPPER BYTE WRITE CYCLE (EARLY WRITE)



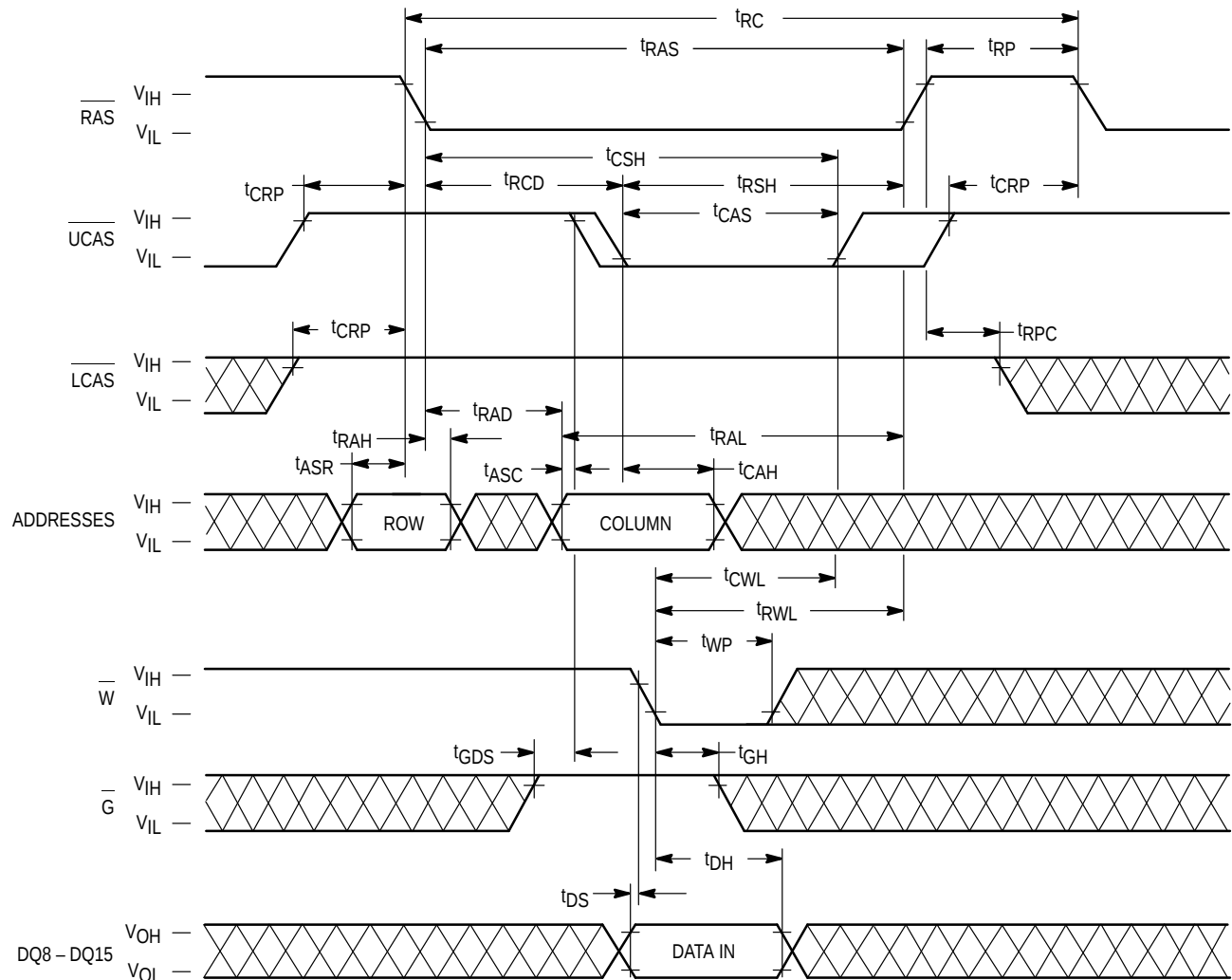
LOWER BYTE WRITE CYCLE (EARLY WRITE)



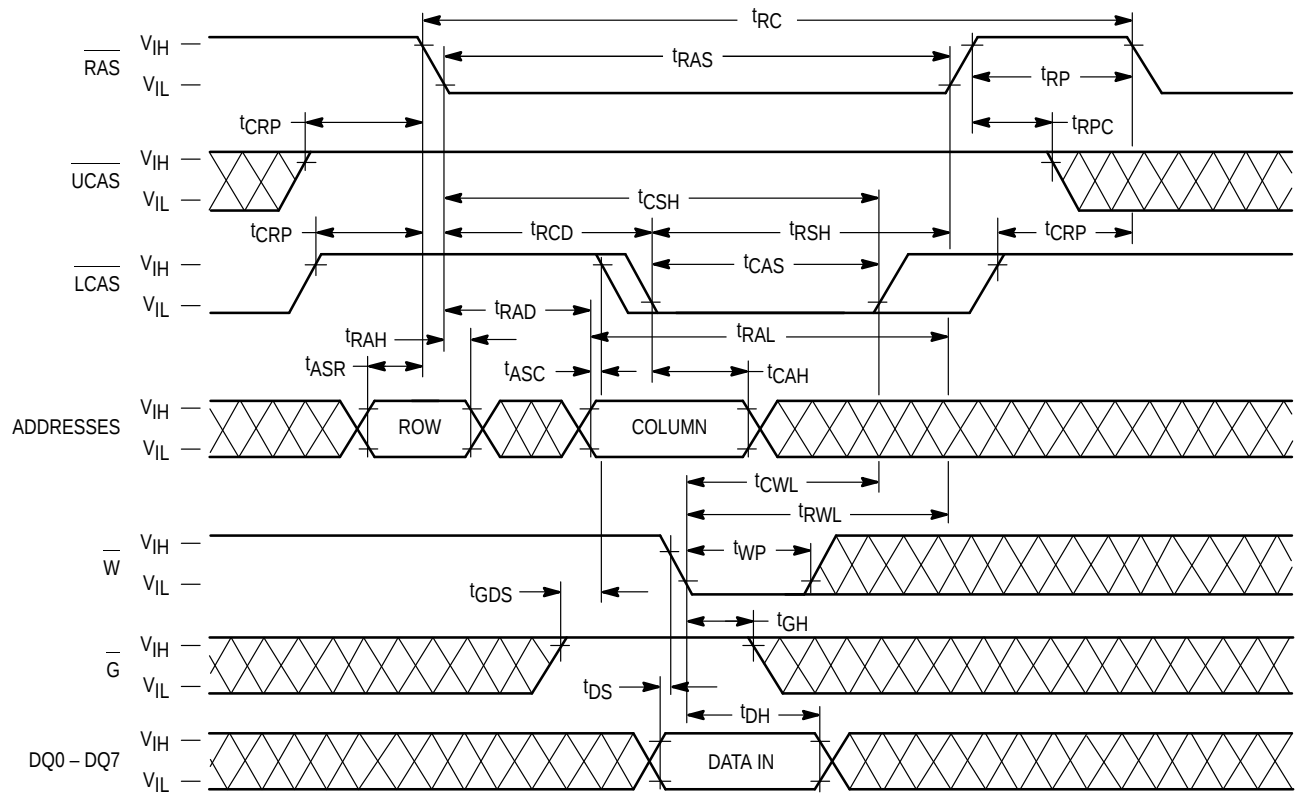
WRITE CYCLE (G CONTROLLED WRITE)



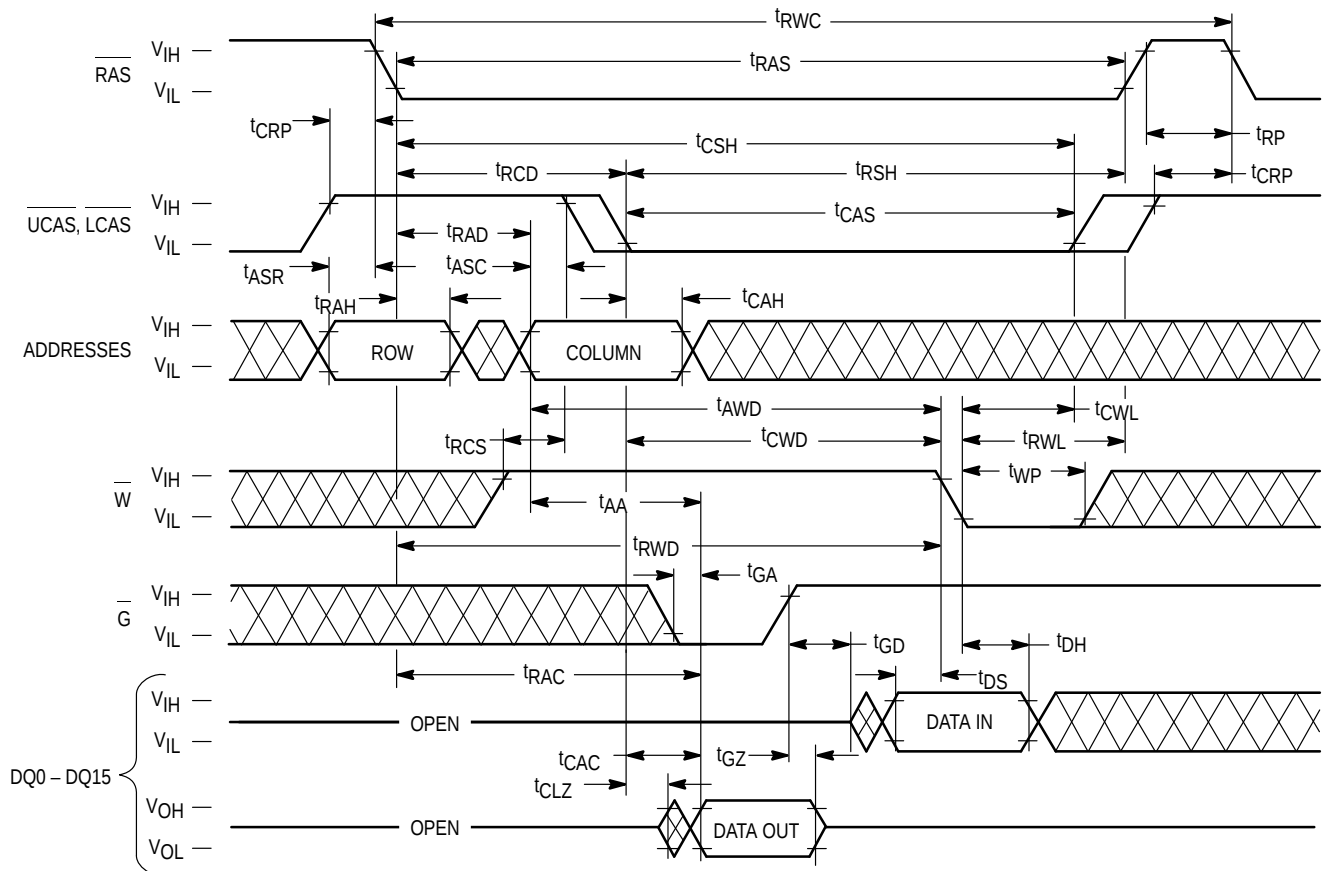
UPPER BYTE WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



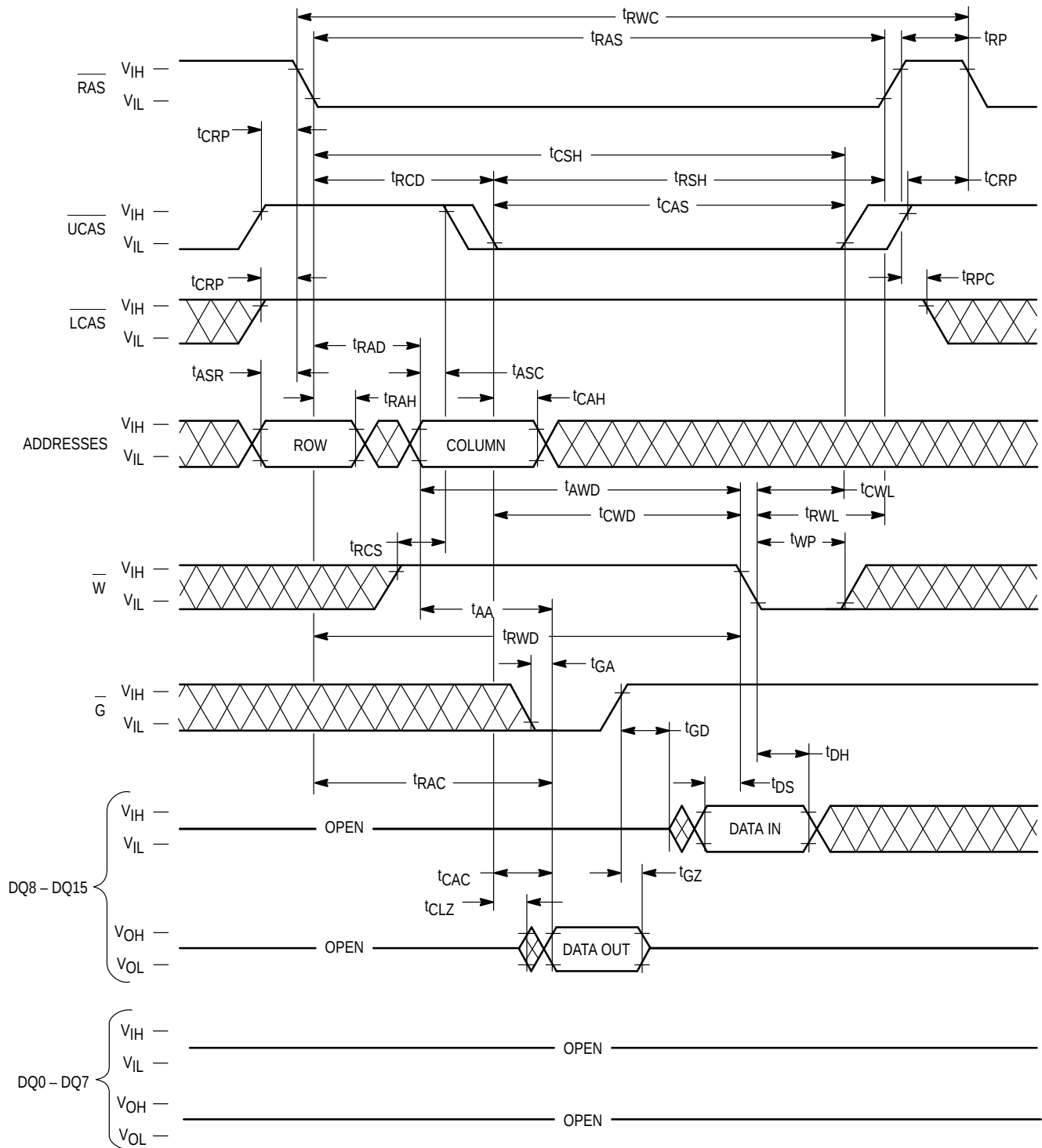
LOWER BYTE WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



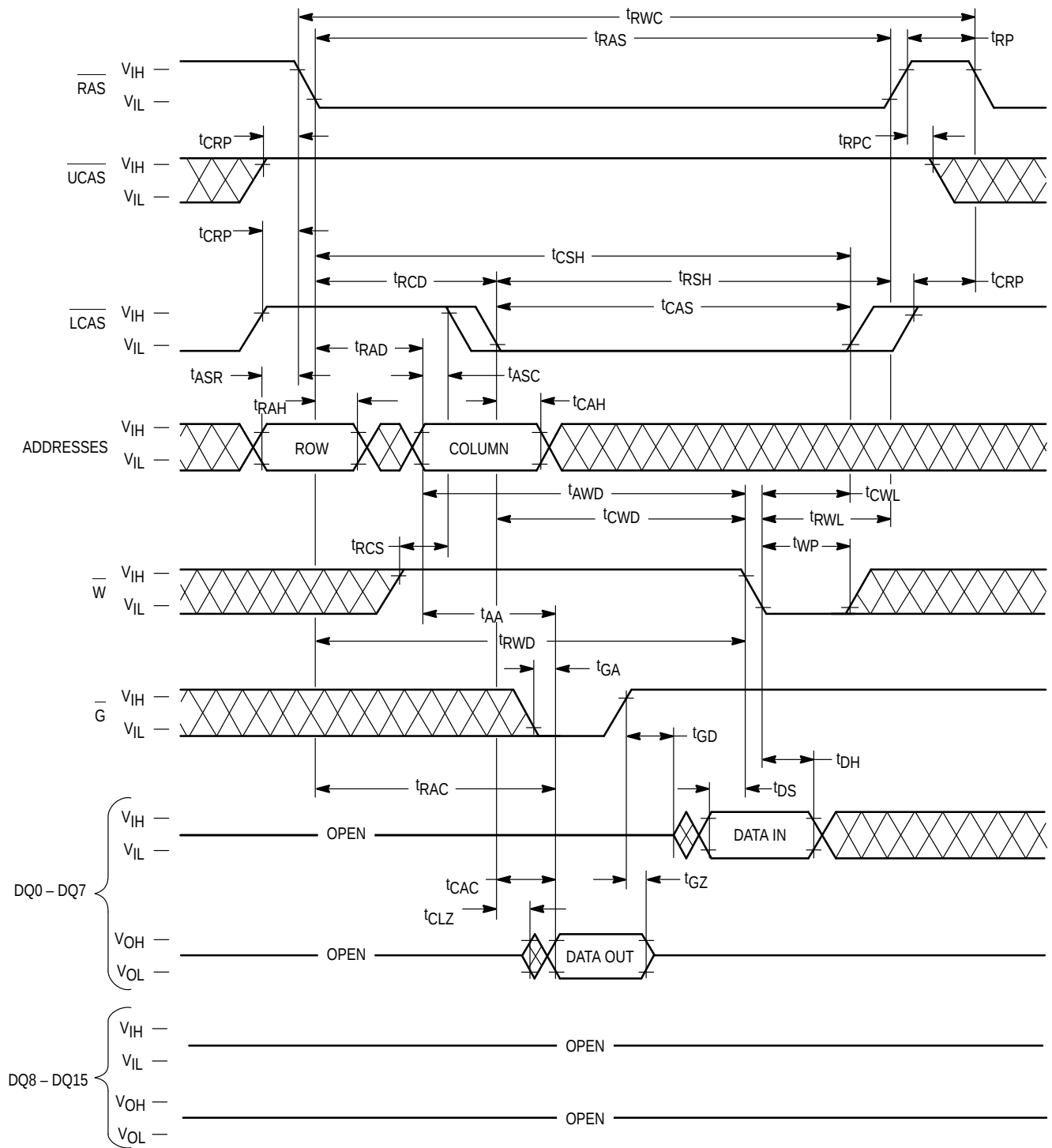
READ-WRITE CYCLE



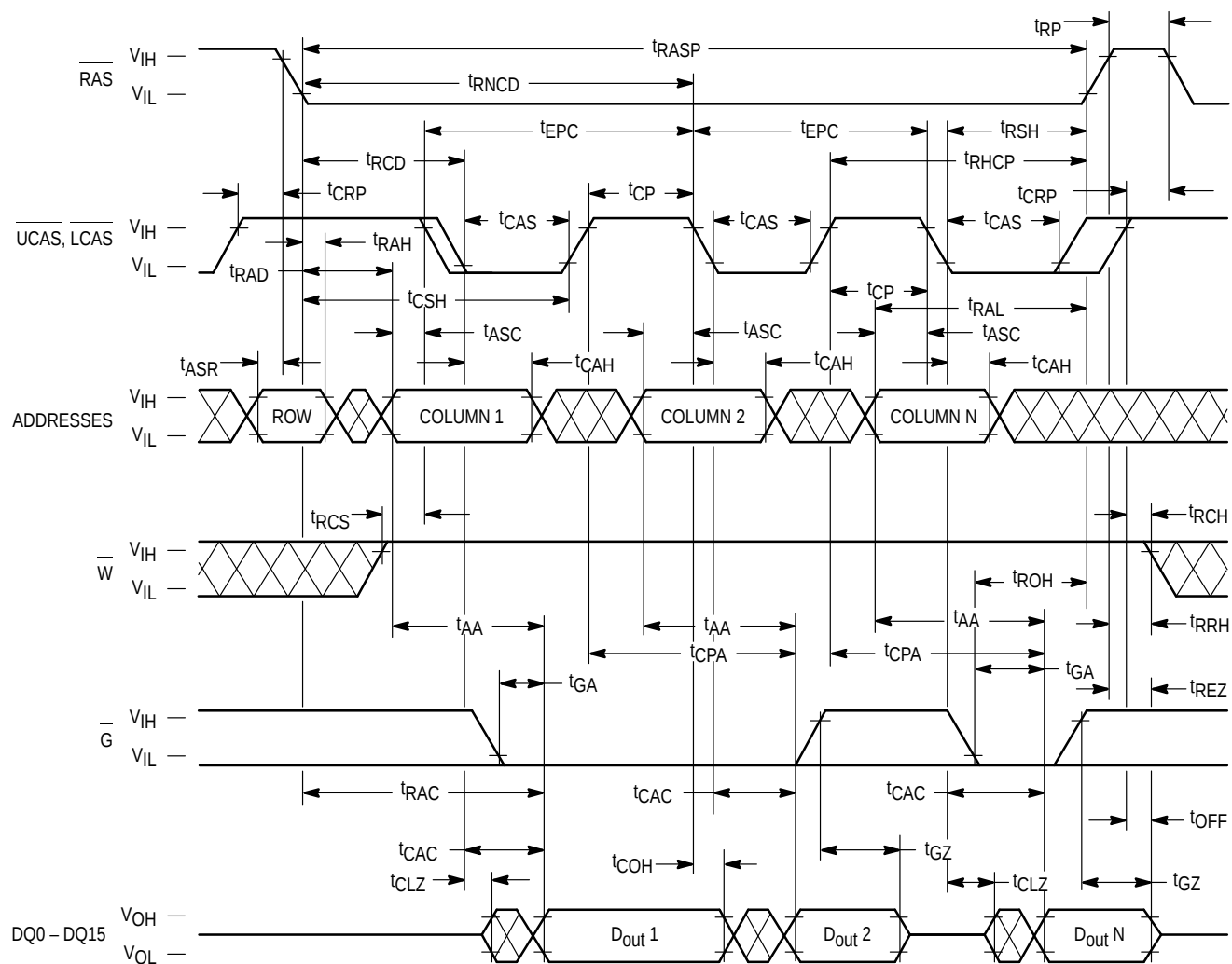
UPPER BYTE READ-WRITE CYCLE



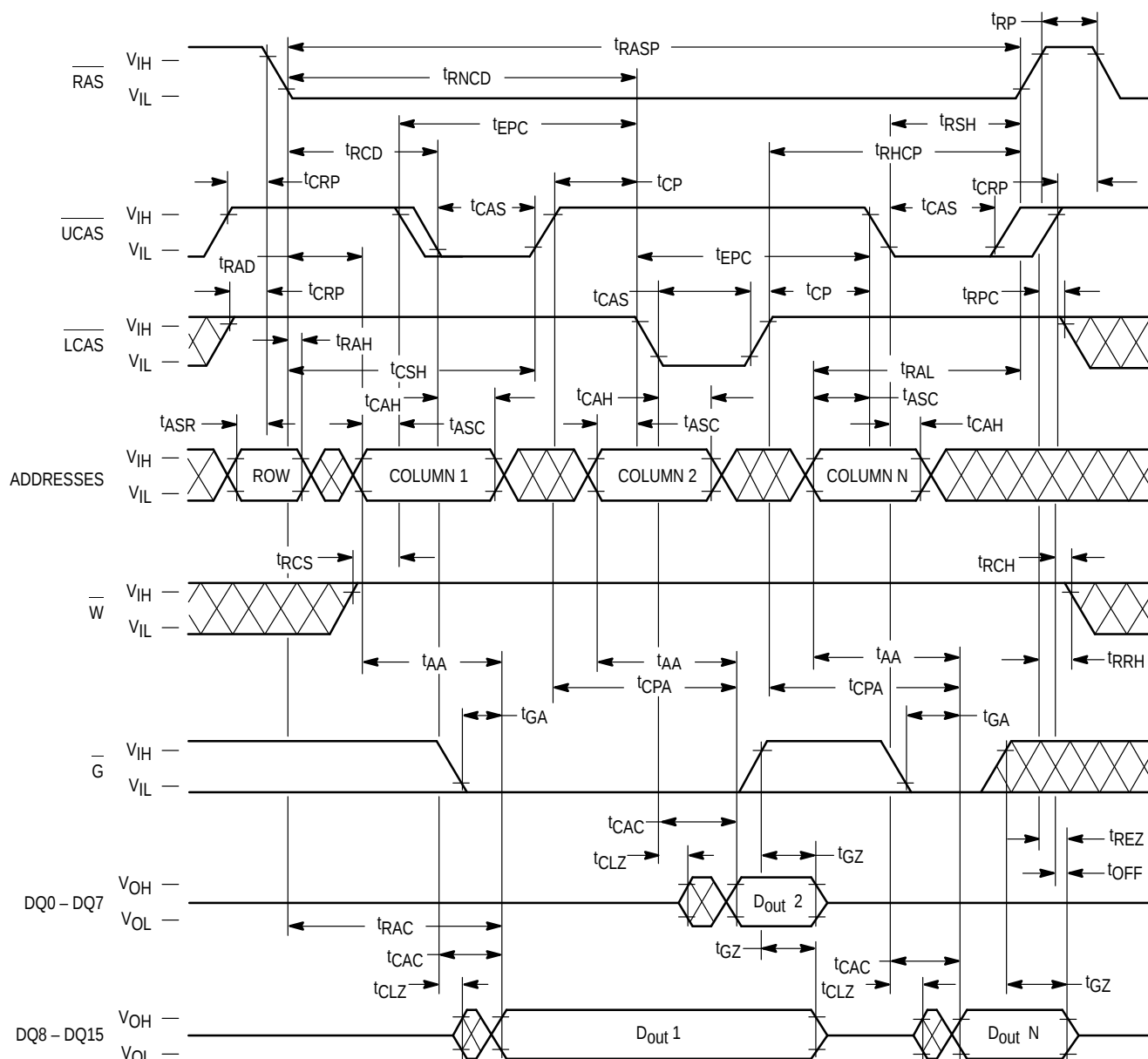
LOWER BYTE READ-WRITE CYCLE



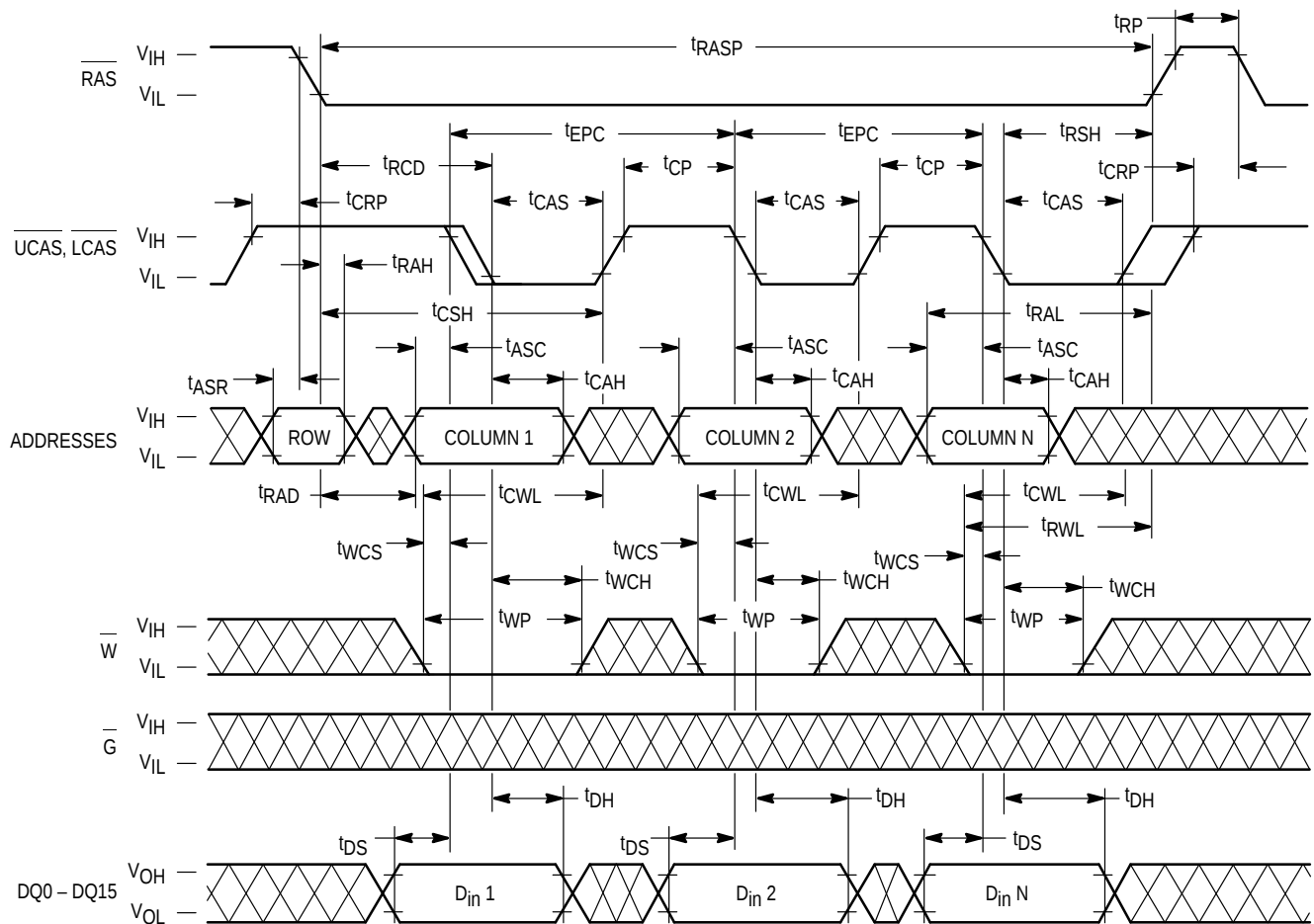
EXTENDED DATA OUT READ CYCLE



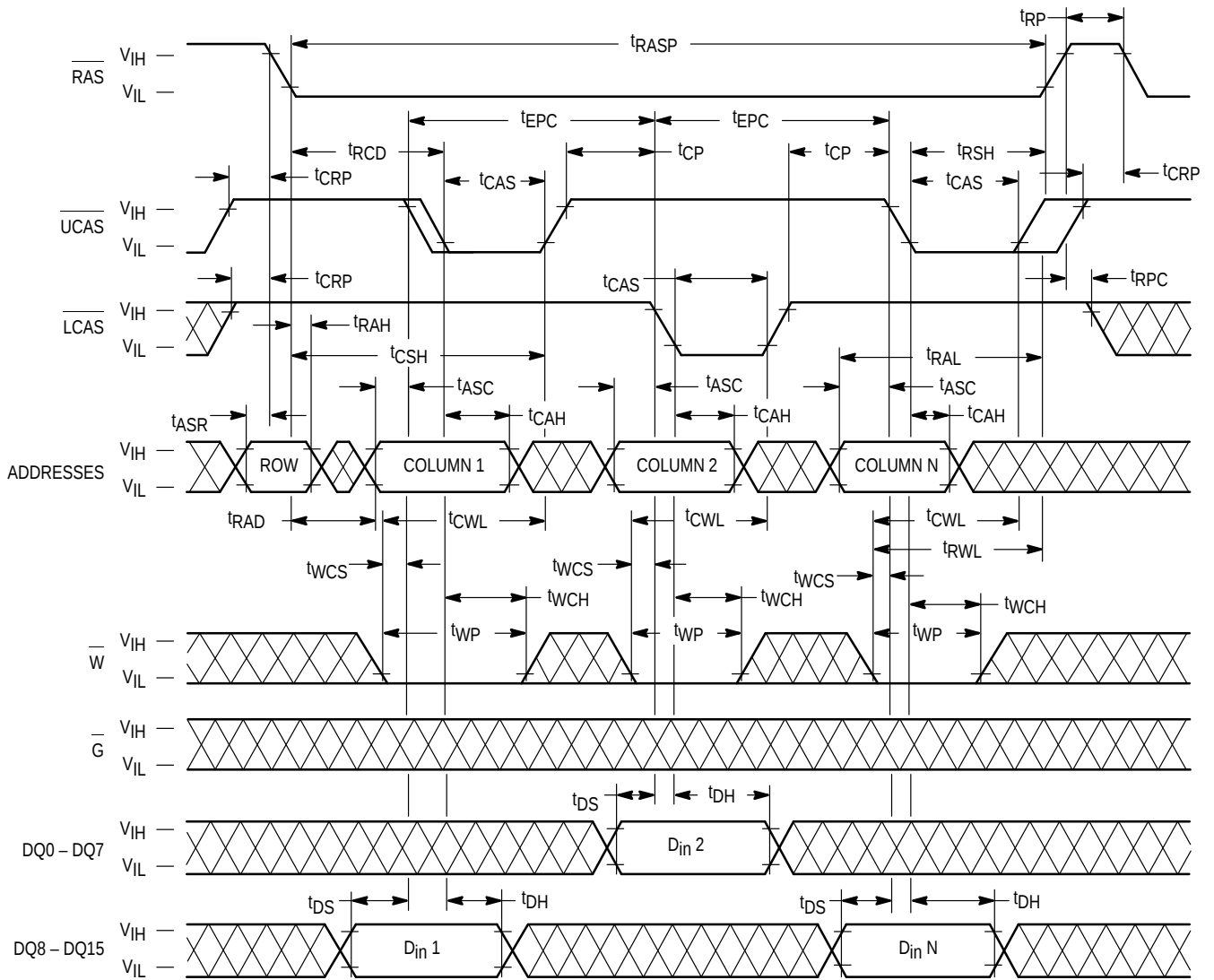
EXTENDED DATA OUT BYTE READ CYCLE



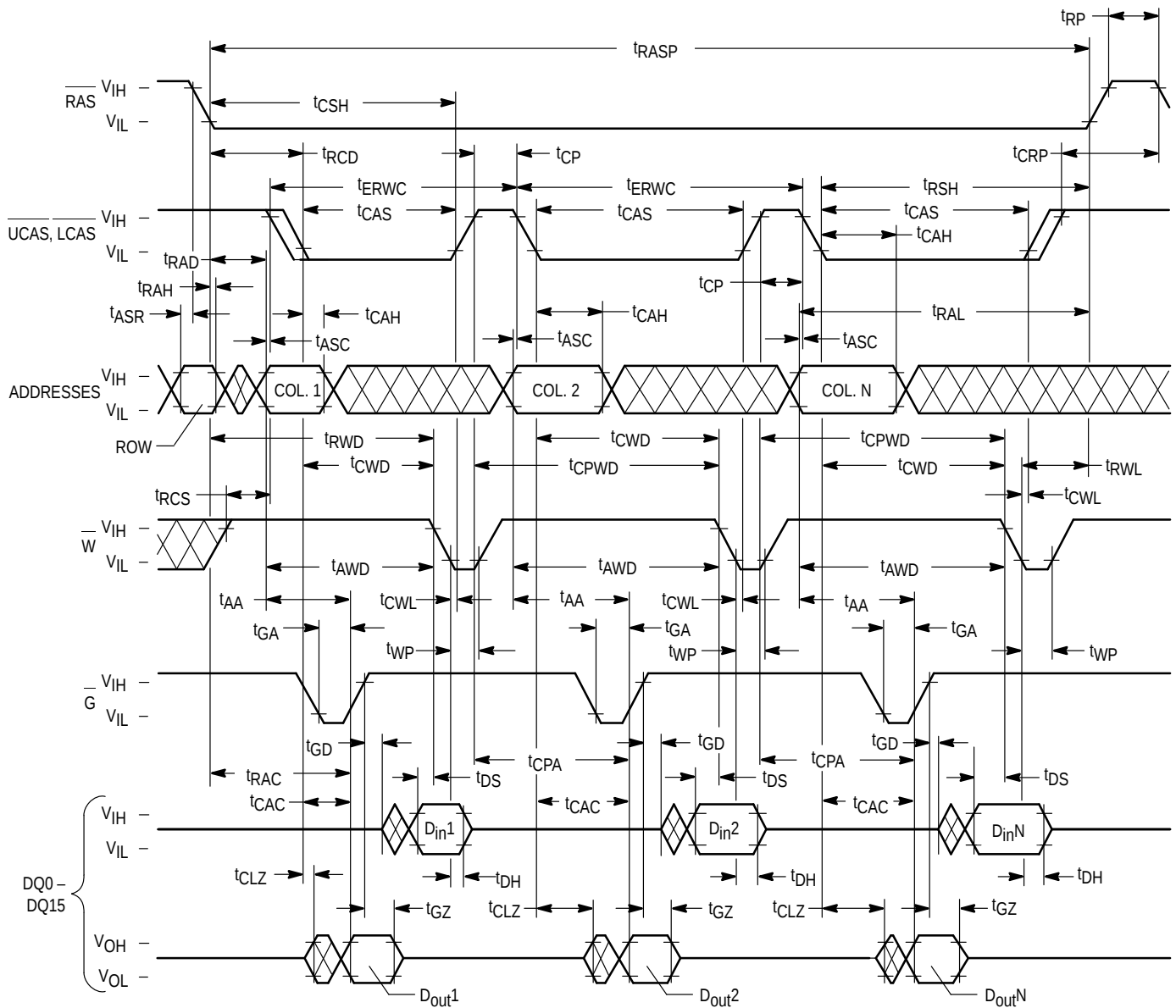
EXTENDED DATA OUT WRITE CYCLE (EARLY WRITE)



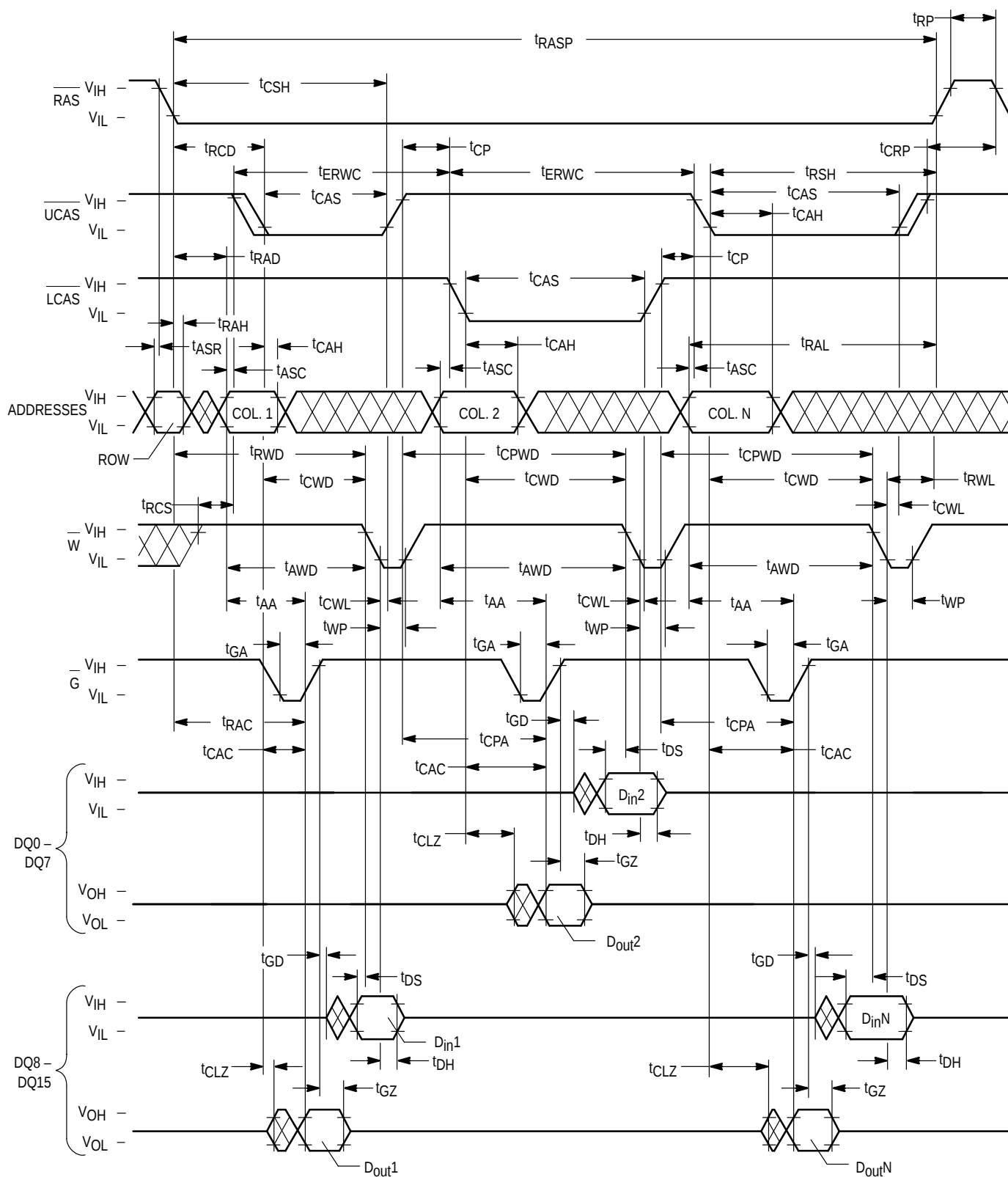
EXTENDED DATA OUT BYTE WRITE CYCLE (EARLY WRITE)



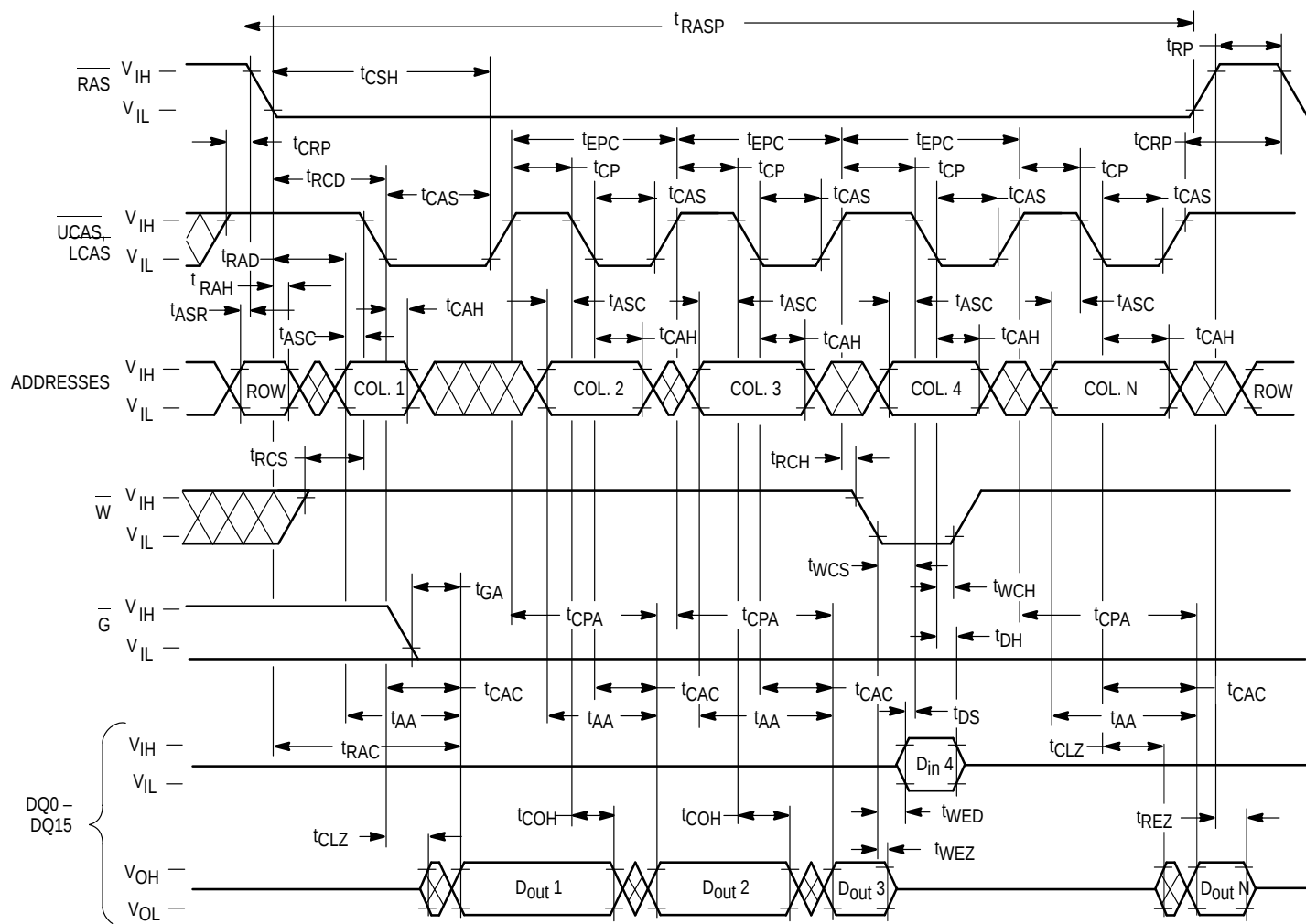
EXTENDED DATA OUT READ-WRITE CYCLE



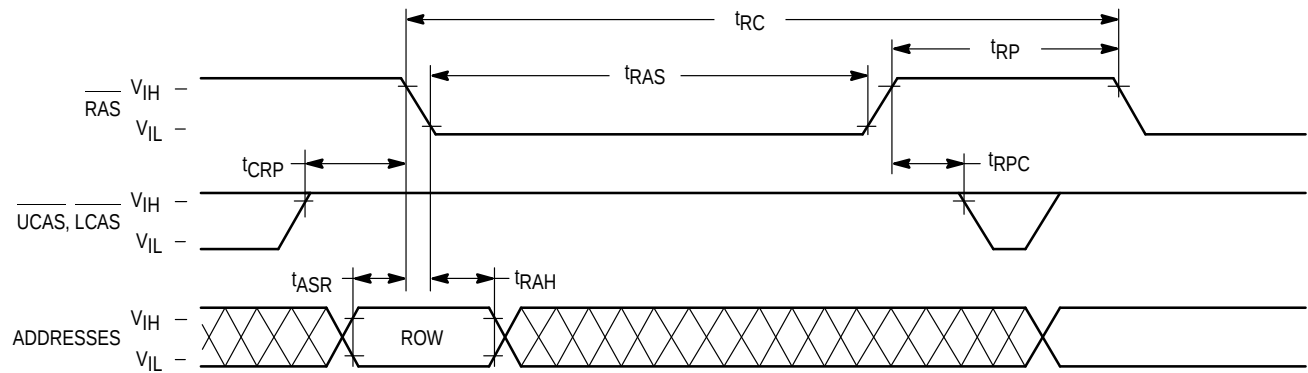
EXTENDED DATA OUT BYTE READ-WRITE CYCLE



EXTENDED DATA OUT READ WRITE MIXED CYCLE

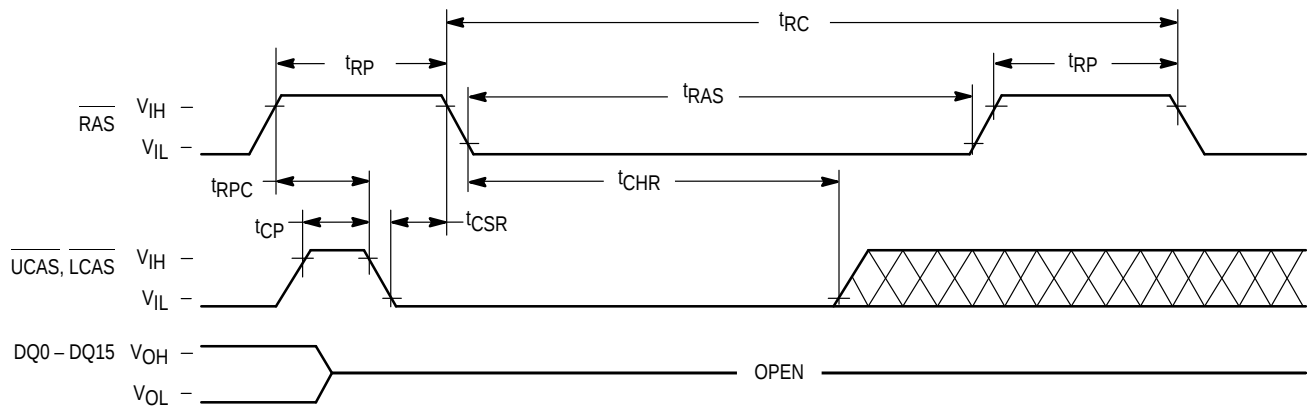


$\overline{\text{RAS}}$ -ONLY REFRESH CYCLE



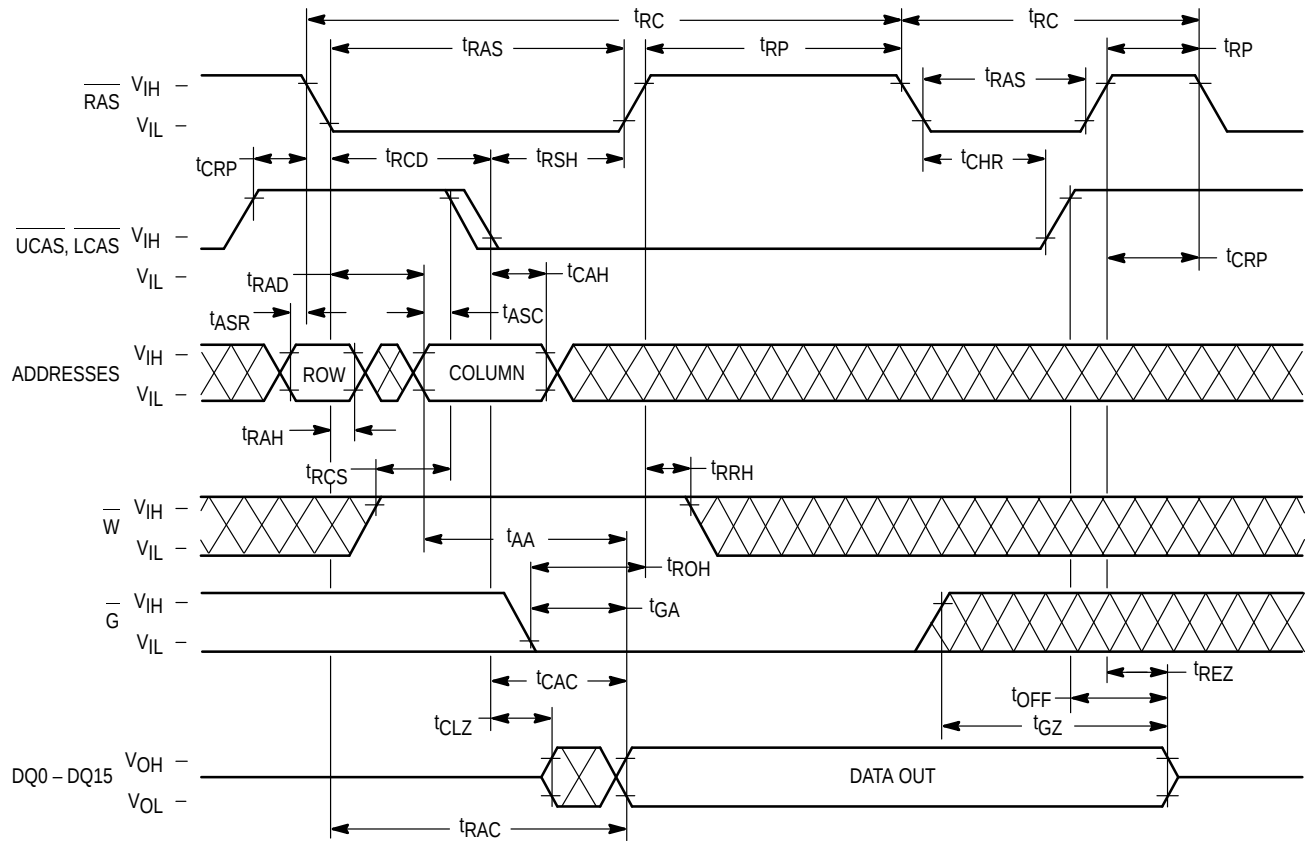
NOTE: $\overline{\text{W}}, \overline{\text{G}} = \text{H or L}$
 $\text{DQ0} - \text{DQ15} = \text{Open}$
 Addresses: MCM516165B — A0 to A11; MCM518165B — A0 to A9.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

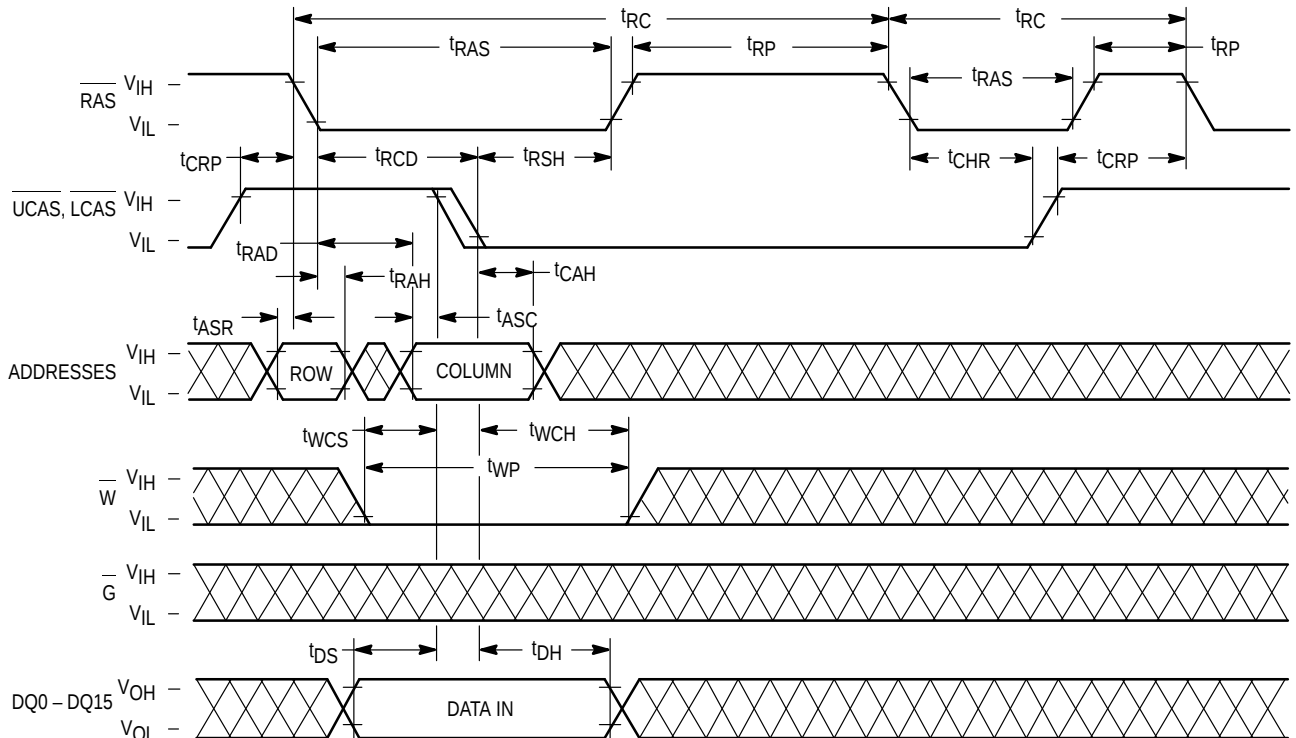


NOTE: $\overline{\text{W}}, \overline{\text{G}}, \text{Addresses} = \text{H or L}$
 $\overline{\text{CAS}}$ before RAS refresh is performed when either UCAS or LCAS meets this timing.

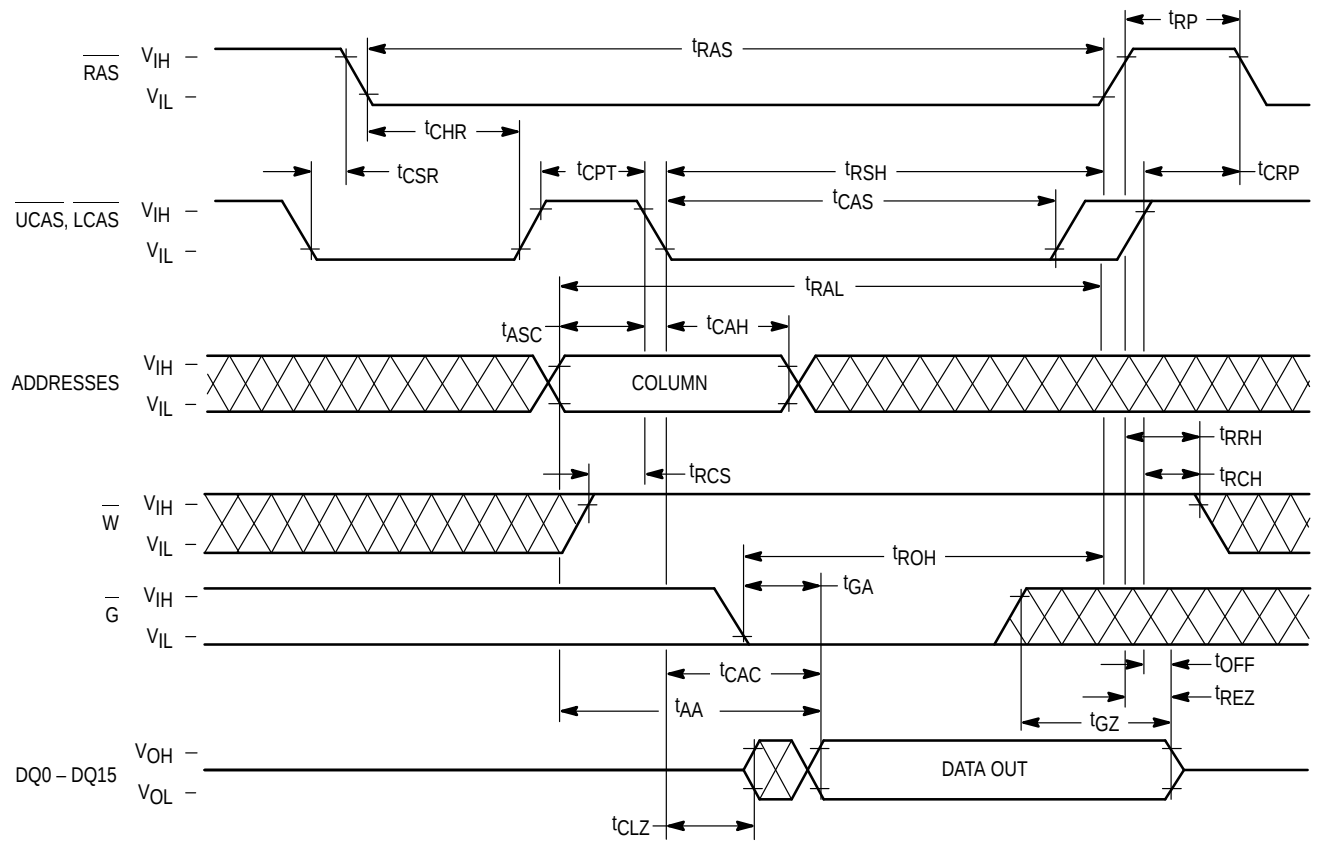
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

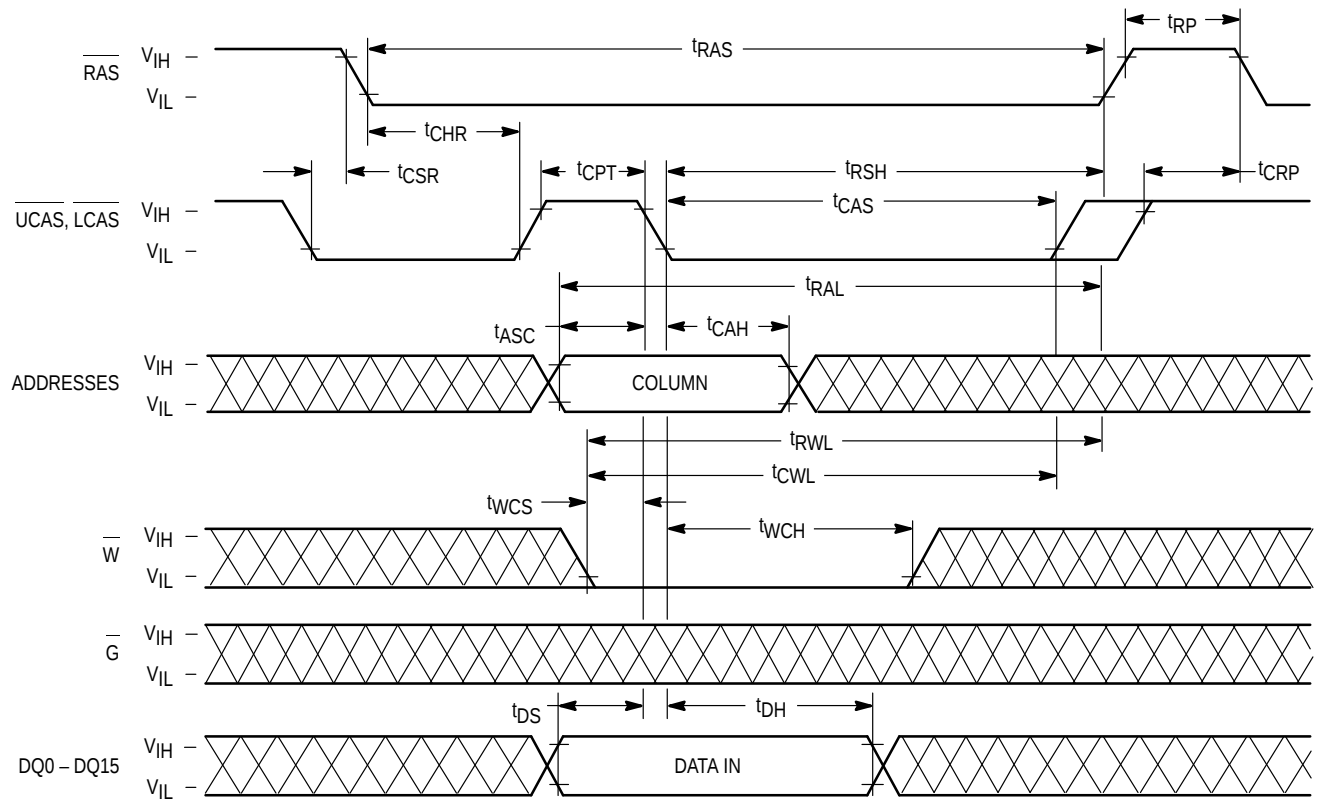


CAS BEFORE RAS REFRESH COUNTER TEST READ CYCLE



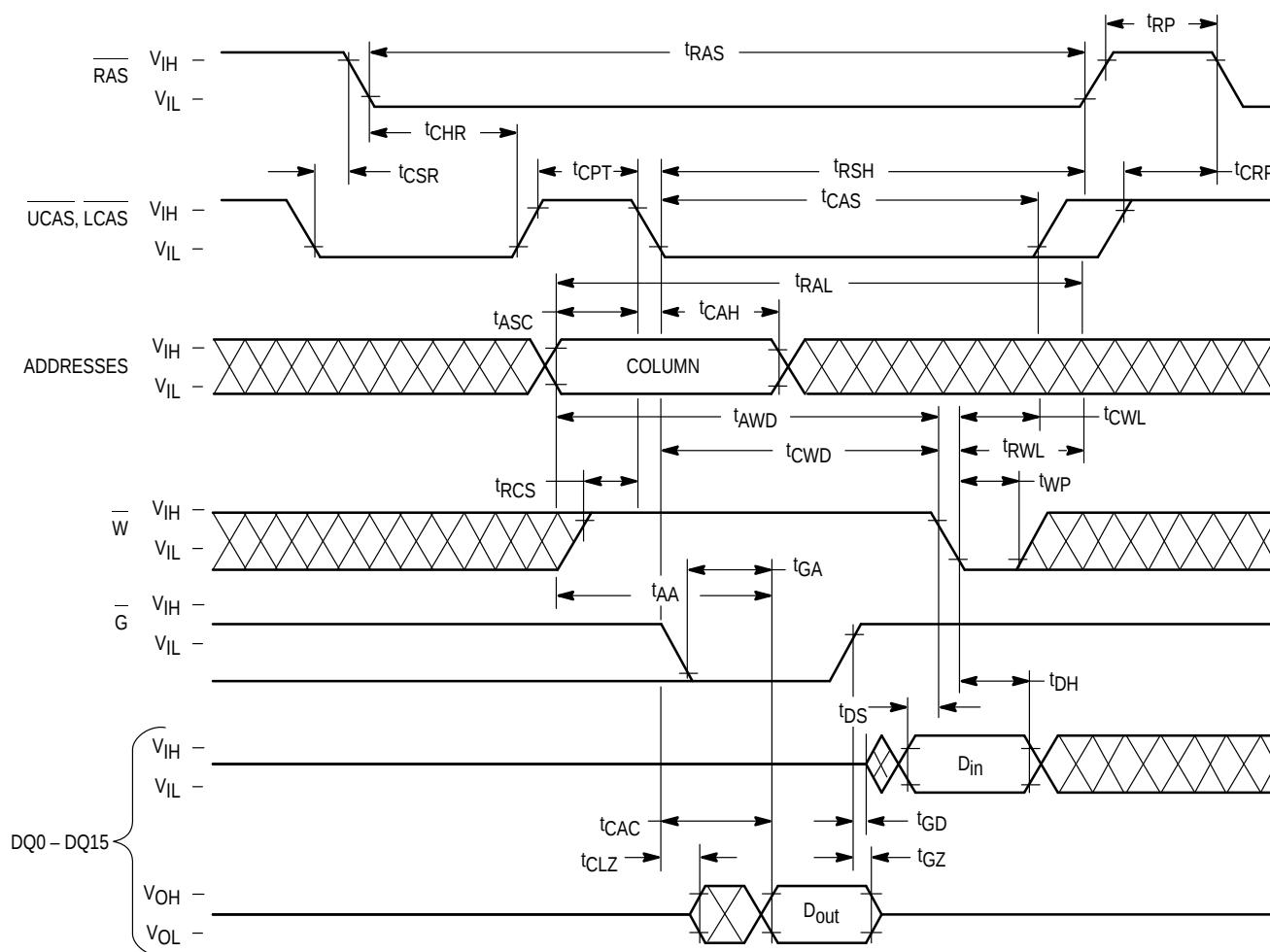
NOTE: Addresses: MCM516165B — A0 to A7; MCM518165B — A0 to A9

CAS BEFORE RAS REFRESH COUNTER TEST WRITE CYCLE



NOTE: Addresses: MCM516165B — A0 to A7; MCM518165B — A0 to A9

CAS BEFORE RAS REFRESH COUNTER TEST READ-WRITE CYCLE



NOTE: Addresses: MCM516165B — A0 to A7; MCM518165B — A0 to A9.

ORDERING INFORMATION (Order by Full Part Number)

Motorola Memory Prefix **MCM** **51x165B** **X** **XX** **X**

Part Number

Shipping Method (R = Tape and Reel, Blank = Rails for SOJ, Trays for TSOP II)

Speed (60 = 60 ns, 70 = 70 ns)

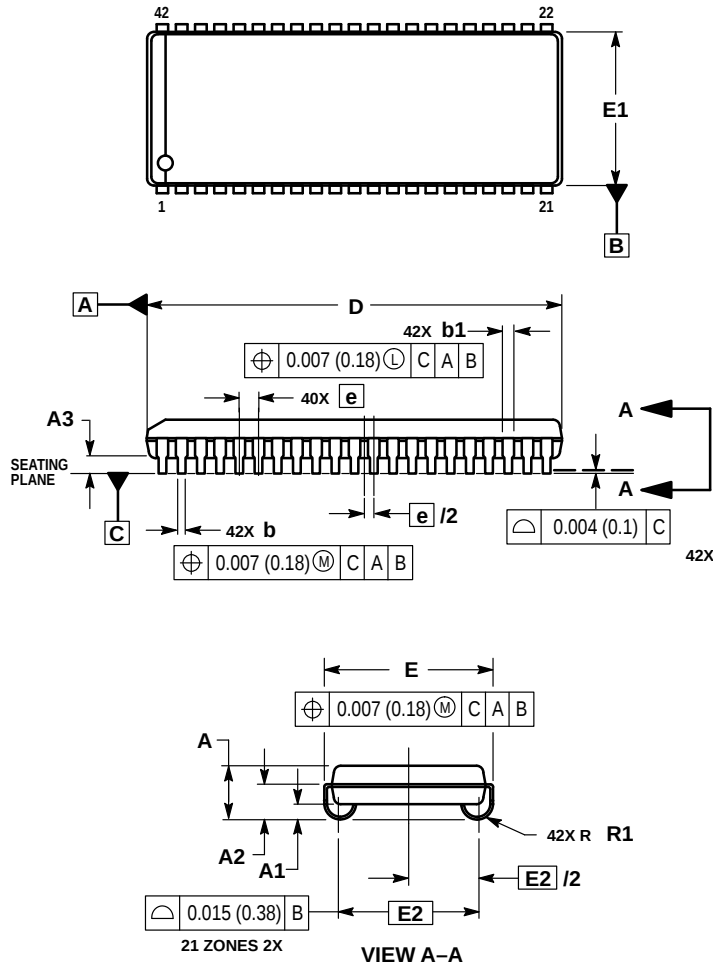
Package (J = 400 mil SOJ, T = 400 mil TSOP II)

Full Part Numbers — MCM516165BJ60 MCM516165BJ60R MCM516165BT60 MCM516165BT60R
MCM516165BJ70 MCM516165BJ70R MCM516165BT70 MCM516165BT70R

MCM518165BJ60 MCM518165BJ60R MCM518165BT60 MCM518165BT60R
MCM518165BJ70 MCM518165BJ70R MCM518165BT70 MCM518165BT70R

PACKAGE DIMENSIONS

J PACKAGE 400 MIL SOJ CASE 986A-01

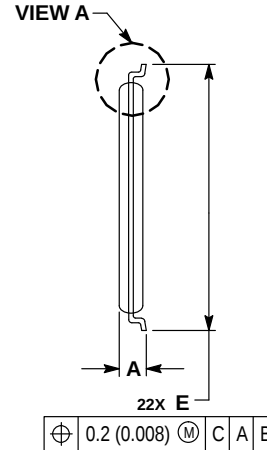
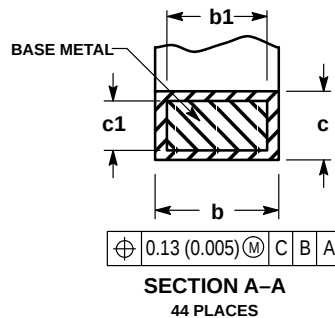
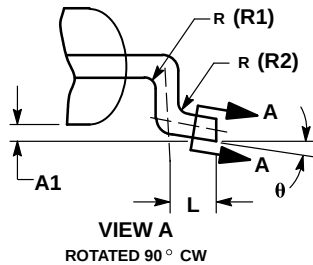
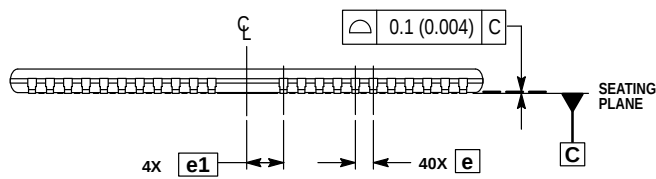
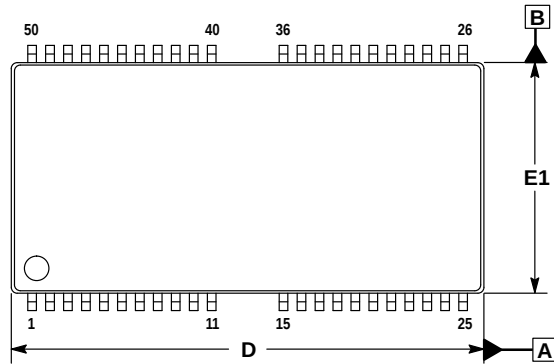


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006 (0.15) PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010 (0.25) PER SIDE.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 AND, HENCE, DATUMS A AND B, ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DIMENSIONS b1 DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE SHOULDER WIDTH TO EXCEED b1 MAX BY MORE THAN 0.005 (0.13). THE DAMBAR INTRUSION(S) SHALL NOT REDUCE THE SHOULDER WIDTH TO LESS THAN 0.001 (0.03) BELOW b2 MIN.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.130	0.146	3.30	3.70
A1	0.031	0.047	0.80	1.20
A2	0.092	—	2.35	—
A3	0.031	—	0.80	—
b	0.016	0.020	0.41	0.50
b1	0.026	0.032	0.66	0.81
D	1.070	1.080	27.19	27.43
E	0.430	0.440	10.92	11.18
E1	0.395	0.405	10.03	10.29
E2	0.366 BSC		9.30 BSC	
e	0.050 BSC		1.27 BSC	
R1	0.025	0.035	0.63	0.89

**T PACKAGE
400 MIL TSOP II
CASE 985A-01**



- NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MM.
 3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION IS 0.15 (0.006) MAXIMUM PER SIDE.
 4. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.58 (0.023).
 5. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 12, 13, 14, 37, 38 AND 39 ARE NOT USED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
b	0.25	0.45	0.010	0.018
b1	0.25	0.40	0.010	0.016
c	0.12	0.25	0.005	0.010
c1	0.10	0.20	0.004	0.008
D	20.85	21.06	0.821	0.829
e	0.80 BSC		0.0315 BSC	
e1	1.60 BSC		0.063 BSC	
E	11.56	11.96	0.455	0.471
E1	10.06	10.26	0.396	0.404
L	0.40	0.60	0.016	0.024
R1	0.10 REF		0.004 REF	
R2	0.10 REF		0.004 REF	
θ	0° 10°		0° 10°	

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