SIEMENS

C505A
C505CA

8-Bit CMOS Microcontroller

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1 Introduction

The C505A is an enhanced, upgraded version of the C505-2R eight bit microcontroller and incorporates more on-chip RAM, a 10-bit A/D Converter and 32K bytes of on-chip OTP memory. With a maximum external clock rate of 20 MHz, the C505A has an instruction cycle time of 300 ns.

With the C505A-4E fast OTP programming cycles are achieved (1 byte in 100 µsec). Also several levels of OTP memory protection can be selected. The basic functionality of the C505A-4E as a microcontroller is identical to the C505A-L (romless part) functionality. Therefore, the programmable C505A-4E typically can be used for prototype system design.

The C505A-4E basically operates with internal OTP and/or external program memory. The C505A-L is identical to the C505A-4E, except that it lacks the on-chip OTP memory. Therefore, in this documentation the term C505A refers to all versions within this specification unless otherwise noted.

The C505CA-4E and C505CA-L, are identical to the C505A-4E and the C505A-L respectively, except that they have, in addition, the full CAN interface. The term C505A refers to all the above four versions within this documentation unless otherwise noted.

Figure 1-1 shows the different functional units of the C505A and **Figure 1-2** shows the simplified logic symbol of the C505A.

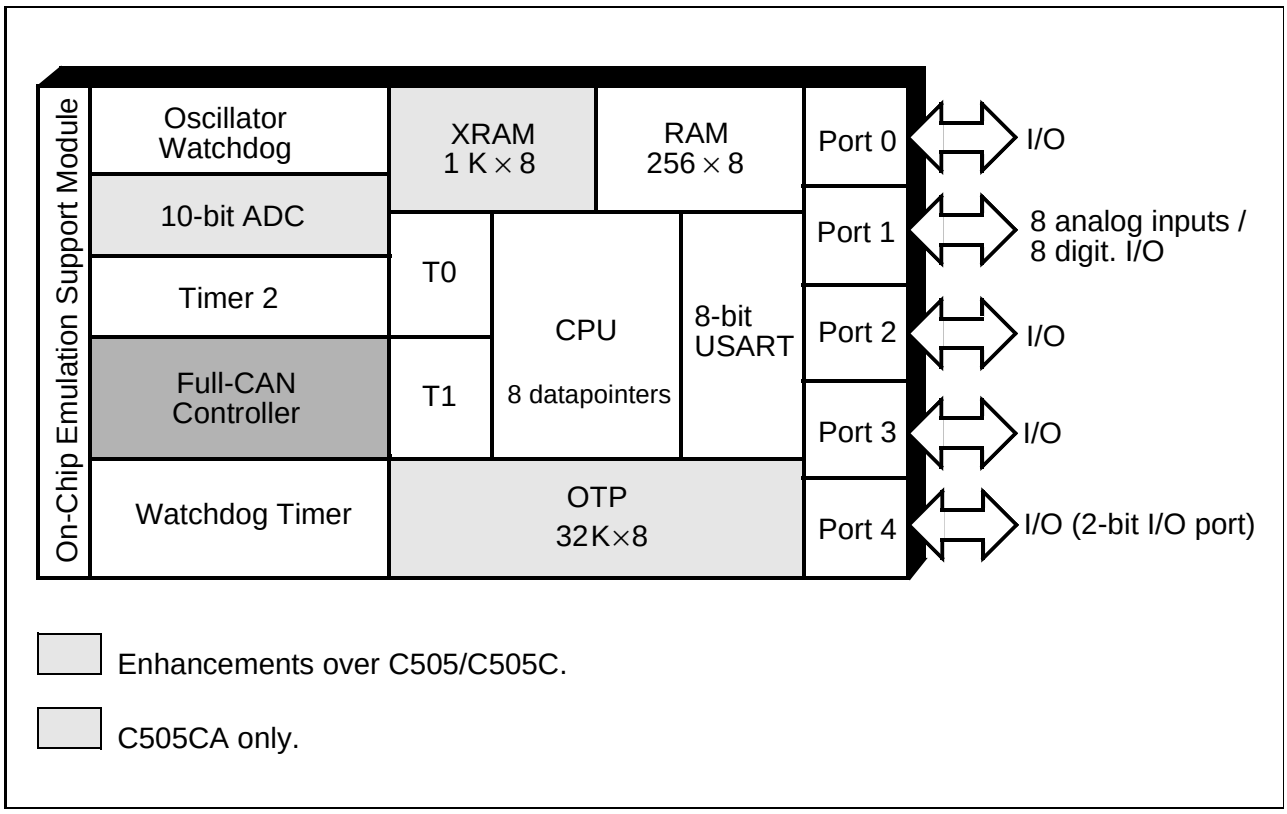


Figure 1-1
C505A Functional Units

Note: This specification describes only the improved functionality over C505/C505C. Please refer to the C505/C505C User's Manual for further details.

Listed below is a summary of the main features of the C505A family:

- Fully compatible to standard 8051 microcontroller
- Superset of the 8051 architecture with 8 datapointers
- Up to 20 MHz operating frequency
  - 375 ns instruction cycle time @ 16 MHz
  - 300 ns instruction cycle time @ 20 MHz (50 % duty cycle)
- 32K byte on-chip OTP memory
  - C505A-4E : programmable OTP versions
  - C505A-L : without on-chip program memory
  - alternatively up to 64 K bytes of external program memory
- 256 byte on-chip RAM
- 1 K byte on-chip XRAM
- Five ports: 32 + 2 digital I/O lines(Port 1 with mixed analog/digital I/O capability)
- Three 16-bit timers/counters
  - Timer 0 / 1 (C501 compatible)
  - Timer 2 with 4 channels for 16-bit capture/compare operation
- Full CAN Module (C505CA only)
  - 256 register/data bytes located in external data memory area
  - 1 MBaud CAN baudrate when operating frequency is equal to or above 8 MHz
  - internal CAN clock prescaler when input frequency is over 10 MHz
- Full duplex serial interface with programmable baudrate generator (USART)
- 10-bit A/D Converter with 8 multiplexed inputs
  - Built-in self calibration
- Twelve interrupt sources with four priority levels
- On-chip emulation support logic
  –Enhanced Hooks Technology ™ 1)
- Programmable 15-bit Watchdog Timer
- Oscillator Watchdog
- Fast Power On Reset
- Power Saving Modes
  - Slow-down mode
  - Idle mode (can be combined with slow-down mode)
  - Software power-down mode with wake up capability through P3.2/$\overline{\text{INT0}}$ or P4.1/RXDC pin
- P-MQFP-44 package
- Pin configuration is compatible to C501, C504, C511/C513-family, C505, C505C
- Temperature ranges:

SAB-C505A versions	T_A = 0 to 70 °C	
SAF-C505A versions	T_A = – 40 to 85°C	
SAH-C505A versions	T_A = – 40 to 110°C	(max. operating frequency: TBD)
SAK-C505A versions	T_A = –40 to 125°C	(max. operating frequency: 12 MHz with 50 % duty cycle)

1 “Enhanced Hooks Technology“ is a trademark and patent of Metalink Corporation licensed to Siemens.

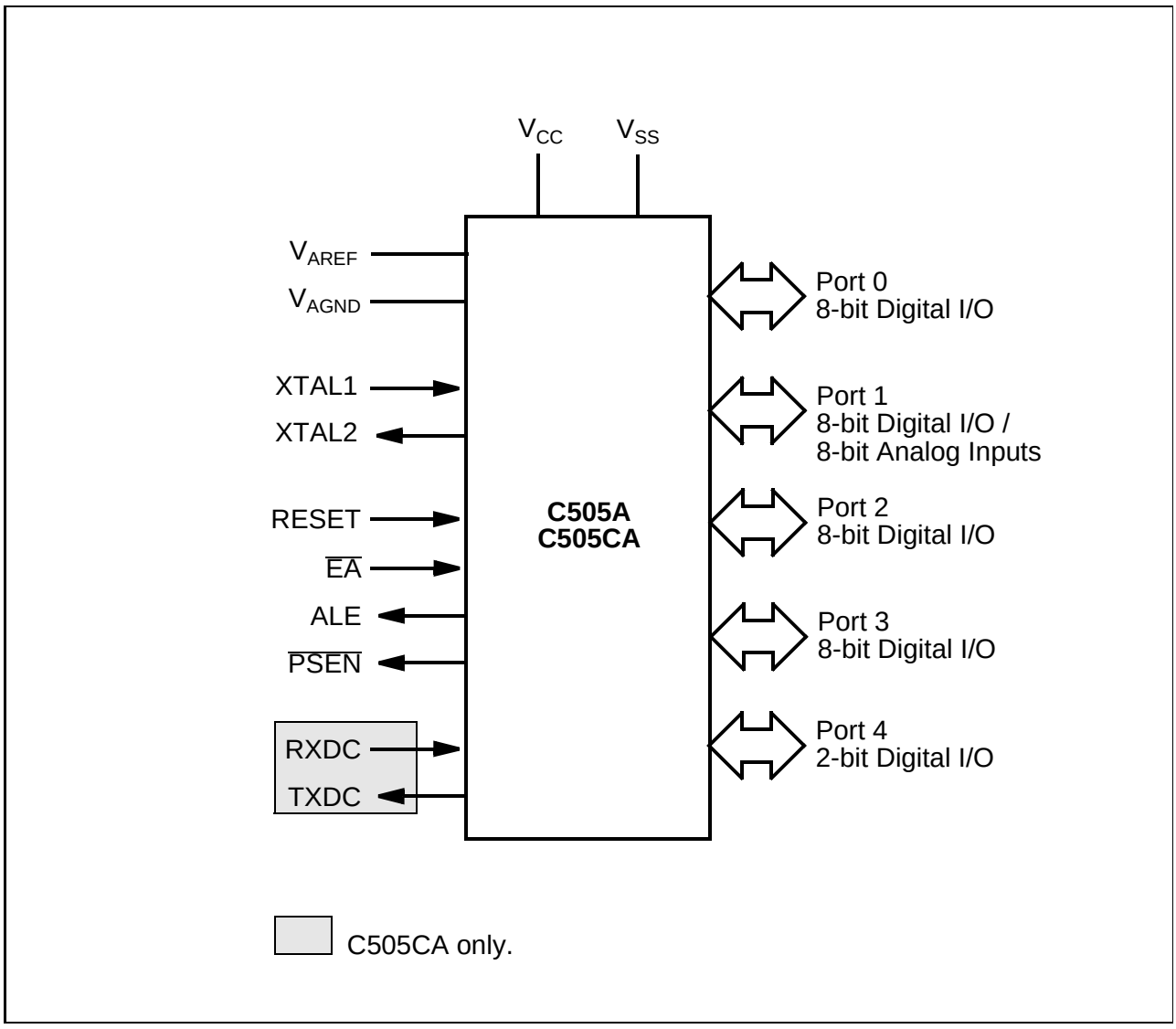


Figure 1-2
Logic Symbol

1.1 Pin Configuration

This section shows the pin configuration of the C505A in the P-MQFP-44 package.

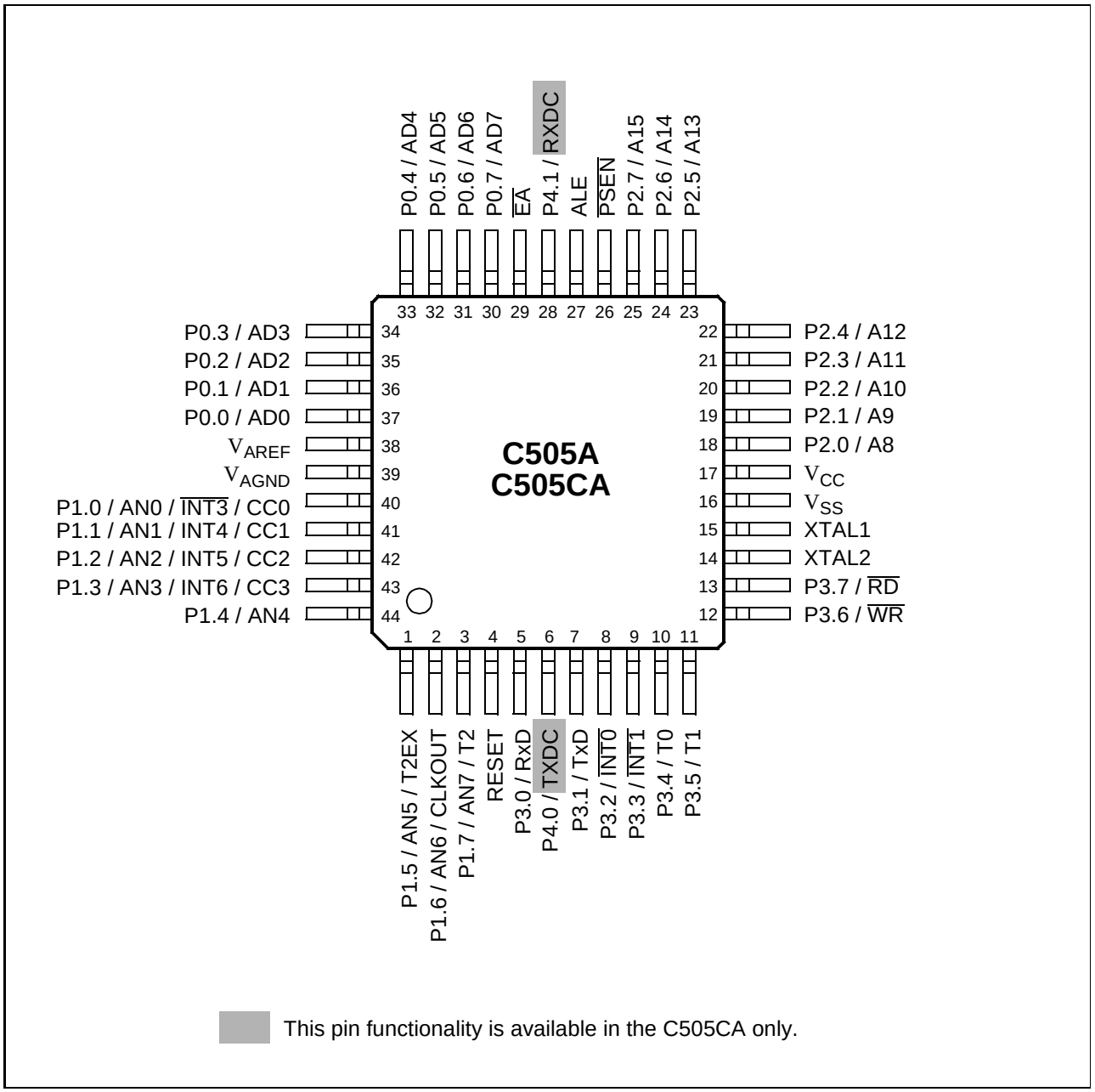


Figure 1-3
Pin Configuration (Top View)

1.2 Pin Definitions and Functions

This section describes all external signals of the C505A with its function.

Table 1-1 :
Pin Definitions and Functions

Symbol	Pin Number	I/O *)	Function
P1.0-P1.7	40-44,1-3	I/O	**Port 1** is an 8-bit quasi-bidirectional port with internal pull-up arrangement. Port 1 pins can be used for digital input/output or as analog inputs of the A/D converter. Port 1 pins that have 1's written to them are pulled high by internal pull-up transistors and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. Port 1 pins are assigned to be used as analog inputs via the register P1ANA. As secondary digital functions, port 1 contains the interrupt, timer, clock, capture and compare pins. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except for compare functions). The secondary functions are assigned to the pins of port 1 as follows:
	40		P1.0 / AN0 / $\overline{\text{INT3}}$ / CC0 — Analog input channel 0 interrupt 3 input / capture/compare channel 0 I/O
	41		P1.1 / AN1 / INT4 / CC1 — Analog input channel 1/ interrupt 4 input / capture/compare channel 1 I/O
	42		P1.2 / AN2 / INT5 / CC2 — Analog input channel 2 / interrupt 5 input / capture/compare channel 2 I/O
	43		P1.3 / AN3 / INT6 / CC3 — Analog input channel 3 interrupt 6 input / capture/compare channel 4 I/O
	44		P1.4 / AN4 — Analog input channel 4
	1		P1.5 / AN5 / T2EX — Analog input channel 5 / Timer 2 external reload / trigger input
	2		P1.6 / AN6 / CLKOUT — Analog input channel 6 / system clock output
	3		P1.7 / AN7 / T2 — Analog input channel 7 / counter 2 input

*) I = Input
O = Output

Table 1-1 :
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
RESET	4	I	**RESET** A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.
P3.0-P3.7	5, 7-13	I/O	**Port 3** is an 8-bit quasi-bidirectional port with internal pull-up arrangement. Port 3 pins that have 1's written to them are pulled high by the internal pull-up transistors and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except for TxD and $\overline{WR}$). The secondary functions are assigned to the pins of port 3 as follows:
	5	P3.0 / RxD	Receiver data input (asynch.) or data input/output (synch.) of serial interface
	7	P3.1 / TxD	Transmitter data output (asynch.) or clock output (synch.) of serial interface
	8	P3.2 / $\overline{INT0}$	External interrupt 0 input / timer 0 gate control input
	9	P3.3 / $\overline{INT1}$	External interrupt 1 input / timer 1 gate control input
	10	P3.4 / T0	Timer 0 counter input
	11	P3.5 / T1	Timer 1 counter input
	12	P3.6 / $\overline{WR}$	$\overline{WR}$ control output; latches the data byte from port 0 into the external data memory
	13	P3.7 / $\overline{RD}$	$\overline{RD}$ control output; enables the external data memory

*) I = Input
O = Output

Table 1-1 :
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
P4.0 P4.1	6 28	I/O I/O	**Port 4** is a 2-bit quasi-bidirectional port with internal pull-up arrangement. Port 4 pins that have 1's written to them are pulled high by the internal pull-up transistors and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. The output latch corresponding to the secondary function RXDC must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the two pins of port 4 as follows (C505CA only) : P4.0 / TXDC Transmitter output of CAN controller P4.1 / RXDC Receiver input of CAN controller
XTAL2	14	O	**XTAL2** Output of the inverting oscillator amplifier.
XTAL1	15	I	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. To operate above a frequency of 16 MHz, a duty cycle of the etxernal clock signal of 50 % should be maintained. Minimum and maximum high and low times as well as rise/ fall times specified in the AC characteristics must be observed.

*) I = Input
O = Output

Table 1-1 :
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
P2.0-P2.7	18-25	I/O	**Port 2** is a an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup transistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register and uses only the internal pullup resistors.
$\overline{\text{PSEN}}$	26	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every three oscillator periods except during external data memory accesses. Remains high during internal program execution. This pin should not be driven during reset operation.
ALE	27	O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every three oscillator periods except during an external data memory access. When instructions are executed from internal OTP ($\overline{\text{EA}}$=1) the ALE generation can be disabled by bit EALE in SFR SYSCON. ALE should not be driven during reset operation.

*) I = Input
O = Output

Table 1-1 :
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
$\overline{EA}$	29	I	**External Access Enable** When held at high level, instructions are fetched from the internal OTP memory when the PC is less than 8000H. When held at low level, the C505A/C505CA fetches all instructions from external program memory. $\overline{EA}$ should not be driven during reset operation. For the C505A-L and the C505CA-L this pin must be tied low.
P0.0-P0.7	37-30	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impendance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pullup transistors when issuing 1's.
V_{AREF}	38	–	**Reference voltage** for the A/D converter.
V_{AGND}	39	–	**Reference ground** for the A/D converter.
V_{SS}	16	–	**Ground** (0V)
V_{CC}	17	–	**Power Supply** (+5V)

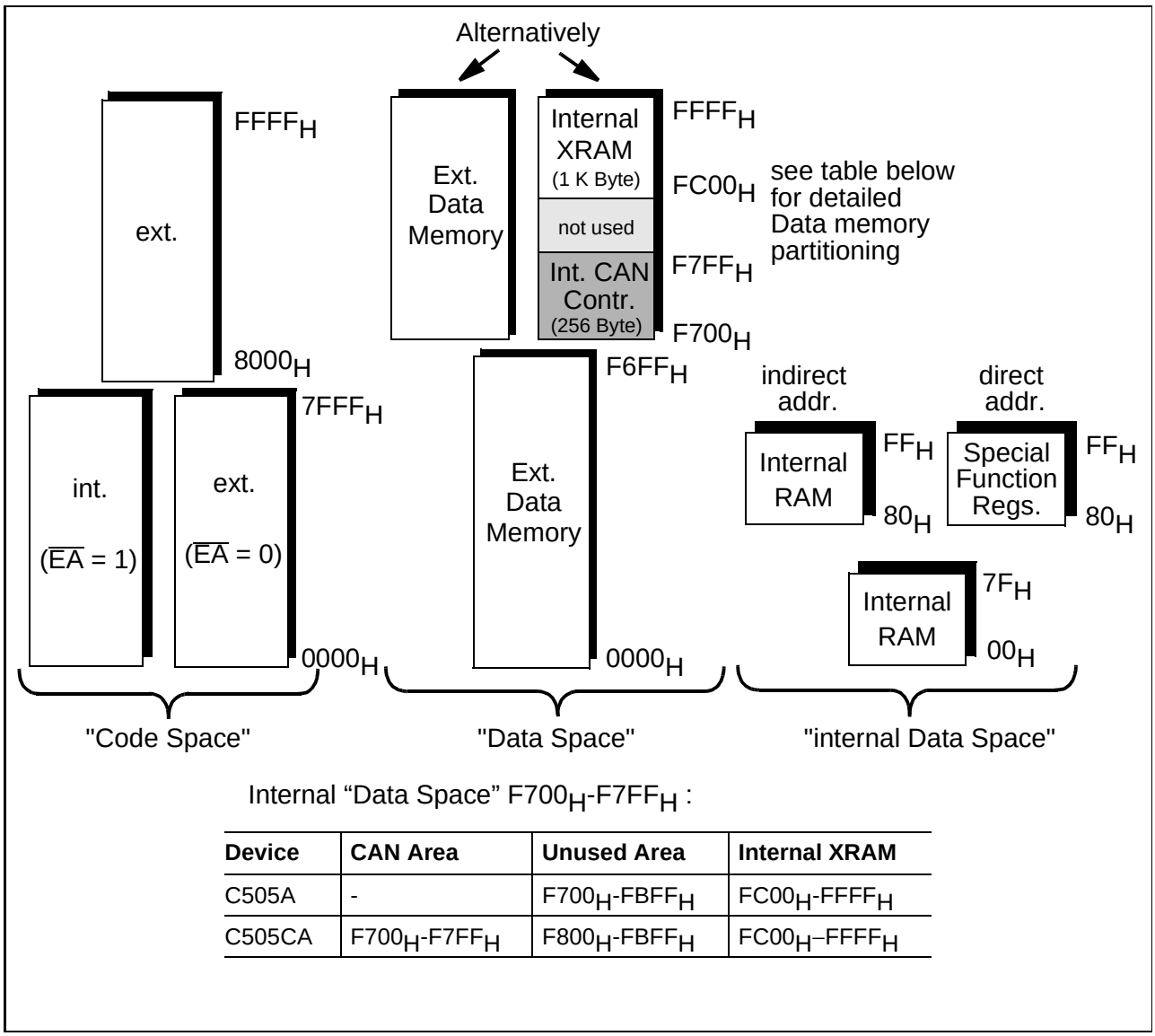
*) I = Input
O = Output

2 Memory Organization

The C505A CPU manipulates operands in the following four address spaces:

- up to 64 Kbytes of program memory (32K on-chip OTP memory for C505A-4E)
- up to 64 Kbytes of external data memory
- 256 bytes of internal data memory
- 1 Kbytes of internal XRAM data memory
- 256 bytes CAN controller registers / data memory (C505CA only)
- a 128 byte special function register area

Figure 2-1 illustrates the memory address spaces of the C505A.



Internal “Data Space” F700$_H$-F7FF$_H$:

Device	CAN Area	Unused Area	Internal XRAM
C505A	-	F700$_H$-FBFF$_H$	FC00$_H$-FFFF$_H$
C505CA	F700$_H$-F7FF$_H$	F800$_H$-FBFF$_H$	FC00$_H$–FFFF$_H$

Figure 2-1
C505A Memory Map

2.1 Program Memory, "Code Space"

The C505A-4E has 32 Kbytes of on-chip OTP program memory which can be externally expanded up to 64 Kbytes. If the $\overline{EA}$ pin is held high, the C505A-4E executes program code out of the OTP memory unless the program counter address exceeds $7FFF_H$. Address locations 8000_H through $FFFF_H$ are then fetched from the external program memory. If the $\overline{EA}$ pin is held low, the C505A fetches all instructions from the external program memory.

2.2 Data Memory, "Data Space"

The data memory address space consists of an internal and an external memory space. The internal data memory is divided into three physically separate and distinct blocks : the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128 byte special function register (SFR) area. While the upper 128 bytes of data memory and the SFR area share the same address locations, they are accessed through different addressing modes. The lower 128 bytes of data memory can be accessed through direct or register indirect addressing; the upper 128 bytes of RAM can be accessed through register indirect addressing; the special function registers are accessible through direct addressing. Four 8-register banks, each bank consisting of eight 8-bit general-purpose registers, occupy locations 0 through $1F_H$ in the lower RAM area. The next 16 bytes, locations 20_H through $2F_H$, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal RAM area, and the stack depth can be expanded up to 256 bytes.

The external data memory can be expanded up to 64 Kbyte and can be accessed by instructions that use a 16-bit or an 8-bit address. The internal CAN controller (in C505CA only) and the internal 1 Kbyte XRAM are located in the external memory address area at addresses $F700_H$ to $F7FF_H$ and $FC00_H$ to $FFFF_H$ respectively. The CAN controller registers and internal XRAM can therefore be accessed using MOVX instructions with addresses pointing to the respective address areas.

2.3 General Purpose Registers

The lower 32 locations of the internal RAM are assigned to four banks of eight general purpose registers (GPRs) each. Only one of these banks may be enabled at a time. Two bits in the program status word, RS0 (PSW.3) and RS1 (PSW.4), select the active register bank (see description of the PSW in chapter 2). This allows fast context switching, which is useful when entering subroutines or interrupt service routines.

The 8 general purpose registers of the selected register bank may be accessed by register addressing. With register addressing the instruction op code indicates which register is to be used. For indirect addressing R0 and R1 are used as pointer or index register to address internal or external memory (e.g. MOV @R0).

Reset initializes the stack pointer to location 07_H and increments it once to start from location 08_H which is also the first register (R0) of register bank 1. Thus, if one is going to use more than one register bank, the SP should be initialized to a different location of the RAM which is not used for data storage.

2.4 Special Function Registers

The registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function register area consists of two portions : the standard special function register area and the mapped special function register area. One special function register of the C505A (PCON1) is located in the mapped special function register area. For accessing the mapped special function register area, bit RMAP in special function register SYSCON must be set. All other special function registers are located in the standard special function register area which is accessed when RMAP is cleared (“0“).

In the C505CA, the registers and data locations of the CAN controller (CAN-SFRs) are located in the external data memory area at addresses $F700_H$ to $F7FF_H$. This is compatible to the C505C and details about the access of these registers is described in the C505C User’s Manual.

Special Function Register SYSCON (Address $B1_H$) **Reset Value : $XX100X01_B$**
(C505CA only) Reset Value : $XX100001_B$

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$B1_H$	–	–	EALE	RMAP	CMOD	CSWO 1)	XMAP1	XMAP0	SYSCON

The functions of the shaded bits are not described here.

1) This bit is available in the C505CA only.

Bit	Function
CSWO	CAN Controller switch-off bit CPWD = 0 : CAN Controller is enabled (default after reset). CPWD = 1 : CAN Controller is switched off. This function is an enhancement over the C505C-2R.
–	Reserved bits for future use. Read by CPU returns undefined values.

As long as bit RMAP is set, mapped special function register area can be accessed. This bit is not cleared by hardware automatically. Thus, when non-mapped/mapped registers are to be accessed, the bit RMAP must be cleared/set respectively by software.

All SFRs with addresses where address bits 0-2 are 0 (e.g. 80_H, 88_H, 90_H, 98_H, ..., $F8_H$, FF_H) are bitaddressable.

The 52 special function registers (SFRs) in the standard and mapped SFR area include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. The SFRs of the C505A are listed in **table 2-1** and **table 2-2**. In **table 2-1** they are organized in groups which refer to the functional blocks of the C505A. The CAN-SFRs (applicable to the C505CA only) are also included in **table 2-1**. **Table 2-2** illustrates the contents of the SFRs in numeric order of their addresses. **Table 2-3** list the CAN-SFRs in numeric order of their addresses.

Table 2-1
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$** [1]	00_H
	B	B-Register	**$F0_H$** [1]	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	DPSEL	Data Pointer Select Register	92_H	$XXXXX000_B$ [3]
	PSW	Program Status Word Register	**$D0_H$** [1]	00_H
	SP	Stack Pointer	81_H	07_H
	SYSCON[2]	System Control Register	$B1_H$	$XX100X01_B$ [3] [6] $XX100101_B$ [3] [7]
	VR0 [4]	Version Register 0	FC_H	$C5_H$
	VR1 [4]	Version Register 1	FD_H	05_H
	VR2 [4]	Version Register 2	FE_H	[5]
A/D-Converter	ADCON0 [2]	A/D Converter Control Register 0	**$D8_H$** [1]	$00X00000_B$ [3]
	ADCON1	A/D Converter Control Register 1	DC_H	$01XXX000_B$ [3]
	ADDATH	A/D Converter High Byte Data Register	$D9_H$	00_H
	ADDATL	A/D Converter Low Byte Data Register	DA_H	$00XXXXXX_B$ [3]
	P1ANA [2] [4]	Port 1 Analog Input Selection Register	90_H	FF_H
Interrupt System	IEN0 [2]	Interrupt Enable Register 0	**$A8_H$** [1]	00_H
	IEN1 [2]	Interrupt Enable Register 1	**$B8_H$** [1]	00_H
	IP0 [2]	Interrupt Priority Register 0	$A9_H$	00_H
	IP1	Interrupt Priority Register 1	$B9_H$	$XX000000_B$ [3]
	TCON [2]	Timer Control Register	**88_H** [1]	00_H
	T2CON [2]	Timer 2 Control Register	**$C8_H$** [1]	$00X00000_B$
	SCON [2]	Serial Channel Control Register	**98_H** [1]	00_H
	IRCON	Interrupt Request Control Register	**$C0_H$** [1]	00_H
XRAM	XPAGE	Page Address Register for Extended on-chip XRAM and CAN Controller	91_H	00_H
	SYSCON[2]	System Control Register	$B1_H$	$XX100X01_B$ [3] [6] $XX100101_B$ [3] [7]
Ports	P0	Port 0	**80_H** [1]	FF_H
	P1	Port 1	**90_H** [1]	FF_H
	P1ANA [2] [4]	Port 1 Analog Input Selection Register	**90_H** [1]	FF_H
	P2	Port 2	**$A0_H$** [1]	FF_H
	P3	Port 3	**$B0_H$** [1]	FF_H
	P4	Port 4	**E8H** [1]	$XXXXXX11_B$

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) “X“ means that the value is undefined and the location is reserved
4) This SFR is a mapped SFR. For accessing this SFR, bit RMAP in SFR SYSCON must be set.
5) The content of this SFR varies with the actual step of the C505A (eg. 11_H for the first step)
6) C505A only
7) C505CA only

Table 2-1
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Serial Channel	ADCON0 2)	A/D Converter Control Register 0	**$D8_H$** 1)	$00X00000_B$ 3)
	PCON 2)	Power Control Register	87_H	00_H
	SBUF	Serial Channel Buffer Register	99_H	XX_H 3)
	SCON	Serial Channel Control Register	**98_H** 1)	00_H
	SRELL	Serial Channel Reload Register, low byte	AA_H	$D9_H$
	SRELH	Serial Channel Reload Register, high byte	BA_H	$XXXXXX11_B$ 3)
Timer 0/ Timer 1	TCON	Timer 0/1 Control Register	**88_H** 1)	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Compare/ Capture Unit / Timer 2	CCEN	Comp./Capture Enable Reg.	$C1_H$	00_H 3)
	CCH1	Comp./Capture Reg. 1, High Byte	$C3_H$	00_H
	CCH2	Comp./Capture Reg. 2, High Byte	$C5_H$	00_H
	CCH3	Comp./Capture Reg. 3, High Byte	$C7_H$	00_H
	CCL1	Comp./Capture Reg. 1, Low Byte	$C2_H$	00_H
	CCL2	Comp./Capture Reg. 2, Low Byte	$C4_H$	00_H
	CCL3	Comp./Capture Reg. 3, Low Byte	$C6_H$	00_H
	CRCH	Reload Register High Byte	CB_H	00_H
	CRCL	Reload Register Low Byte	CA_H	00_H
	TH2	Timer 2, High Byte	CD_H	00_H
	TL2	Timer 2, Low Byte	CC_H	00_H
	T2CON	Timer 2 Control Register	**$C8_H$** 1)	$00X00000_B$ 3)
	IEN0 2)	Interrupt Enable Register 0	**$A8_H$** 1)	00_H
	IEN1 2)	Interrupt Enable Register 1	**$B8_H$** 1)	00_H
Watchdog	WDTREL	Watchdog Timer Reload Register	86_H	00_H
	IEN0 2)	Interrupt Enable Register 0	**$A8_H$** 1)	00_H
	IEN1 2)	Interrupt Enable Register 1	**$B8_H$** 1)	00_H
	IP0 2)	Interrupt Priority Register 0	$A9_H$	00_H
Power Save Modes	PCON 2)	Power Control Register	87_H	00_H
	PCON1 4)	Power Control Register 1	**88_H** 1)	$0XX0XXXX_B$ 3)

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) "X" means that the value is undefined and the location is reserved
4) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 2-1
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
CAN Controller (C505CA only)	CR	Control Register	$F700_H$	01_H
	SR	Status Register	$F701_H$	XX_H 3)
	IR	Interrupt Register	$F702_H$	XX_H 3)
	BTR0	Bit Timing Register Low	$F704_H$	UU_H 3)
	BTR1	Bit Timing Register High	$F705_H$	$0UUUUUUU_B$ 3)
	GMS0	Global Mask Short Register Low	$F706_H$	UU_H 3)
	GMS1	Global Mask Short Register High	$F707_H$	$UUU11111_B$ 3)
	UGML0	Upper Global Mask Long Register Low	$F708_H$	UU_H 3)
	UGML1	Upper Global Mask Long Register High	$F709_H$	UU_H 3)
	LGML0	Lower Global Mask Long Register Low	$F70A_H$	UU_H 3)
	LGML1	Lower Global Mask Long Register High	$F70B_H$	$UUUUU000_B$ 3)
	UMLM0	Upper Mask of Last Message Register Low	$F70C_H$	UU_H 3)
	UMLM1	Upper Mask of Last Message Register High	$F70D_H$	UU_H 3)
	LMLM0	Lower Mask of Last Message Register Low	$F70E_H$	UU_H 3)
	LMLM1	Lower Mask of Last Message Register High	$F70F_H$	$UUUUU000_B$ 3)
		Message Object Registers :		
	MCR0	Message Control Register Low	$F7n0_H$ 5)	UU_H 3)
	MCR1	Message Control Register High	$F7n1_H$ 5)	UU_H 3)
	UAR0	Upper Arbitration Register Low	$F7n2_H$ 5)	UU_H 3)
	UAR1	Upper Arbitration Register High	$F7n3_H$ 5)	UU_H 3)
	LAR0	Lower Arbitration Register Low	$F7n4_H$ 5)	UU_H 3)
	LAR1	Lower Arbitration Register High	$F7n5_H$ 5)	$UUUUU000_B$ 3)
	MCFG	Message Configuration Register	$F7n6_H$ 5)	$UUUUUU00_B$ 3)
	DB0	Message Data Byte 0	$F7n7_H$ 5)	XX_H 3)
	DB1	Message Data Byte 1	$F7n8_H$ 5)	XX_H 3)
	DB2	Message Data Byte 2	$F7n9_H$ 5)	XX_H 3)
	DB3	Message Data Byte 3	$F7nA_H$ 5)	XX_H 3)
	DB4	Message Data Byte 4	$F7nB_H$ 5)	XX_H 3)
	DB5	Message Data Byte 5	$F7nC_H$ 5)	XX_H 3)
	DB6	Message Data Byte 6	$F7nD_H$ 5)	XX_H 3)
	DB7	Message Data Byte 7	$F7nE_H$ 5)	XX_H 3)

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) "X" means that the value is undefined and the location is reserved. "U" means that the value is unchanged by a reset operation. "U" values are undefined (as "X") after a power-on reset operation
4) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.
5) The notation "n" (n= 1 to F) in the message object address definition defines the number of the related message object.

Table 2-2
Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80_H [2)]	P0	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
81_H	SP	07_H	.7	.6	.5	.4	.3	.2	.1	.0
82_H	DPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
83_H	DPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
86_H	WDTREL	00_H	WDT PSEL	.6	.5	.4	.3	.2	.1	.0
87_H	PCON	00_H	SMOD	PDS	IDLS	SD	GF1	GF0	PDE	IDLE
88_H [2)]	TCON	00_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
88_H [3)]	PCON1	$0XX0\text{-}XXXX_B$	EWPD	–	–	WS	–	–	–	–
89_H	TMOD	00_H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
$8A_H$	TL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8B_H$	TL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8C_H$	TH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8D_H$	TH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
90_H [2)]	P1	FF_H	T2	CLK-OUT	T2EX	.4	.3	INT5	INT4	.0
90_H [3)]	P1ANA	FF_H	EAN7	EAN6	EAN5	EAN4	EAN3	EAN2	EAN1	EAN0
91_H	XPAGE	00_H	.7	.6	.5	.4	.3	.2	.1	.0
92_H	DPSEL	$XXXX\text{-}X000_B$	–	–	–	–	–	.2	.1	.0
98_H [2)]	SCON	00_H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99_H	SBUF	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$A0_H$ [2)]	P2	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$A8_H$ [2)]	IEN0	00_H	EA	WDT	ET2	ES	ET1	EX1	ET0	EX0
$A9_H$	IP0	00_H	OWDS	WDTS	.5	.4	.3	.2	.1	.0
AA_H	SRELL	$D9_H$	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) Bit-addressable special function registers
3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 2-2
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$B0_H$[2)]	P3	FF_H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TxD	RxD
$B1_H$	SYSCON [3)]	XX10-0X01$_B$	–	–	EALE	RMAP	CMOD	–	XMAP1	XMAP0
$B1_H$	SYSCON [4)]	XX10-0001$_B$	–	–	EALE	RMAP	CMOD	CSWO	XMAP1	XMAP0
$B8_H$[2)]	IEN1 [3)]	0000-00X0$_B$	EXEN2	SWDT	EX6	EX5	EX4	EX3	–	EADC
$B8_H$[2)]	IEN1 [4)]	00_H	EXEN2	SWDT	EX6	EX5	EX4	EX3	ECAN	EADC
$B9_H$	IP1	XX00-0000$_B$	–	–	.5	.4	.3	.2	.1	.0
BA_H	SRELH	XXXX-XX11$_B$	–	–	–	–	–	–	.1	.0
$C0_H$ [2)]	IRCON	00_H	EXF2	TF2	IEX6	IEX5	IEX4	IEX3	SWI	IADC
$C1_H$	CCEN	00_H	COCAH3	COCAL3	COCAH2	COCAL2	COCAH1	COCAL1	COCAH0	COCAL0
$C2_H$	CCL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C3_H$	CCH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C4_H$	CCL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C5_H$	CCH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C6_H$	CCL3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C7_H$	CCH3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C8_H$ [2)]	T2CON	00X0-0000$_B$	T2PS	I3FR	–	T2R1	T2R0	T2CM	T2I1	T2I0
CA_H	CRCL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CB_H	CRCH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CC_H	TL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CD_H	TH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D0_H$ [2)]	PSW	00_H	CY	AC	F0	RS1	RS0	OV	F1	P

1) X means that the value is undefined and the location is reserved
2) Bit-addressable special function registers
3) C505A only
4) C505CA only

Table 2-2
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$D8_H$ [2)]	ADCON0	$00X0\text{-}0000_B$	BD	CLK	–	BSY	ADM	MX2	MX1	MX0
$D9_H$	ADDATH	00_H	.9	.8	.7	.6	.5	.4	.3	.2
DA_H	ADDATL	$00XX\text{-}XXXX_B$	.1	.0	–	–	–	–	–	–
DC_H	ADCON1	$01XX\text{-}X000_B$	ADCL1	ADCL0	–	–	–	MX2	MX1	MX0
$E0_H$ [2)]	ACC	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E8_H$ [2)]	P4 [3)]	$XXXX\text{-}XX11_B$	–	–	–	–	–	–	–	–
$E8_H$ [2)]	P4 [4)]	$XXXX\text{-}XX11_B$	–	–	–	–	–	–	RXDC	TXDC
$F0_H$ [2)]	B	00_H	.7	.6	.5	.4	.3	.2	.1	.0
FC_H [5) 6)]	VR0	$C5_H$	.7	.6	.5	.4	.3	.2	.1	.0
FD_H [5) 6)]	VR1	05_H	.7	.6	.5	.4	.3	.2	.1	.0
FE_H [5) 6)]	VR2	[7)]	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) Bit-addressable special function registers
3) C505A only
4) C505CA only
5) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.
6) These are read-only registers
7) The content of this SFR varies with the actual of the step C505A (eg. 11_H for the first step)

Table 2-3
Contents of the CAN Registers in numeric order of their addresses (C505CA only)

Addr. n=1-F$_H$ 1)	Register	Content after Reset 2)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F700$_H$	CR	01$_H$	TEST	CCE	0	0	EIE	SIE	IE	INIT
F701$_H$	SR	XX$_H$	BOFF	EWRN	–	RXOK	TXOK	LEC2	LEC1	LEC0
F702$_H$	IR	XX$_H$	INTID							
F704$_H$	BTR0	UU$_H$	SJW		BRP					
F705$_H$	BTR1	0UUU. UUUU$_B$	0	TSEG2			TSEG1			
F706$_H$	GMS0	UU$_H$	ID28-21							
F707$_H$	GMS1	UUU1. 1111$_B$	ID20-18			1	1	1	1	1
F708$_H$	UGML0	UU$_H$	ID28-21							
F709$_H$	UGML1	UU$_H$	ID20-13							
F70A$_H$	LGML0	UU$_H$	ID12-5							
F70B$_H$	LGML1	UUUU. U000$_B$	ID4-0					0	0	0
F70C$_H$	UMLM0	UU$_H$	ID28-21							
F70D$_H$	UMLM1	UU$_H$	ID20-18			ID17-13				
F70E$_H$	LMLM0	UU$_H$	ID12-5							
F70F$_H$	LMLM1	UUUU. U000$_B$	ID4-0					0	0	0
F7n0$_H$	MCR0	UU$_H$	MSGVAL		TXIE		RXIE		INTPND	
F7n1$_H$	MCR1	UU$_H$	RMTPND		TXRQ		MSGLST CPUUPD		NEWDAT	
F7n2$_H$	UAR0	UU$_H$	ID28-21							
F7n3$_H$	UAR1	UU$_H$	ID20-18			ID17-13				
F7n4$_H$	LAR0	UU$_H$	ID12-5							
F7n5$_H$	LAR1	UUUU. U000$_B$	ID4-0					0	0	0
F7n6$_H$	MCFG	UUUU. UU00$_B$	DLC				DIR	XTD	0	0

1) The notation “n“ (n= 1 to F) in the address definition defines the number of the related message object.
2) “X“ means that the value is undefined and the location is reserved. “U“ means that the value is unchanged by a reset operation. “U“ values are undefined (as “X“) after a power-on reset operation

Table 2-3
Contents of the CAN Registers in numeric order of their addresses (cont'd) (C505CA only)

Addr. n=1-F$_H$ 1)	Register	Content after Reset 2)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F7n7$_H$	DB0	XX$_H$	.7	.6	.5	.4	.3	.2	.1	.0
F7n8$_H$	DB1	XX$_H$	.7	.6	.5	.4	.3	.2	.1	.0
F7n9$_H$	DB2	XX$_H$	.7	.6	.5	.4	.3	.2	.1	.0
F7nA$_H$	DB3	XX$_H$	.7	.6	.5	.4	.3	.2	.1	.0
F7nB$_H$	DB4	XX$_H$	.7	.6	.5	.4	.3	.2	.1	.0
F7nC$_H$	DB5	XX$_H$	.7	.6	.5	.4	.3	.2	.1	.0
F7nD$_H$	DB6	XX$_H$	.7	.6	.5	.4	.3	.2	.1	.0
F7nE$_H$	DB7	XX$_H$	.7	.6	.5	.4	.3	.2	.1	.0

1) The notation "n" (n= 1 to F) in the address definition defines the number of the related message object.
2) "X" means that the value is undefined and the location is reserved. "U" means that the value is unchanged by a reset operation. "U" values are undefined (as "X") after a power-on reset operation

3 A/D Converter

The C505A includes a high performance / high speed 10-bit A/D-Converter (ADC) with 8 analog input channels. It operates with a successive approximation technique and uses self calibration mechanisms for reduction and compensation of offset and linearity errors. The A/D converter provides the following features:

- 8 multiplexed input channels (port 1), which can also be used as digital inputs/outputs
- 10-bit resolution
- Single or continuous conversion mode
- Internal start-of-conversion trigger capability
- Interrupt request generation after each conversion
- Using successive approximation conversion technique via a capacitor array
- Built-in hidden calibration of offset and linearity errors

The externally applied reference voltage range has to be held on a fixed value within the specifications. The main functional blocks of the A/D converter are shown in **figure 3-1**.

3.1 A/D Converter Operation

An internal start of a single A/D conversion is triggered by a write-to-ADDATL instruction. The start procedure itself is independent of the value which is written to ADDATL. When single conversion mode is selected (bit ADM=0) only one A/D conversion is performed. In continuous mode (bit ADM=1), after completion of an A/D conversion a new A/D conversion is triggered automatically until bit ADM is reset.

The busy flag BSY (ADCON0.4) is automatically set when an A/D conversion is in progress. After completion of the conversion it is reset by hardware. This flag can be read only, a write has no effect. The interrupt request flag IADC (IRCON.0) is set when an A/D conversion is completed.

The bits MX0 to MX2 in special function register ADCON0 and ADCON1 are used for selection of the analog input channel. The bits MX0 to MX2 are represented in both registers ADCON0 and ADCON1; however, these bits are present only once. Therefore, there are two methods of selecting an analog input channel : If a new channel is selected in ADCON1 the change is automatically done in the corresponding bits MX0 to MX2 in ADCON0 and vice versa.

Port 1 is a dual purpose input/output port. These pins can be used either for digital I/O functions or as the analog inputs. If less than 8 analog inputs are required, the unused analog inputs at port 1 are free for digital I/O functions.

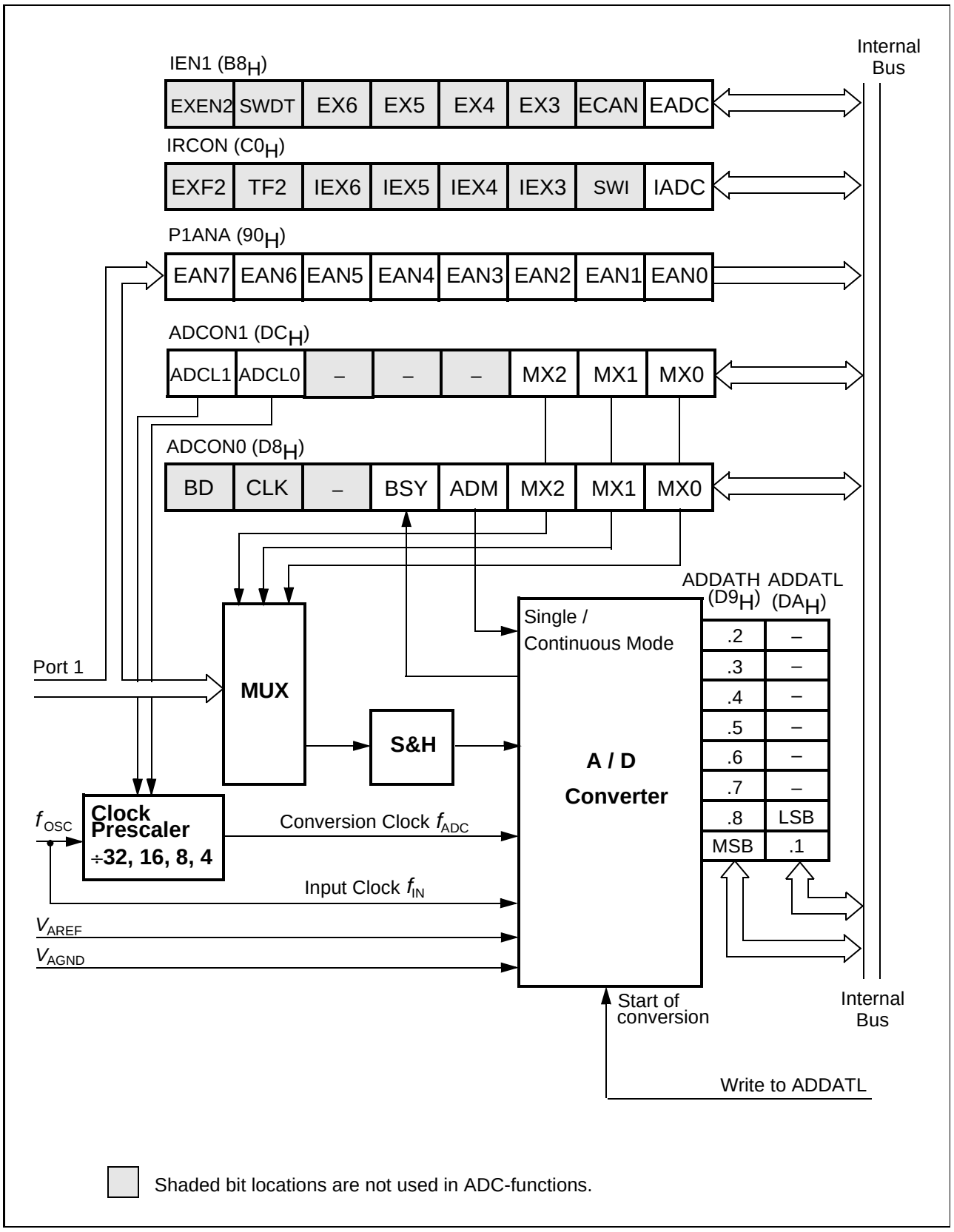


Figure 3-1
Block Diagram of the A/D Converter

3.2 A/D Converter Registers

This section describes the bits/functions of all registers which are used by the A/D converter.

Special Function Register ADDATH (Address $D9_H$) **Reset Value : 00_H**
Special Function Register ADDATL (Address DA_H) **Reset Value : $00XXXXXX_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$D9_H$	MSB .9	.8	.7	.6	.5	.4	.3	.2	ADDATH
DA_H	.1	LSB .0	–	–	–	–	–	–	ADDATL

The registers ADDATH and ADDATL hold the 10-bit conversion result in left justified data format. The most significant bit of the 10-bit conversion result is bit 7 of ADDATH. The least significant bit of the 10-bit conversion result is bit 6 of ADDATL. To get a 10-bit conversion result, both ADDAT registers must be read. If an 8-bit conversion result is required, only the reading of ADDATH is necessary. The data remains in ADDAT until it is overwritten by the next converted data. ADDAT can be read or written under software control. lf the A/D converter of the C505A is not used, register ADDATH can be used as an additional general purpose register.

Special Function Register ADCON0 (Address $D8_H$) **Reset Value : 00_H**
Special Function Register ADCON1 (Address DC_H) **Reset Value : $01XXX000_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$D8_H$	BD	CLK	–	BSY	ADM	MX2	MX1	MX0	ADCON0
DC_H	ADCL1	ADCL0	–	–	–	MX2	MX1	MX0	ADCON1

The shaded bits are not used for A/D converter control.

Bit	Function
–	Reserved bits for future use
BSY	Busy flag This flag indicates whether a conversion is in progress (BSY = 1). The flag is cleared by hardware when the conversion is finished.
ADM	A/D conversion mode When set, a continuous A/D conversion is selected. If cleared during a running A/D conversion, the conversion is stopped at its end.
MX2 - MX0	A/D converter input channel select bits Bits MX2-0 can be written or read either in ADCON0 or ADCON1. The channel selection done by writing to ADCON 1(0) overwrites the selection in ADCON 0(1) when ADCON 1(0) is written after ADCON 0(1). The analog inputs are selected according the following table :

MX2	MX1	MX0	Selected Analog Input
0	0	0	P1.0 / AN0 / $\overline{INT3}$ / CC0
0	0	1	P1.1 / AN1 / INT4 / CC1
0	1	0	P1.2 / AN2 / INT5 / CC2
0	1	1	P1.3 / AN3 / INT6 / CC3
1	0	0	P1.4 / AN4
1	0	1	P1.5 / AN5 / T2EX
1	1	0	P1.6 / AN6 / CLKOUT
1	1	1	P1.7 / AN7 / T2

Bit	Function
ADCL1 ADCL0	A/D converter clock prescaler selection ADCL1 and ADCL0 select the prescaler ratio for the A/D conversion clock f_{ADC}. Depending on the clock rate f_{OSC} of the C505A, f_{ADC} must be adjusted in a way that the resulting conversion clock f_{ADC} is less than or equal to 2 MHz (see section 3.3). The prescaler ratio is selected according to the following table :

ADCL1	ADCL0	Prescaler Ratio
0	0	divide by 4
0	1	divide by 8 (default after reset)
1	0	divide by 16
1	1	divide by 32

Note : Generally, before entering the power-down mode, an A/D conversion in progress must be stopped. If a single A/D conversion is running, it must be terminated by polling the BSY bit or waiting for the A/D conversion interrupt. In continuous conversion mode, bit ADM must be cleared and the last A/D conversion must be terminated before entering the power-down mode.

A single A/D conversion is started by writing to SFR ADDATL with dummy data. A continuous conversion is started under the following conditions :

- By setting bit ADM during a running single A/D conversion
- By setting bit ADM when at least one A/D conversion has occurred after the last reset operation.
- By writing ADDATL with dummy data after bit ADM has been set before (if no A/D conversion has occurred after the last reset operation).

When bit ADM is reset by software in continuous conversion mode, the just running A/D conversion is stopped after its end.

The A/D converter interrupt is controlled by bits which are located in the SFRs IEN1 and IRCON.

Special Function Register IEN1 (Address $B8_H$) **Reset Value : 00_H**
Special Function Register IRCON (Address $C0_H$) **Reset Value : 00_H**

Bit No.	MSB BF_H	BE_H	BD_H	BC_H	BB_H	BA_H	$B9_H$	LSB $B8_H$	
$B8_H$	EXEN2	SWDT	EX6	EX5	EX4	EX3	ECAN	EADC	IEN1

	$C7_H$	$C6_H$	$C5_H$	$C4_H$	$C3_H$	$C2_H$	$C1_H$	$C0_H$	
$C0_H$	EXF2	TF2	IEX6	IEX5	IEX4	IEX3	SWI	IADC	IRCON

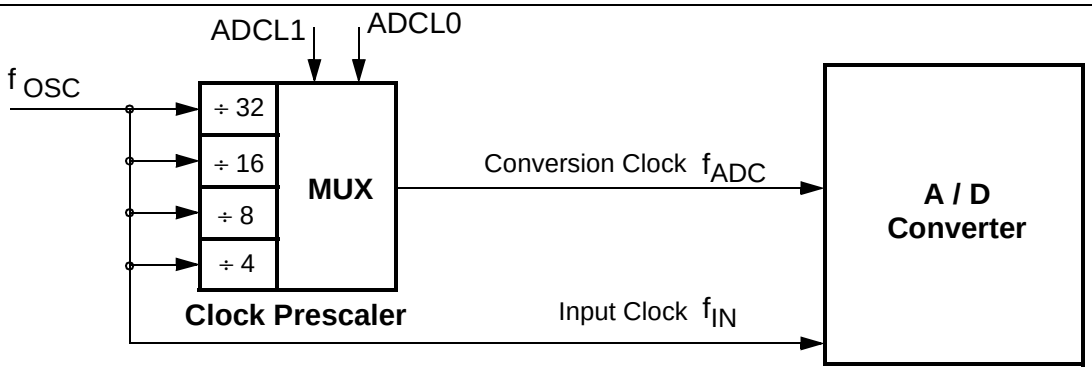
The shaded bits are not used for A/D converter control.

Bit	Function
EADC	Enable A/D converter interrupt If EADC = 0, the A/D converter interrupt is disabled.
SWI	This bit can be set by software to generate an interrupt. The interrupt service routine is at $004B_H$. This bit is cleared when the interrupt is processed. This interrupt is enabled by setting bit IEN1.1(ECAN).

3.3 A/D Converter Clock Selection

The ADC uses two clock signals for operation : the conversion clock f_{ADC} (=1/t_{ADC}) and the input clock f_{IN} (=1/t_{IN}). f_{ADC} is derived from the C505A system clock f_{OSC} which is applied at the XTAL pins via the ADC clock prescaler as shown in **figure 3-2**. The input clock f_{IN} is equal to f_{OSC} The conversion f_{ADC} clock is limited to a maximum frequency of 2 MHz. Therefore, the ADC clock prescaler must be programmed to a value which assures that the conversion clock does not exceed 2 MHz. The prescaler ratio is selected by the bits ADCL1 and ADCL0 of SFR ADCON1.

The table in **figure 3-2** shows the prescaler ratio which must be selected by ADCL1 and ADCL0 for typical system clock rates. Up to 8 MHz system clock the prescaler ratio 4 is selected. Using a system clock greater than 8 MHz and less than 16 MHz, the prescaler ratio of at least 8 must be selected. A prescaler ratio of at least 16 must be selected when using a system clock greater than 16 MHz. A prescaler ratio of 32 can used for any of the above frequency ranges.



Condition : $f_{ADC\ max} = 2$ MHz $\quad f_{IN} = f_{OSC} = \frac{1}{CLP}$

MCU System Clock Rate (f_{OSC})	f_{IN} [MHz]	Prescaler Ratio	f_{ADC} [MHz]	ADCL1	ADCL0
2 MHz	2	÷ 4	0.5	0	0
6 MHz	6	÷ 4	1.5	0	0
8 MHz	8	÷ 4	2	0	0
12 MHz	12	÷ 8	1.5	0	1
16 MHz	16	÷ 8	2	0	1
20 MHz	20	÷ 16	1.25	1	0

Figure 3-2
A/D Converter Clock Selection

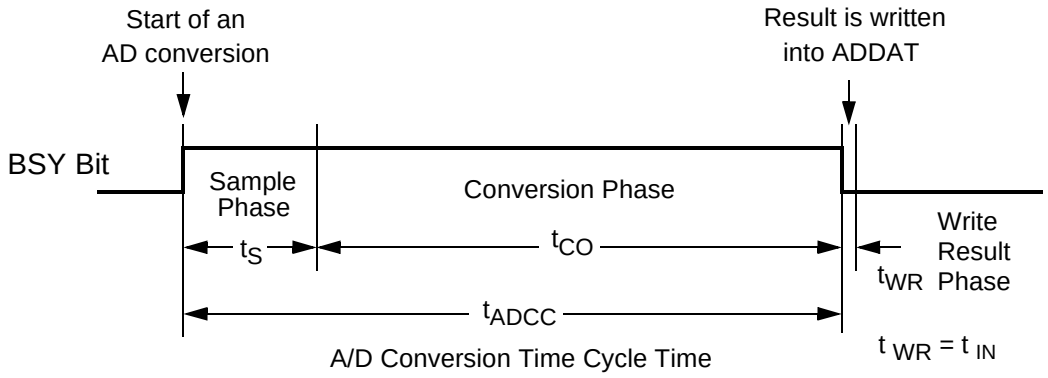
The duration of an A/D conversion is a multiple of the period of the f_{IN} clock signal. The calculation of the A/D conversion time is shown in the next section.

3.4 A/D Conversion Timing

An A/D conversion is started by writing into the SFR ADDATL with dummy data. A write to SFR ADDATL will start a new conversion even if a conversion is currently in progress. The conversion begins with the next machine cycle, and the BSY flag in SFR ADCON0 will be set.
The A/D conversion procedure is divided into three parts :

- Sample phase (t_S), used for sampling the analog input voltage.
- Conversion phase (t_{CO}), used for the real A/D conversion (includes calibration).
- Write result phase (t_{WR}), used for writing the conversion result into the ADDAT registers.

The total A/D conversion time is defined by t_{ADCC} which is the sum of the two phase times t_S and t_{CO}. The duration of the three phases of an A/D conversion is specified by their corresponding timing parameter as shown in **figure 3-3**.



$t_{ADCC} = t_S + t_{CO}$
PS = Prescaler value

Prescaler Ratio (=PS)	t_S	t_{CO}	t_{ADCC}
32	64 x t_{IN}	320 x t_{IN}	384 x t_{IN}
16	32 x t_{IN}	160 x t_{IN}	192 x t_{IN}
8	16 x t_{IN}	80 x t_{IN}	96 x t_{IN}
4	8 x t_{IN}	40 x t_{IN}	48 x t_{IN}

Figure 3-3
A/D Conversion Timing

Sample Time t_S :
During this time the internal capacitor array is connected to the selected analog input channel and is loaded with the analog voltage to be converted. The analog voltage is internally fed to a voltage comparator. With beginning of the sample phase the BSY bit in SFR ADCON0 is set.

Conversion Time t_{CO} :
During the conversion time the analog voltage is converted into a 10-bit digital value using the successive approximation technique with a binary weighted capacitor network. During an A/D conversion also a calibration takes place. During this calibration alternating offset and linearity calibration cycles are executed (see also section 3.5). At the end of the calibration time the BSY bit is reset and the IADC bit in SFR IRCON is set indicating an A/D converter interrupt condition.

Write Result Time t_{WR} :
At the result phase the conversion result is written into the ADDAT registers.

Figure 3-4 shows how an A/D conversion is embedded into the microcontroller cycle scheme using the relation 6 x t_{IN} = 1 instruction cycle. It also shows the behaviour of the busy flag (BSY) and the interrupt flag (IADC) during an A/D conversion.

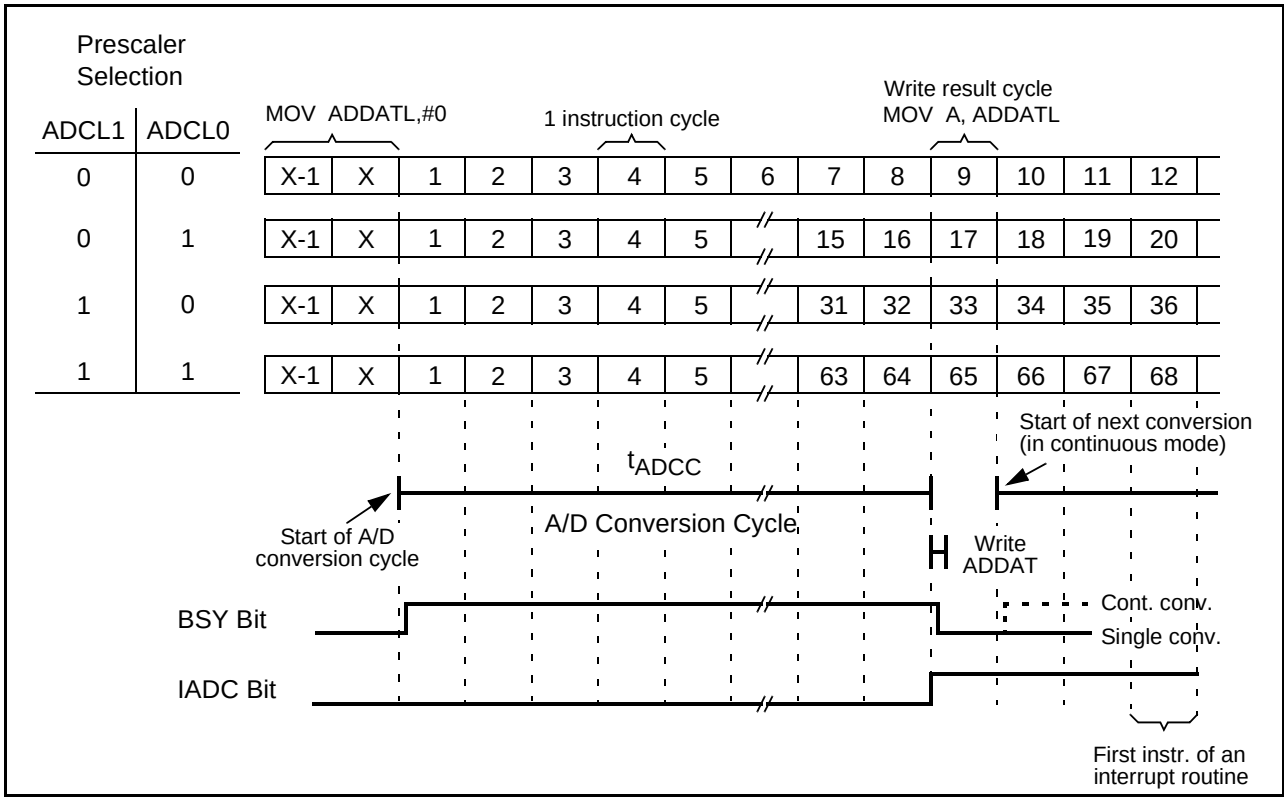


Figure 3-4
A/D Conversion Timing in Relation to Processor Cycles

Depending on the selected prescaler ratio (see **figure 3-2**), four different relationships between machine cycles and A/D conversion are possible. The A/D conversion is started when SFR ADDATL is written with dummy data. This write operation may take one or two machine cycles. In **figure 3-4**, the instruction MOV ADDATL,#0 starts the A/D conversion (machine cycle X-1 and X). The total A/D conversion (sample, conversion, and calibration phase) is finished with the end of the 8th, 16th, 32nd, or 64th machine cycle after the A/D conversion start. In the next machine cycle the conversion result is written into the ADDAT registers and can be read in the same cycle by an instruction (e.g. MOV A,ADDATL). If continuous conversion is selected (bit ADM set), the next conversion is started with the beginning of the machine cycle which follows the write result cycle.

The BSY bit is set at the beginning of the first A/D conversion machine cycle and reset at the beginning of the write result cycle. If continuous conversion is selected, BSY is again set with the beginning of the machine cycle which follows the write result cycle.

The interrupt flag IADC is set at the end of the A/D conversion. If the A/D converter interrupt is enabled and the A/D converter interrupt is prioritized to be serviced immediately, the first instruction of the interrupt service routine will be executed in the third machine cycle which follows the write result cycle. IADC must be reset by software.

Depending on the application, typically there are three methods to handle the A/D conversion in the C505A.

- Software delay
  The machine cycles of the A/D conversion are counted and the program executes a software delay (e.g. NOPs) before reading the A/D conversion result in the write result cycle. This is the fastest method to get the result of an A/D conversion.
- Polling BSY bit
  The BSY bit is polled and the program waits until BSY=0. Attention : a polling JB instruction which is two machine cycles long, possibly may not recognize the BSY=0 condition during the write result cycle in the continuous conversion mode.
- A/D conversion interrupt
  After the start of an A/D conversion the A/D converter interrupt is enabled. The result of the A/D conversion is read in the interrupt service routine. If other C505A interrupts are enabled, the interrupt latency must be regarded. Therefore, this software method is the slowest method to get the result of an A/D conversion.

Depending on the oscillator frequency of the C505A and the selected divider ratio of the conversion clock prescaler the total time of an A/D conversion is calculated according **figure 3-3** and **table 3-1. Figure 3-5** on the next page shows the minimum A/D conversion time in relation to the oscillator frequency f_{OSC}. The minimum conversion time is 6 µs and can be achieved at f_{OSC} of 8 or 16 MHz (or whenever f_{ADC} = 2 MHz).

Table 4-1
A/D Conversion Time for Dedicated System Clock Rates

f_{OSC} [MHz]	Prescaler Ratio PS	f_{ADC} [MHz]	Sample Time t_S [µs]	Total Conversion Time t_{ADCC} [µs]
2 MHz	÷ 4	0.5	4	24
6 MHz	÷ 4	1.5	1.33	8
8 MHz	÷ 4	2	1	6
12 MHz	÷ 8	1.5	1.33	8
16 MHz	÷ 8	2	1	6
20 MHz	÷ 16	1.25	1.6	9.6

Note : The prescaler ratios in **table 3-1** are minimum values.

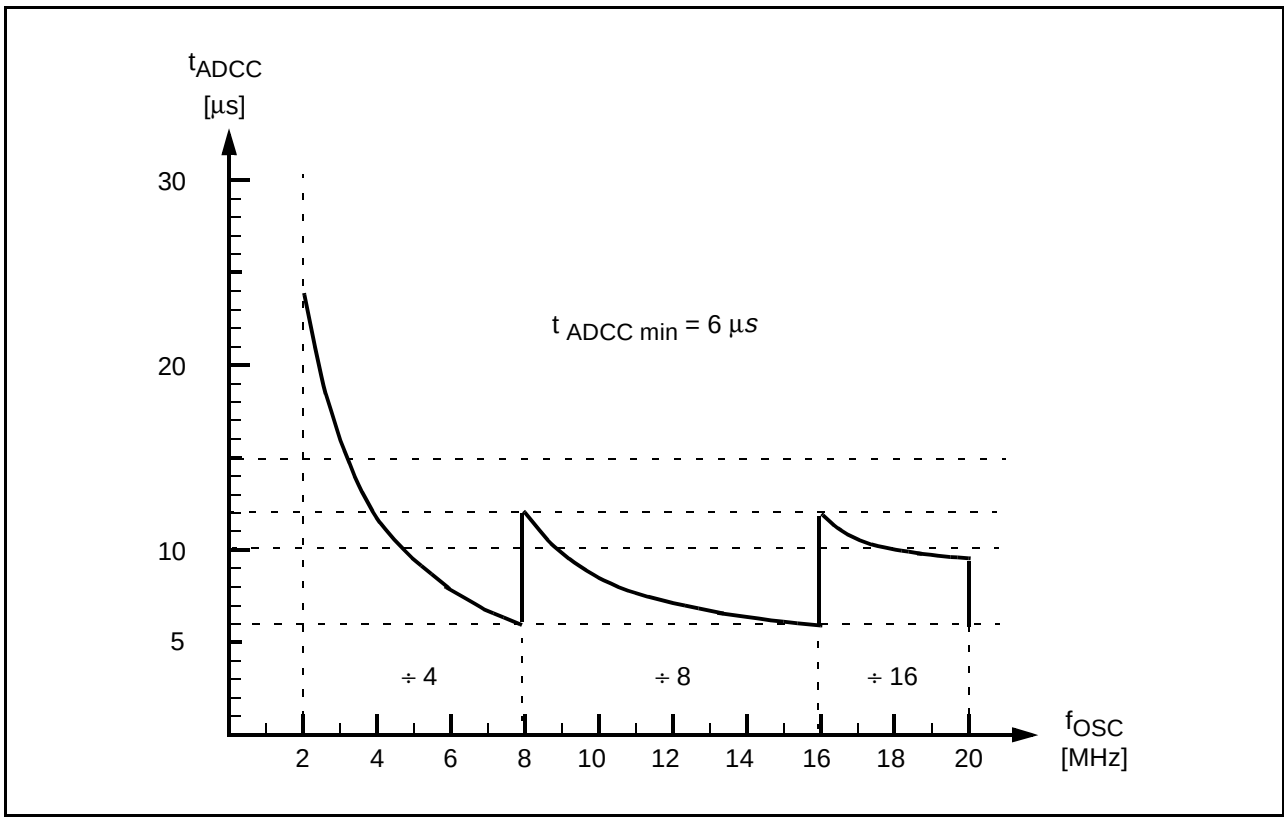


Figure 3-5
Minimum A/D Conversion Time in Relation to System Clock

3.5 A/D Converter Calibration

The C505A A/D converter includes hidden internal calibration mechanisms which assure a safe functionality of the A/D converter according to the DC characteristics. The A/D converter calibration is implemented in a way that a user program which executes A/D conversions is not affected by its operation. Further, the user program has no control over the calibration mechanism. The calibration itself executes two basic functions :

- Offset calibration : correction of offset errors of comparator and the capacitor network
- Linearity calibration : correction of the binary weighted capacitor network

The A/D converter calibration operates in two phases : calibration after a reset operation and calibration at each A/D conversion. The calibration phases are controlled by a state machine in the A/D converter. This state machine executes the calibration phases and stores the calibration results dynamically in a small calibration RAM.

After a reset operation the A/D calibration is automatically started. This reset calibration phase which takes 3328 f_{ADC} clocks, alternating offset and linearity calibration is executed. Therefore, at 8 MHz oscillator frequency and with the default after reset prescaler value of 4, a reset calibration time of approx. 1.66 ms is reached. For achieving a proper reset calibration, the f_{ADC} prescaler value must satisfy the condition $f_{ADC\,max} \leq 2$ MHz. If this condition is not met at a specific oscillator frequency with the default prescaler value after reset, the f_{ADC} prescaler must be adjusted immediately after reset by setting bits ADCL1 and ADCL0 in SFR ADCON1 to a suitable value. It is also recommended to have the proper voltages, as specified in the DC specifications, applied at the V_{AREF} and V_{AREF} pins before the reset calibration has started.

After the reset calibration phase the A/D converter is calibrated according to its DC characteristics. Nevertheless, during the reset calibration phase single or continuous A/D can be executed. In this case it must be regarded that the reset calibration is interrupted and continued after the end of the A/D conversion. Therefore, interrupting the reset calibration phase by A/D conversions extends the total reset calibration time. If the specified total unadjusted error (TUE) has to be valid for an A/D conversion, it is recommended to start the first A/D conversions after reset when the reset calibration phase is finished. Depending on the oscillator frequency used, the reset calibration phase can be possibly shortened by setting ADCL1 and ADCL0 (prescaler value) to its final value immediately after reset.

After the reset calibration, a second calibration mechanism is initiated. This calibration is coupled to each A/D conversion**.** With this second calibration mechanism alternatively offset and linearity calibration values, stored in the calibration RAM, are always checked when an A/D conversion is executed and corrected if required.

3.5.1 A/D Converter Analog Input Selection

The analog inputs are located at port 1. The corresponding pins have a port structure, which allows to use them either as digital I/O pins or as analog inputs (see section 6.1.3.2). The analog input function of these digital/analog port lines are selected via the register P1ANA. This register lies in the mapped SFR area and can be accessed when bit RMAP in SFR SYSCON is set when writing to its address (90_H). If a specific bit location of P1ANA is set, the corresponding port line is configured as a digital input. With a 0 in the bit location the port line operates as analog port.

Special Function Registers P1ANA (Address 90_H) **Reset Value : FF_H**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
90_H	EAN7	EAN6	EAN5	EAN4	EAN3	EAN2	EAN1	EAN0	P1ANA

Bit	Function
EAN7 - EAN0	Enable analog port 1 inputs If EANx (x = 7-0) is cleared, port pin P1.x is enabled for operation as an analog input. If EANx is set, port pin P1.x is enabled for digital I/O function (default after reset).

4 OTP Memory Operation

The C505A-4E is the OTP version in the C505A microcontroller with a 32K byte one-time programmable (OTP) program memory. With the C505A-4E fast programming cycles are achieved (1 byte in 100 µsec). Also several levels of OTP memory protection can be selected. The basic functionality of the C505A-4E as microcontroller is identical to the C505A-L (romless part) functionality.

4.1 Programming Configuration

During normal program execution the C505A-4E behaves like the C505A-L. For programming the device, the C505A-4E must be put into the programming mode. This, typically, is done not in-system but in a special programming hardware. In the programming mode the C505A-4E operates as a slave device similar as an EPROM standalone memory device and must be controlled with address/ data information, control lines, and an external 11.5 V programming voltage.

In the programming mode port 0 provides the bidirectional data lines and port 2 is used for the multiplexed address inputs. The upper address information at port 2 is latched with the signal PALE. For basic programming mode selection the inputs RESET, $\overline{PSEN}$, $\overline{EA}/V_{PP}$, ALE and PMSEL1/0 and $\overline{PSEL}$ are used. Further, the inputs PMSEL1,0 are required to select the access types (e.g. program/verify data, write lock bits, ...) in the programming mode. In programming mode V_{CC}/V_{SS} and a clock signal at the XTAL pins must be applied to the C505A-4E. The 11.5 V external programming voltage is input through the $\overline{EA}/V_{PP}$ pin.

Figure 4-1 shows the pins of the C505A-4E which are required for controlling of the OTP programming mode.

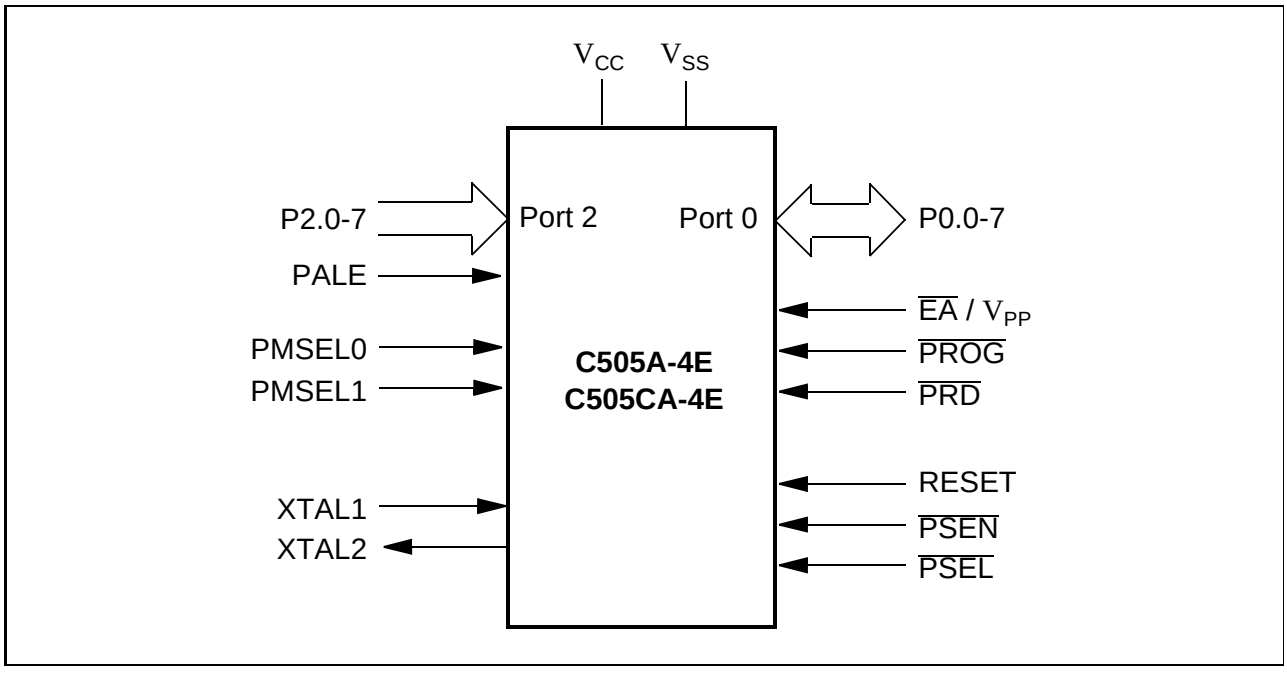


Figure 4-1
Programming Mode Configuration

4.2 Pin Configuration

Figure 4-2 shows the detailed pin configuration of the C505A-4E in programming mode.

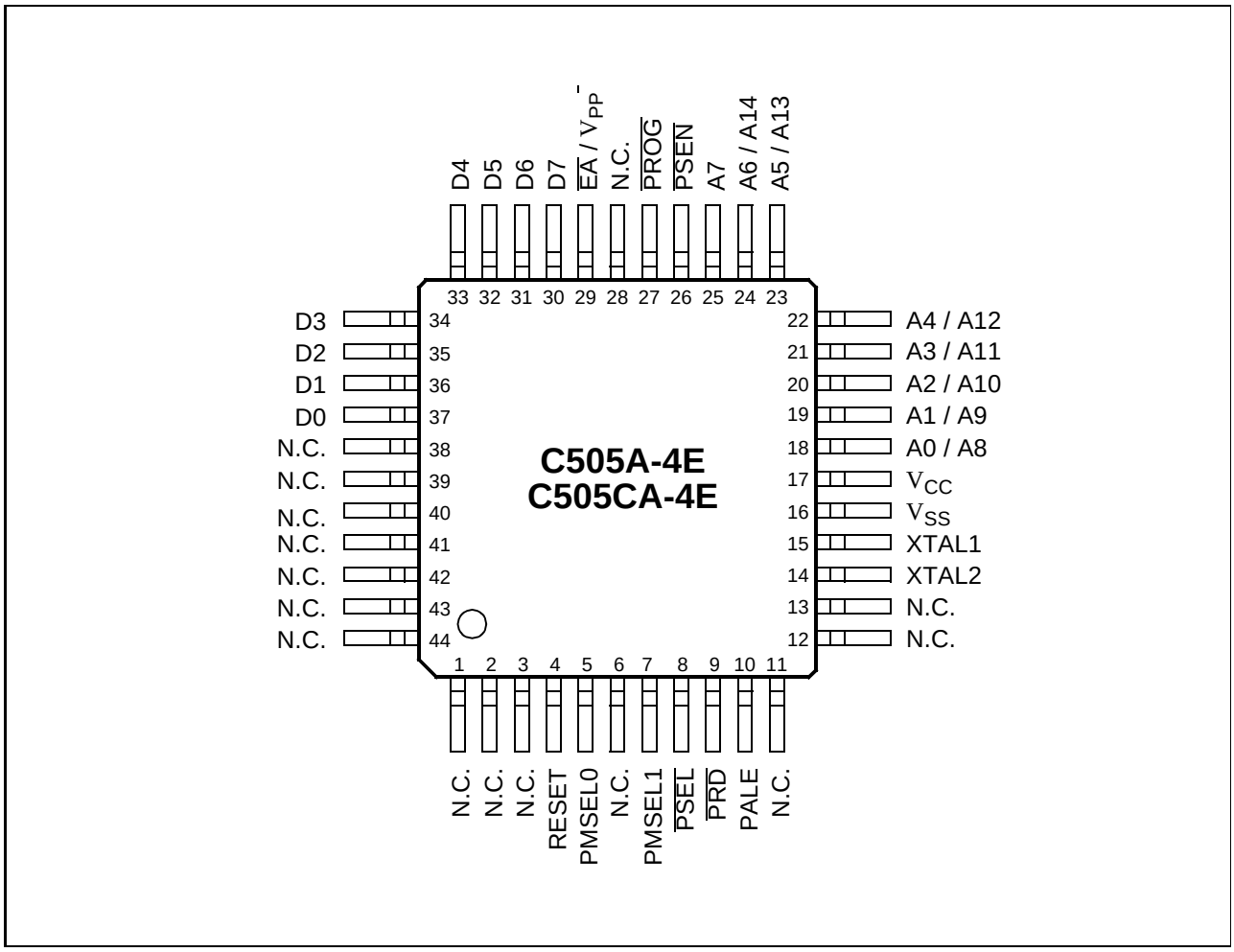


Figure 4-2
OTP Programming Mode Pin Configuration (Top View)

4.3 Pin Definitions

The following **figure 4-1** contains the functional description of all C505A-4E pins which are required for OTP memory programming

Table 4-1
Pin Definitions and Functions of the C505A-4E in Programming Mode

<table>
<tr><th>Symbol</th><th>Pin Number
P-MQFP-44</th><th>I/O *)</th><th>Function</th></tr>
<tr><td>RESET</td><td>4</td><td>I</td><td>Reset
This input must be at static “1“ (active) level during the whole programming mode.</td></tr>
<tr><td>PMSEL0
PMSEL1</td><td>5
7</td><td>I
I</td><td>Programming mode selection pins
These pins are used to select the different access modes in programming mode. PMSEL1,0 must satisfy a setup time to the rising edge of PALE. When the logic level of PMSEL1,0 is changed, PALE must be at low level.
<table>
<tr><th>PMSEL1</th><th>PMSEL0</th><th>Access Mode</th></tr>
<tr><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>Read signature bytes</td></tr>
<tr><td>1</td><td>0</td><td>Program/read lock bits</td></tr>
<tr><td>1</td><td>1</td><td>Program/read OTP memory byte</td></tr>
</table></td></tr>
<tr><td>$\overline{\text{PSEL}}$</td><td>8</td><td>I</td><td>Basic programming mode select
This input is used for the basic programming mode selection and must be switched according figure 4-3.</td></tr>
<tr><td>$\overline{\text{PRD}}$</td><td>9</td><td>I</td><td>Programming mode read strobe
This input is used for read access control for OTP memory read, version byte read, and lock bit read operations.</td></tr>
<tr><td>PALE</td><td>10</td><td>I</td><td>Programming address latch enable
PALE is used to latch the high address lines. The high address lines must satisfy a setup and hold time to/from the falling edge of PALE. PALE must be at low level when the logic level of PMSEL1,0 is changed.</td></tr>
<tr><td>XTAL2</td><td>14</td><td>O</td><td>XTAL2
Output of the inverting oscillator amplifier.</td></tr>
<tr><td>XTAL1</td><td>15</td><td>I</td><td>XTAL1
Input to the oscillator amplifier.</td></tr>
</table>

*) I = Input
O = Output

Table 4-1
Pin Definitions and Functions of the C505A-4E in Programming Mode (cont'd)

Symbol	Pin Number P-MQFP-44	I/O *)	Function
V_{SS}	16	–	**Circuit ground potential** must be applied in programming mode.
V_{CC}	17	–	**Power supply terminal** must be applied in programming mode.
P2.0-7	18-25	I	**Address lines** P2.0-7 are used as multiplexed address input lines A0-A7 and A8-A14. A8-A14 must be latched with PALE.
$\overline{PSEN}$	26	I	**Program store enable** This input must be at static "0" level during the whole programming mode.
$\overline{PROG}$	27	I	**Programming mode write strobe** This input is used in programming mode as a write strobe for OTP memory program, and lock bit write operations During basic programming mode selection a low level must be applied to $\overline{PROG}$.
$\overline{EA}/V_{PP}$	29	–	**Programming voltage** This pin must be at 11.5 V (V_{PP}) voltage level during programming of an OTP memory byte or lock bit. During an OTP memory read operation this pin must be at V_{IHx} high level. This pin is also used for basic programming mode selection. At basic programming mode selection a low level must be applied to $\overline{EA}/V_{PP}$.
P0.7-0	30-37	I/O	**Data lines 0-7** During programming mode, data bytes are transferred via the bidirectional D7-0 lines which are located at port 0.
N.C.	1-3, 6, 11-13, 28, 38-44	–	**Not Connected** These pins should not be connected in programming mode.

*) I = Input
O = Output

4.4 Programming Mode Selection

The selection for the OTP programming mode can be separated into two different parts :

- Basic programming mode selection
- Access mode selection

With the basic programming mode selection the device is put into the mode in which it is possible to access the OTP memory through the programming interface logic. Further, after selection of the basic programming mode, OTP memory accesses are executed by using one of the access modes. These access modes are OTP memory byte program/read, version byte read, and program/read lock byte operations.

4.4.1 Basic Programming Mode Selection

The basic programming mode selection scheme is shown in **figure 4-3**.

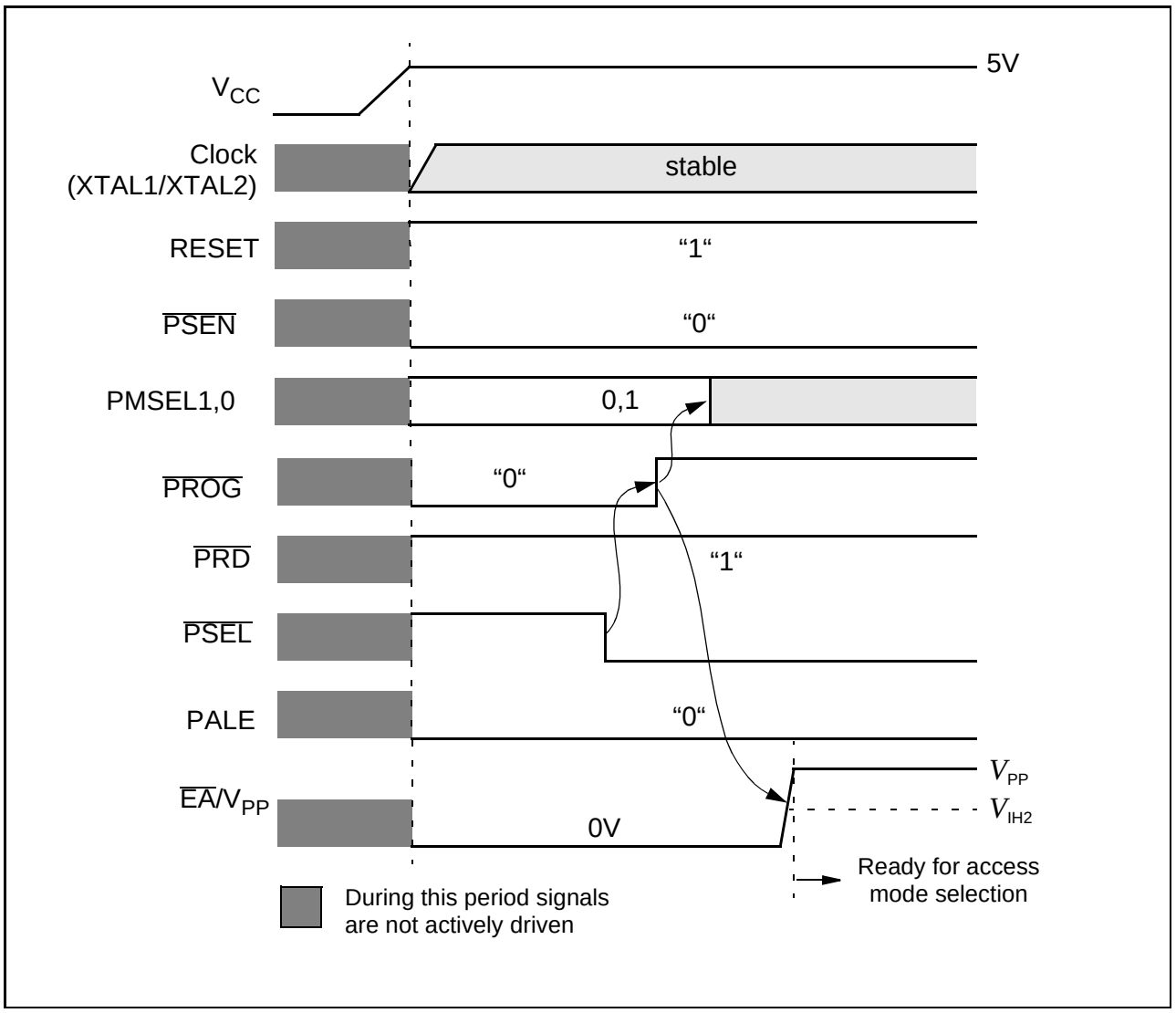


Figure 4-3
Basic Programming Mode Selection

The basic programming mode is selected by executing the following steps :

- With a stable V_{CC} a clock signal is applied to the XTAL pins; the RESET pin is set to “1“ level and the $\overline{PSEN}$ pin is set to “0“ level.
- $\overline{PROG}$, PALE, PMSEL1 and $\overline{EA}/V_{PP}$ are set to “0“ level; $\overline{PRD}$, $\overline{PSEL}$, and PMSEL0 are set to “1“ level.
- $\overline{PSEL}$ is switched from “1“ to “0“ level and thereafter $\overline{PROG}$ is switched to “1“ level.
- PMSEL1,0 can now be changed; after $\overline{EA}/V_{PP}$ has been set to V_{IHx} high level or to V_{PP} the OTP memory is ready for access.

The pins RESET and $\overline{PSEN}$ must stay at “1“ respectively “0“ static signal level during the whole programming mode. With a falling edge of $\overline{PSEL}$ the logic state of $\overline{PROG}$ and $\overline{EA}/V_{PP}$ is internally latched. These two signals are now used as programming write pulse signal ($\overline{PROG}$) and as programming voltage input pin V_{PP}. After the falling edge of $\overline{PSEL}$, $\overline{PSEL}$ must stay at “0“ state during all programming operations.

Note: If protection level 1 to 3 has been programmed (see section 4.6) and the programming mode has been left, it is no more possible to enter the programming mode !

4.4.2 OTP Memory Access Mode Selection

When the C505A-4E has been put into the programming mode using the basic programming mode selection, several access modes of the OTP memory programming interface are available. The conditions for the different control signals of these access modes are listed in **table 4-2**.

Table 4-2
Access Modes Selection

Access Mode	$\overline{EA}/V_{PP}$	$\overline{PROG}$	$\overline{PRD}$	PMSEL		Address (Port 2)	Data (Port 0)
				1	0		
Program OTP memory byte	V_{PP}	⎍	H	H	H	A0-7 A8-14	D0-7
Read OTP memory byte	V_{IHx}	H	⎍				
Program OTP lock bits	V_{PP}	⎍	H	H	L	–	D1,D0 see **table 4-3**
Read OTP lock bits	V_{IHx}	H	⎍				
Read OTP version byte	V_{IHx}	H	⎍	L	H	Byte addr. of version byte	D0-7

The access modes from the table above are basically selected by setting the two PMSEL1,0 lines to the required logic level. The $\overline{PROG}$ and $\overline{PRD}$ signal are the write and read strobe signal. Data is transferred via port 0 and addresses are applied to port 2.

The following sections describes the details of the different access modes.

4.5 Program / Read OTP Memory Bytes

The program/read OTP memory byte access mode is defined by PMSEL1,0 = 1,1. It is initiated when the PMSEL1,0 = 1,1 is valid at the rising edge of PALE. With the falling edge of PALE the upper addresses A8-A14 of the 15-bit OTP memory address are latched. After A8-A14 has been latched, A0-A7 is put on the address bus (port 2). A0-A7 must be stable when $\overline{\text{PROG}}$ is low or $\overline{\text{PRD}}$ is low. If subsequent OTP address locations are accessed with constant address information at the high address lines A8-14, A8-A14 must only be latched once (page address mechanism).

Figure 4-4 shows a typical basic OTP memory programming cycle with a following OTP memory read operation. In this example A0-A14 of the read operation are identical to A8-A14 of the preceeding programming operation.

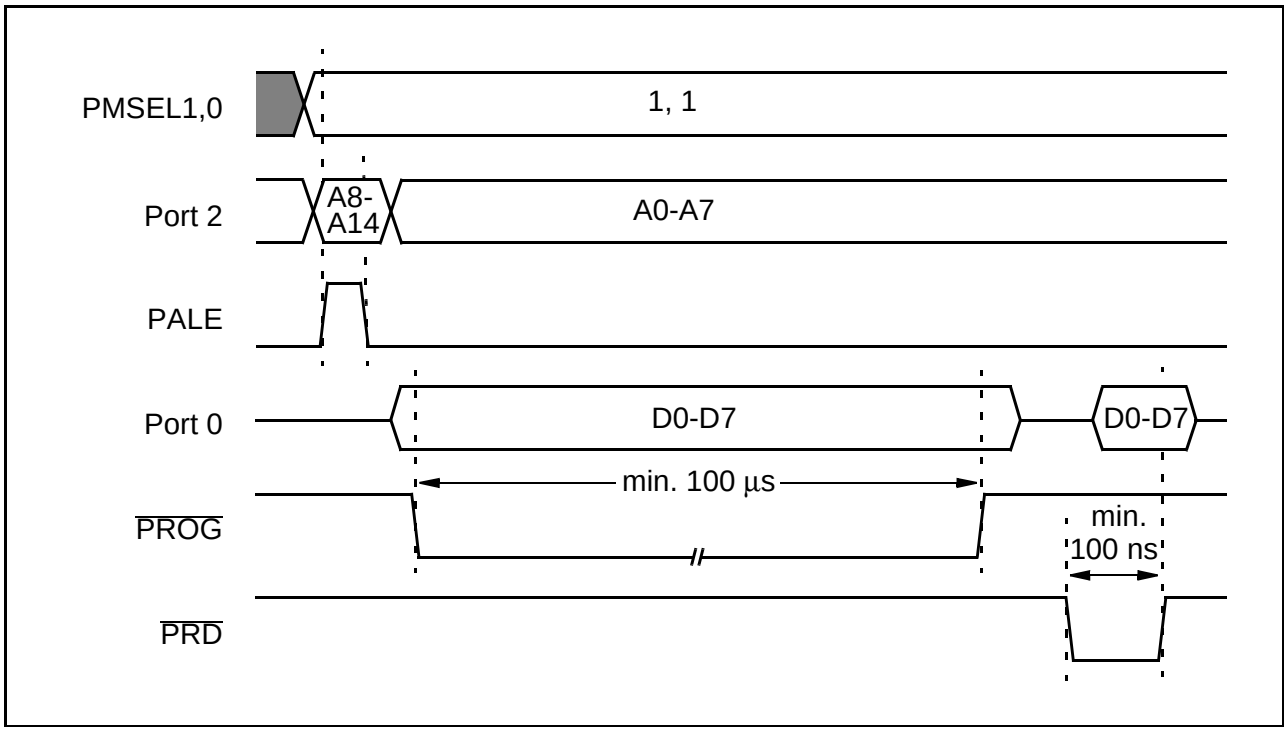


Figure 4-4
Programming / Verify OTP Memory Access Waveform

If the address lines A8-A14 must be updated, PALE must be activated for the latching of the new A8-A14 value. Control, address, and data information must only be switched when the $\overline{\text{PROG}}$ and $\overline{\text{PRD}}$ signals are at high level. The PALE high pulse must always be executed if a different access mode has been used prior to the actual access mode.

Figure 4-5 shows a waveform example of the program/read mode access for several OTP memory bytes. In this example OTP memory locations $3FD_H$ to 400_H are programmed. Thereafter, OTP memory locations 400_H and $3FD_H$ are read.

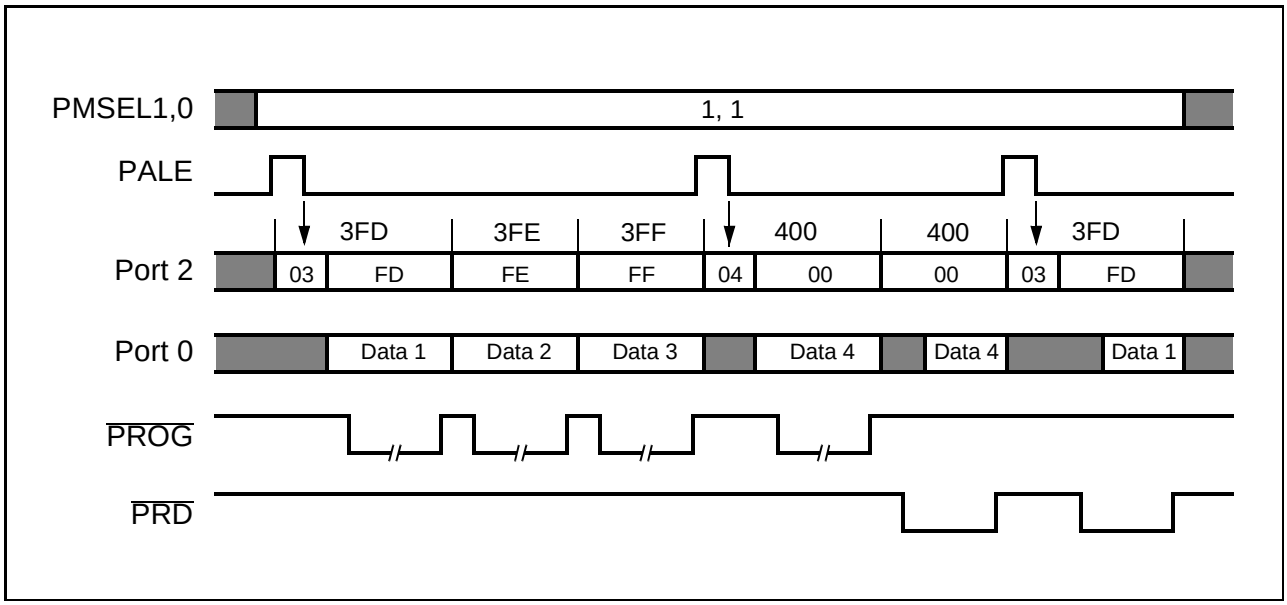


Figure 4-5
Typical OTP Memory Programming/Verify Access Waveform

4.6 Lock Bits Programming / Read

The C505A-4E has two programmable lock bits which, when programmed according **table 4-3**, provide four levels of protection for the on-chip OTP code memory.

Table 4-3
Lock Bit Protection Types

Lock Bits at D1,D0		Protection Level	Protection Type
D1	**D0**		
1	1	Level 0	The OTP lock feature is disabled. During normal operation of the C505A-4E, the state of the $\overline{EA}$ pin is not latched on reset.
1	0	Level 1	During normal operation of the C505A-4E, MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset. An OTP memory read operation is only possible according to OTP verification mode. Further programming of the OTP memory is disabled (reprogramming security).
0	1	Level 2	Same as level 1, but also OTP memory read operation using OTP verification mode is disabled.
0	0	Level 3	Same as level 2; but additionally external code execution by setting $\overline{EA}$=low during normal operation of the C505A-4E is no more possible. External code execution, which is initiated by an internal program (e.g. by an internal jump instruction above the OTP memory boundary), is still possible.

Note : A 1 means that the lock bit is unprogrammed. 0 means that lock bit is programmed.

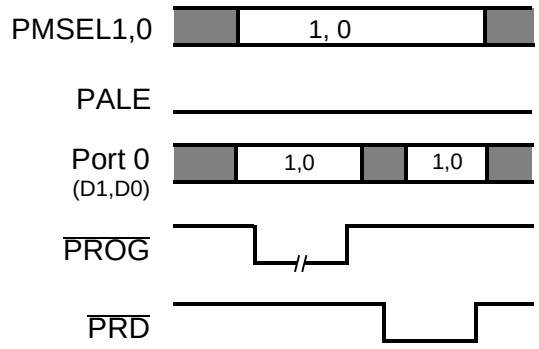
For a OTP verify operation at protection level 1, the C505A-4E must be put into the OTP verification mode.

If a device is programmed with protection level 2 or 3, it is no longer possible to verify the OTP content of a customer rejected (FAR) OTP device.

When a protection level has been activated by programming of the lock bits, the basic programming mode must be left for activation of the protection mechanisms. This means, after the activation of a protection level further OTP program/verify operations are still possible if the basic programming mode is maintained.

The state of the lock bits can always be read if protection level 0 is selected. If protection level 1 to 3 has been programmed and the programming mode has been left, it is not possible to re-enter the programming mode. In this case, the lock bits cannot be read anymore.

Figure 4-6 shows the waveform of a lock bit write/read access. For a simple drawing, the $\overline{PROG}$ pulse is shortened. In reality, for lock bit programming, a 100µs $\overline{PROG}$ low pulse must be applied.



The example shows the programming and reading of a protection level 1.

Figure 4-6
Write/Read Lock Bit Waveform

4.6.1 Access of Version Bytes

The C505A-4E and C505CA-4E provide three version bytes at address locations FC_H, FD_H, and FE_H. The information stored in the version bytes, is defined by the mask of each microcontroller step, Therefore, the version bytes can be read but not written. The three Version Registers hold information as manufacturer code, device type, and stepping code.

For reading of the version bytes the control lines must be used according **table 4-2** and **figure 4-7**. The address of the version byte must be applied at the port 1 address lines. PALE must not be activated.

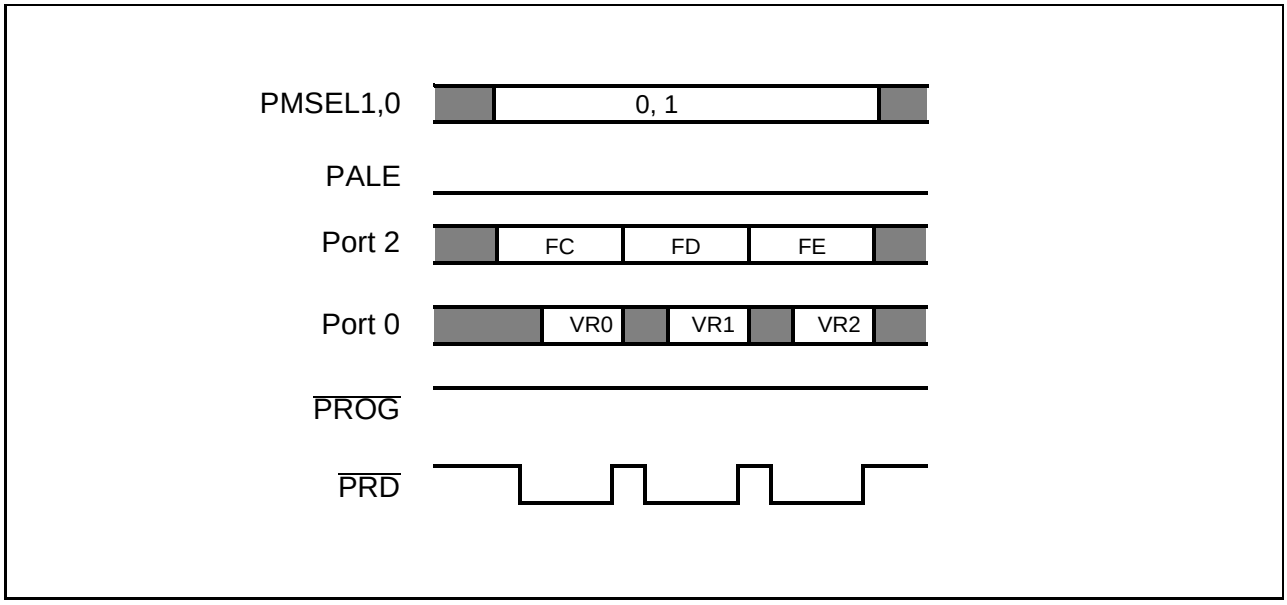


Figure 4-7
Read Version Register(s) Waveform

Version bytes are typically used by programming systems for adapting the programming firmware to specific device characteristics such as OTP size etc.

Note: The 3 version bytes are implemented in a way that they can be also be read during normal program execution mode as a mapped register with bit RMAP in SFR SYSCON set. The addresses of the version bytes in normal mode and programming mode are identical and therefore they are located in the SFR address range.

The steppings of the C505A versions will contain the following version byte information :

Stepping	Version Byte 0 = VR0 (mapped addr. FC_H)	Version Byte 1 = VR1 (mapped addr. FD_H)	Version Byte 2 = VR2 (mapped addr. FE_H)
ES-AA Steps of C505A-4E and C505CA-4E	$C5_H$	05_H	11_H

Note:

Future steppings of C505A would have a different version byte 2 content.

4.7 OTP Verification Mode

The OTP verification mode as shown in **figure 4-8** is used to verify the contents of the OTP when the protection level 1 has been set. The detailed timing characteristics of the OTP verification mode are shown in the AC specifications (chapter 5).

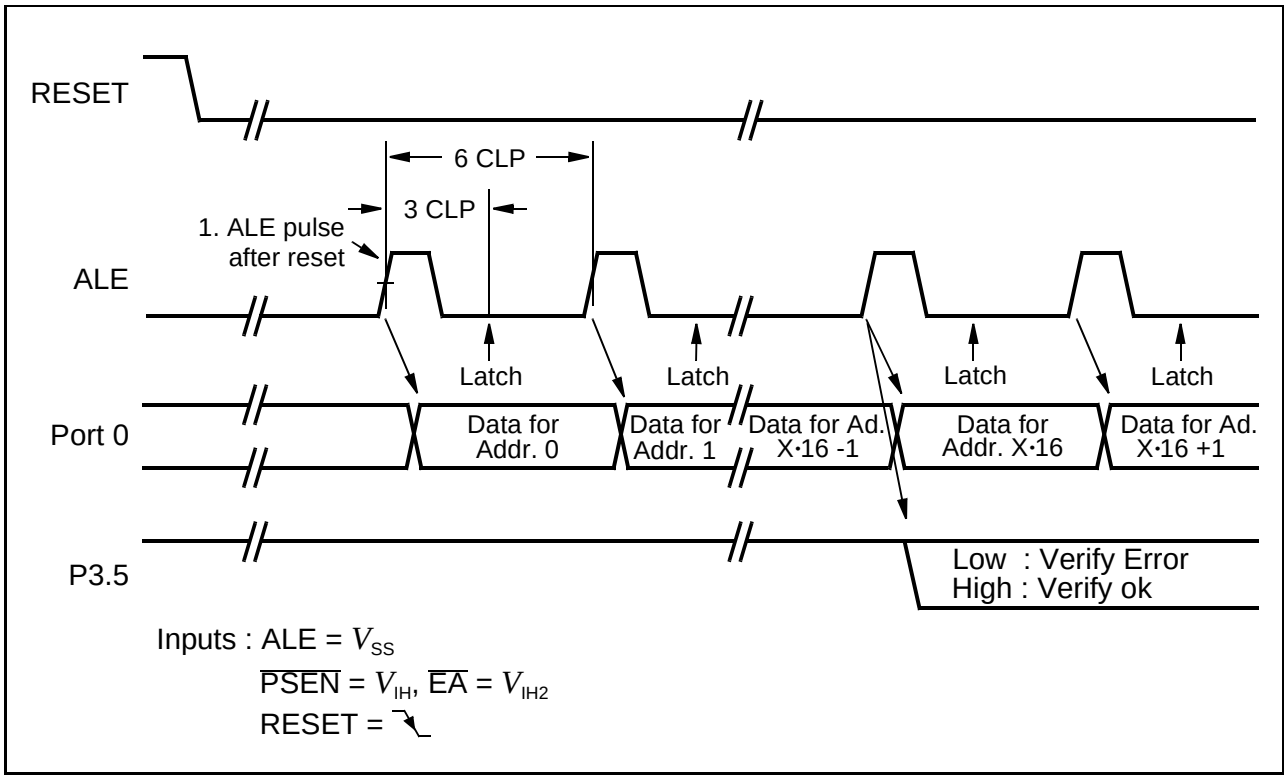


Figure 4-8
OTP Verification Mode

OTP verification mode is selected if the inputs $\overline{PSEN}$, $\overline{EA}$, and ALE are put to the specified logic levels. With RESET going inactive, the OTP verification mode sequence is started. The C505A-4E outputs an ALE signal with a period of 3 CLP and expects data bytes at port 0. The data bytes at port 0 are assigned to the OTP addresses in the following way :

1. Data Byte = content of OTP address 0000_H
2. Data Byte = content of OTP address 0001_H
3. Data Byte = content of OTP address 0002_H
:
16. Data Byte = content of OTP address $000F_H$
:

The C505A-4E does not output any address information during the OTP verification mode. The first data byte to be verified is always the byte which is assigned to the OTP address 0000_H and must be put onto the data bus with the falling edge of RESET. With each following ALE pulse the OTP address pointer is internally incremented and the expected data byte for the next OTP address must be delivered externally.
Between two ALE pulses the data at port 0 is latched (at 3 CLP after ALE rising edge) and compared internally with the OTP content of the actual address. If a verify error is detected, the error condition

is stored internally. After each 16th data byte the cumulated verify result (pass or fail) of the last 16 verify operations is output at P3.5. This means that P3.5 stays at static level (low for fail and high for pass) during the time when the following 16 bytes are checked. In OTP verification mode, the C505A-4E must be provided with a system clock at the XTAL pins.

Figure 4-9 shows an application example of an external circuitry which allows to verify the OTP, with protection level 1, inside the C505A-4E in the OTP verification mode. With RESET going inactive, the C505A-4E starts the OTP verify sequence. Its ALE is clocking a 15-bit address counter. This counter generates the addresses for an external EPROM which is programmed with the contents of the OTP. The verify detect logic typically displays the pass/fail information of the verify operation. P3.5 can be latched with the falling edge of ALE.

When the last byte of the OTP has been handled, the C505A-4E starts generating a $\overline{\text{PSEN}}$ signal. This signal or the CY signal of the address counter indicate to the verify detect logic the end of the OTP verification.

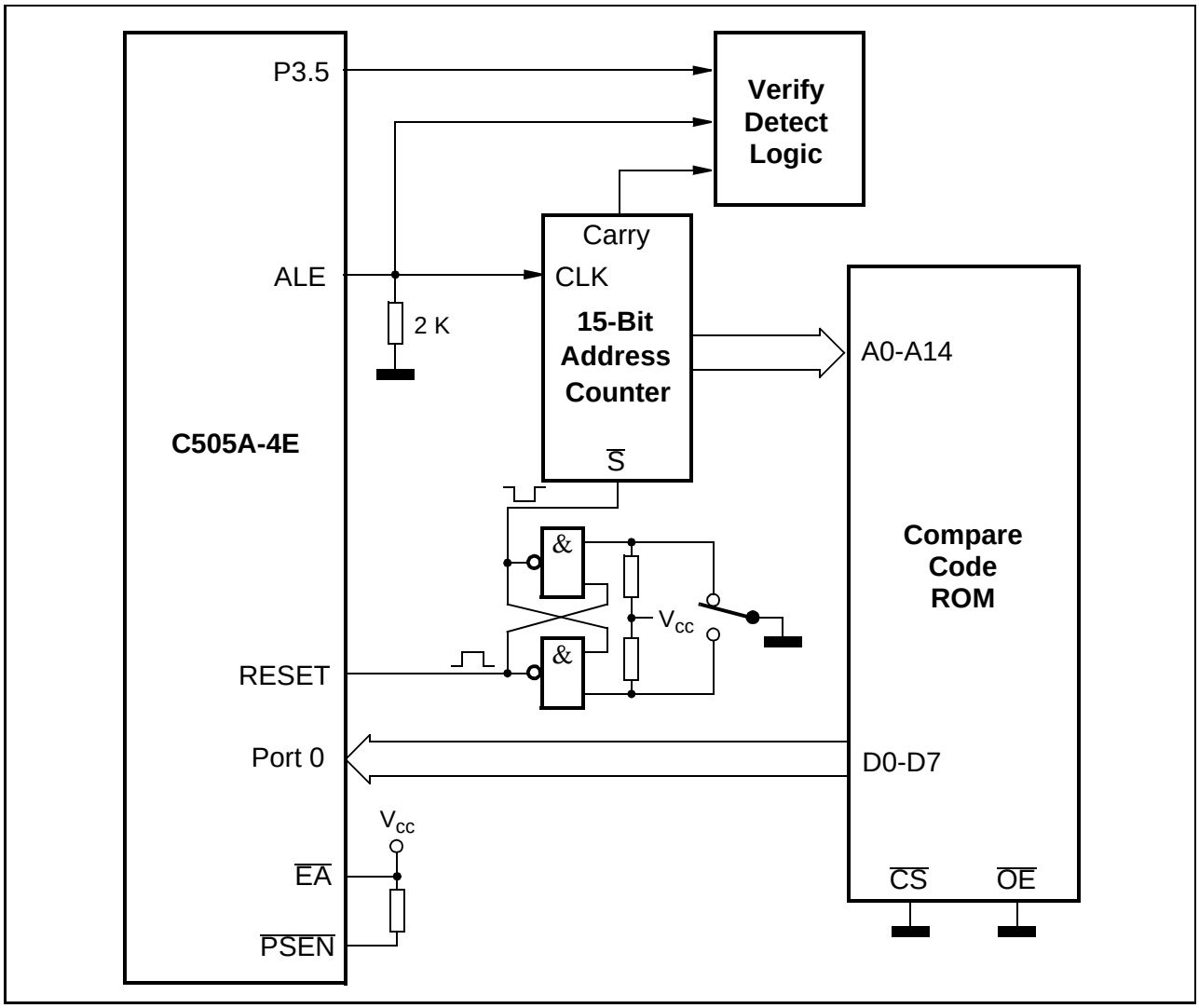


Figure 4-9
OTP Verification Mode - External Circuitry Example

5 Device Specifications

5.1 Absolute Maximum Ratings

Ambient temperature under bias (T_A) ..... – 40 °C to + 125 °C
Storage temperature (T_{ST}).....– 65 °C to + 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS}) .....– 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}).....– 0.5 V to V_{CC} + 0.5 V
Input current on any pin during overload condition.....– 10 mA to + 10 mA
Absolute sum of all input currents during overload condition .....| 100 mA |
Power dissipation.....TBD

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

5.2 DC Characteristics

V_{CC} = 5V +10%, -15%; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB- versions
T_A = -40 to 85 °C for the SAF- versions
T_A = -40 to 110 °C for the SAH- versions
T_A = -40 to 125 °C for the SAK- versions

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltages					
all except $\overline{EA}$, RESET	V_{IL}	– 0.5	0.2 V_{CC} - 0.1	V	–
$\overline{EA}$ pin	V_{IL1}	– 0.5	0.2 V_{CC} - 0.3	V	–
RESET pin	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltages					
all except XTAL1, RESET	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
XTAL1 pin	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
RESET pin	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltages					
Ports 1, 2, 3, 4	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Port 0, ALE, $\overline{PSEN}$	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltages					
Ports 1, 2, 3, 4	V_{OH}	2.4	–	V	I_{OH} = – 80 µA
		0.9 V_{CC}	–	V	I_{OH} = – 10 µA
Port 0 in external bus mode,	V_{OH2}	2.4	–	V	I_{OH} = – 800 µA
ALE, $\overline{PSEN}$		0.9 V_{CC}	–	V	I_{OH} = – 80 µA [2]
Logic 0 input current					
Ports 1, 2, 3, 4	I_{IL}	– 10	– 70	µA	V_{IN} = 0.45 V
Logical 0-to-1 transition current Ports 1, 2, 3, 4	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current					
Port 0, AN0-7 (Port 1), $\overline{EA}$	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	–	10	pF	f_c = 1 MHz, T_A = 25 °C
Overload current	I_{OV}	–	± 5	mA	[3] [4]
Programming voltage	V_{PP}	10.9	12.1	V	11.5 V ± 5% [5]
Supply current at $\overline{EA}$/V_{CC}			30	mA	[5]

Notes see next page

Power Supply Current

Parameter			Symbol	Limit Values		Unit	Test Condition
				typ. [11]	max.[12]		
C505A	Active Mode	12 MHz 20 MHz	I_{CC} I_{CC}	TBD TBD	TBD TBD	mA	[6]
	Idle Mode	12 MHz 20 MHz	I_{CC} I_{CC}	TBD TBD	TBD TBD	mA	[7]
	Active Mode with slow-down enabled	12 MHz 20 MHz	I_{CC} I_{CC}	TBD TBD	TBD TBD	mA	[8]
	Idle Mode with slow-down enabled	12 MHz 20 MHz	I_{CC} I_{CC}	TBD TBD	TBD TBD	mA	[9]
	Power down current		I_{PD}	TBD	60	µA	V_{CC} = 2..5.5 V [10]

Notes :

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) Overload conditions occur if the standard operating conditions are exceeded, ie. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{CC}$ + 0.5 V or $V_{OV} < V_{SS}$ - 0.5 V). The supply voltage V_{CC} and V_{SS} must remain within the specified limits. The absolute sum of input currents on all port pins may not exceed 50 mA.

4) Not 100% tested, guaranteed by design characterization.

5) Only valid in porgramming mode.

6) I_{CC} (active mode) is measured with:
XTAL1 driven with t_R /t_F = 5 ns, 50% duty cycle , $V_{IL} = V_{SS}$ + 0.5 V, $V_{IH} = V_{CC}$ – 0.5 V; XTAL2 = N.C.;
EA = Port0 = RESET =V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (approx. 1 mA)

7) I_{CC} (idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_R/t_F = 5 ns, 50% duty cycle, $V_{IL} = V_{SS}$ + 0.5 V, $V_{IH} = V_{CC}$ – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS} ; Port0 = V_{CC} ; all other pins are disconnected;

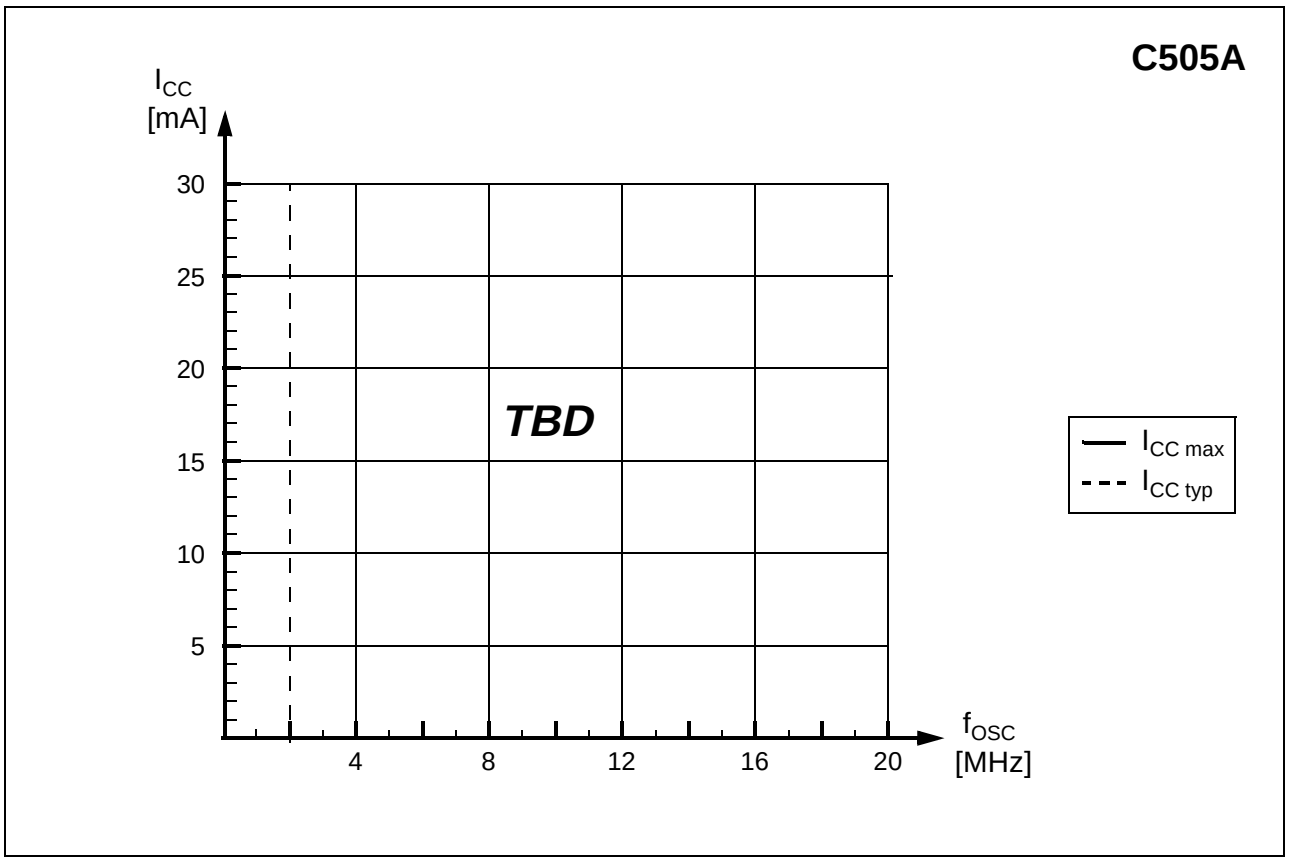
8) I_{CC} (active mode with slow-down mode) is measured : TBD

9) I_{CC} (idle mode with slow-down mode) is measured : TBD

10) I_{PD} (power-down mode) is measured under following conditions:
$\overline{EA}$ = Port 0 = V_{CC}; RESET =V_{SS}; XTAL2 = N.C.; XTAL1 = V_{CC}; $V_{AGND} = V_{SS}$; $V_{AREF} = V_{CC}$;
all other pins are disconnected.

11) The typical I_{CC} values are periodically measured at T_A = +25 °C but not 100% tested.

12) The maximum I_{CC} values are measured under worst case conditions (T_A = 0 °C or -40 °C and V_{CC} = 5.5 V)



ICC Diagram

C505A : Power Supply Current Calculation Formulas

Parameter	Symbol	Formula
Active mode	$I_{CC\ typ}$ $I_{CC\ max}$	TBD TBD
Idle mode	$I_{CC\ typ}$ $I_{CC\ max}$	TBD TBD
Active mode with slow-down enabled	$I_{CC\ typ}$ $I_{CC\ max}$	TBD TBD
Idle mode with slow-down enabled	$I_{CC\ typ}$ $I_{CC\ max}$	TBD TBD

Note : f_{osc} is the oscillator frequency in MHz. I_{CC} values are given in mA.

5.3 A/D Converter Characteristics

V_{CC} = 5 V + 10%, – 15%; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB-C505A versions
T_A = – 40 to 85 °C for the SAF-C505A versions
T_A = – 40 to 110 °C for the SAH-C505A versions
T_A = – 40 to 125 °C for the SAK-C505A versions

4 $V \le V_{AREF} \le V_{CC}$ + 0.1 V; V_{SS} – 0.1 V ≤ V_{AGND} ≤ Vss + 0.2 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	1)
Sample time	t_S	–	64 x t_{IN} 32 x t_{IN} 16 x t_{IN} 8 x t_{IN}	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 2)
Conversion cycle time	t_{ADCC}	–	384 x t_{IN} 192 x t_{IN} 96 x t_{IN} 48 x t_{IN}	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 3)
Total unadjusted error	T_{UE}	–	± 2	LSB	V_{SS}+0.5V ≤ V_{AIN} ≤ V_{CC}-0.5V 4)
		–	± 4	LSB	V_{SS} < V_{AIN} < V_{CC}+0.5V V_{CC} - 0.5 V < V_{AIN} < V_{CC} 4)
Internal resistance of reference voltage source	R_{AREF}	–	t_{ADC} / 250 - 0.25	kΩ	t_{ADC} in [ns] 5) 6)
Internal resistance of analog source	R_{ASRC}	–	t_S / 500 - 0.25	kΩ	t_S in [ns] 2) 6)
ADC input capacitance	C_{AIN}	–	50	pF	6)

Notes see next page.

Clock calculation table :

Clock Prescaler Ratio	ADCL1, 0		t_{ADC}	t_S	t_{ADCC}
÷ 32	1	1	32 x t_{IN}	64 x t_{IN}	384 x t_{IN}
÷ 16	1	0	16 x t_{IN}	32 x t_{IN}	192 x t_{IN}
÷ 8	0	1	8 x t_{IN}	16 x t_{IN}	96 x t_{IN}
÷ 4	0	0	4 x t_{IN}	8 x t_{IN}	48 x t_{IN}

Further timing conditions : t_{ADC} min = 500 ns
$t_{IN} = 1 / f_{OSC} = t_{CLP}$

Notes:

1) V_{AIN} may exeed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2) During the sample time the input capacitance C_{AIN} must be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result and the time for the calibration. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.

4) T_{UE} is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{CC} = 4.9 V. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 unused analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100% tested, but guaranteed by design characterization.

5.4 AC Characteristics (12 MHz, 0.5 Duty Cycle)

V_{CC} = 5V +10%, -15%; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB-C505A versions
T_A = -40 to 85 °C for the SAF-C505A versions
T_A = -40 to 110 °C for the SAH-C505A versions
T_A = -40 to 125 °C for the SAK-C505A versions

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz clock 0.5 Duty Cycle		Variable Clock 1/CLP = 2 MHz to 12 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	43	–	CLP - 40	–	ns
Address setup to ALE	t_{AVLL}	17	–	CLP/2 - 25	–	ns
Address hold after ALE	t_{LLAX}	17	–	CLP/2 - 25	–	ns
ALE to valid instruction in	t_{LLIV}	–	80	–	2 CLP - 87	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	22	–	CLP/2 - 20	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	95	–	3/2 CLP - 30	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	t_{PLIV}	–	60	–	3/2 CLP - 65	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	32	–	CLP/2 - 10	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	37	–	CLP/2 - 5	–	ns
Address to valid instruction in	t_{AVIV}	–	148	–	5/2 CLP - 60	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the C505A to devices with float times up to 37 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (12 MHz, 0.5 Duty Cycle, cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz clock 0.5 Duty Cycle		Variable Clock 1/CLP = 2 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	180	–	3 CLP - 70	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	180	–	3 CLP - 70	–	ns
Address hold after ALE	t_{LLAX2}	56	–	CLP - 27	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	118	–	5/2 CLP- 90	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	63	–	CLP - 20	ns
ALE to valid data in	t_{LLDV}	–	200	–	4 CLP - 133	ns
Address to valid data in	t_{AVDV}	–	220	–	9/2 CLP - 155	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	75	175	3/2 CLP - 50	3/2 CLP + 50	ns
Address valid to $\overline{WR}$	t_{AVWL}	70	–	2 CLP - 97	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	17	67	CLP/2 - 25	CLP/2 + 25	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	CLP/2 - 37	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	170	–	7/2 CLP - 122	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	15	–	CLP/2 - 27	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 2 MHz to 12 MHz		
		min.	max.	
Oscillator period	CLP	83.3	500	ns
High time	TCL_H	20	CLP-TCL_L	ns
Low time	TCL_L	20	CLP-TCL_H	ns
Rise time	t_R	–	12	ns
Fall time	t_F	–	12	ns
Oscillator duty cycle	DC	0.5	0.5	–

5.5 AC Characteristics (16 MHz, 0.4 to 0.6 Duty Cycle)

V_{CC} = 5V +10%, -15%; V_{SS} = 0 V T_A = 0 to 70 °C for the SAB-C505A versions
T_A = -40 to 85 °C for the SAF-C505A versions

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		16-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP= 2 MHz to 16 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	48	–	CLP - 15	–	ns
Address setup to ALE	t_{AVLL}	10	–	TCL_{Hmin} -15	–	ns
Address hold after ALE	t_{LLAX}	10	–	TCL_{Hmin} -15	–	ns
ALE to valid instruction in	t_{LLIV}	–	75	–	2 CLP - 50	ns
ALE to $\overline{PSEN}$	t_{LLPL}	10	–	TCL_{Lmin} -15	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	73	–	CLP+ TCL_{Hmin} -15	–	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	–	38	–	CLP+ TCL_{Hmin}- 50	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} *)	–	15	–	TCL_{Lmin} -10	ns
Address valid after $\overline{PSEN}$	t_{PXAV} *)	20	–	TCL_{Lmin} - 5	–	ns
Address to valid instruction in	t_{AVIV}	–	95	–	2 CLP + TCL_{Hmin} -55	ns
Address float to $\overline{PSEN}$	t_{AZPL}	-5	–	-5	–	ns

*) Interfacing the C505A to devices with float times up to 20 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (16 MHz, 0.4 to 0.6 Duty Cycle, cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		16-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP= 2 MHz to 16 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	158	–	3 CLP - 30	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	158	–	3 CLP - 30	–	ns
Address hold after ALE	t_{LLAX2}	48	–	CLP - 15	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	100	–	2 CLP+ TCL_{Hmin} - 50	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	51	–	CLP - 12	ns
ALE to valid data in	t_{LLDV}	–	200	–	4 CLP - 50	ns
Address to valid data in	t_{AVDV}	–	200	–	4 CLP + TCL_{Hmin} -75	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	73	103	CLP + TCL_{Lmin} - 15	CLP+ TCL_{Lmin}+ 15	ns
Address valid to $\overline{WR}$	t_{AVWL}	95	–	2 CLP - 30	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	TCL_{Hmin} - 15	TCL_{Hmin} + 15	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	TCL_{Lmin} - 20	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	163	–	3 CLP + TCL_{Lmin} - 50	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	5	–	TCL_{Hmin} - 20	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

AC Characteristics (16 MHz, 0.4 to 0.6 Duty Cycle, cont'd)

External Clock Drive Characteristics

Parameter	Symbol	CPU Clock = 16 MHz Duty Cycle 0.4 to 0.6		Variable CPU Clock 1/CLP = 2 to 16 MHz		Unit
		min.	max.	min.	max.	
Oscillator period	CLP	62.5	62.5	62.5	500	ns
High time	TCL_H	25	–	25	CLP - TCL_L	ns
Low time	TCL_L	25	–	25	CLP - TCL_H	ns
Rise time	t_R	–	10	–	10	ns
Fall time	t_F	–	10	–	10	ns
Oscillator duty cycle	DC	0.4	0.6	25 / CLP	1 - 25 / CLP	–
Clock cycle	TCL	25	37.5	CLP * DC_{min}	CLP * DC_{max}	ns

Note: The 16 MHz values in the tables are given as an example for a typical duty cycle variation of the oscillator clock from 0.4 to 0.6.

5.6 AC Characteristics (20 MHz, 0.5 Duty Cycle)

V_{CC} = 5V +10%, -15%; V_{SS} = 0 V T_A = 0 to 70 °C for the SAB-C505A versions
T_A = -40 to 85 °C for the SAF-C505A versions

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		20 MHz clock 0.5 Duty Cycle		Variable Clock 1/CLP = 2 MHz to 20 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	35	–	CLP - 15	–	ns
Address setup to ALE	t_{AVLL}	10	–	CLP/2 - 15	–	ns
Address hold after ALE	t_{LLAX}	10	–	CLP/2 - 15	–	ns
ALE to valid instruction in	t_{LLIV}	–	55	–	2 CLP - 45	ns
ALE to $\overline{PSEN}$	t_{LLPL}	10	–	CLP/2 - 15	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	60	–	3/2 CLP - 15	–	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	–	25	–	3/2 CLP - 50	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} *)	–	20	–	CLP/2 - 5	ns
Address valid after $\overline{PSEN}$	t_{PXAV} *)	20	–	CLP/2 - 5	–	ns
Address to valid instruction in	t_{AVIV}	–	65	–	5/2 CLP - 60	ns
Address float to $\overline{PSEN}$	t_{AZPL}	- 5	–	- 5	–	ns

*) Interfacing the C505A to devices with float times up to 20 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

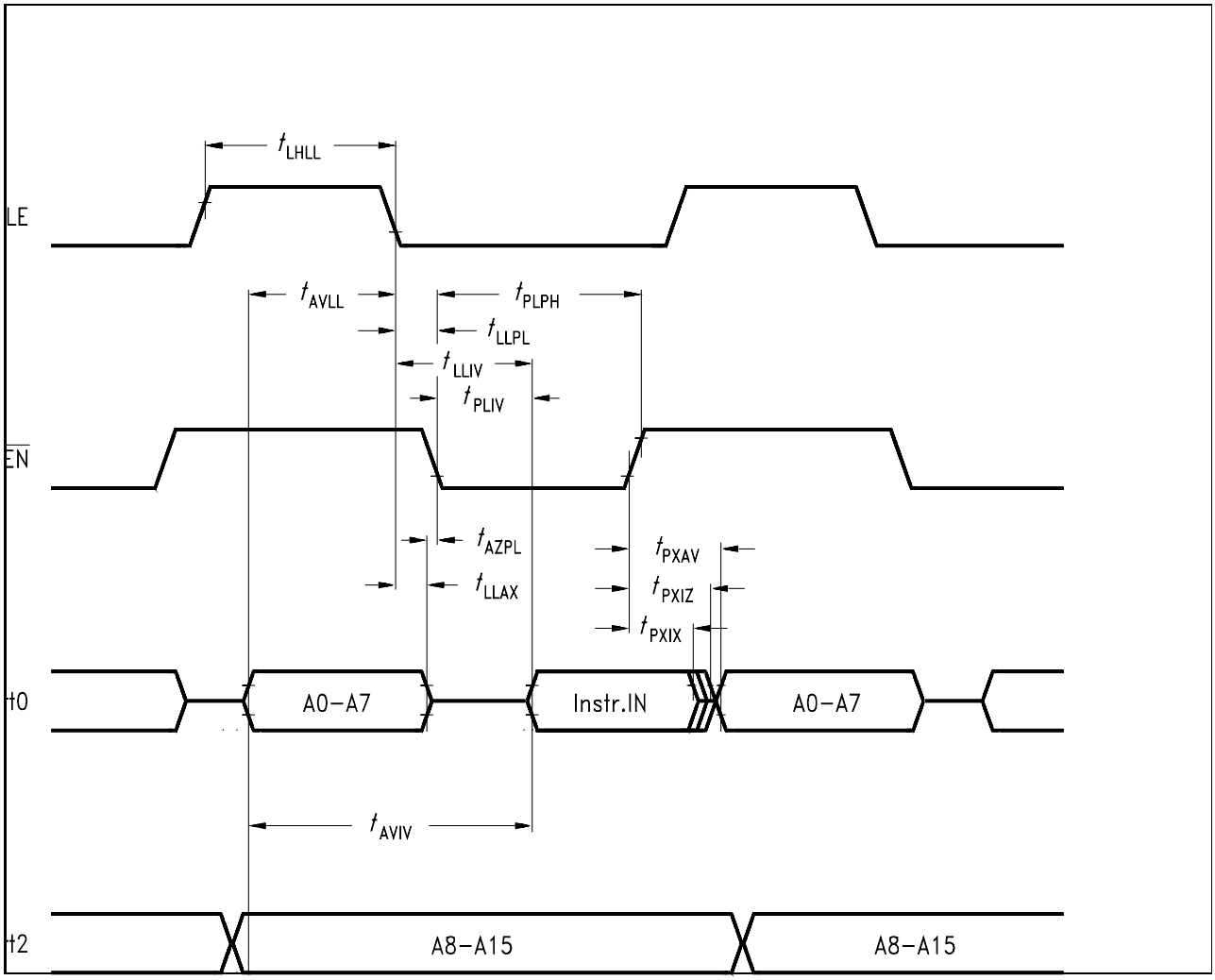
AC Characteristics (20 MHz, 0.5 Duty Cycle, cont'd)

External Data Memory Characteristics

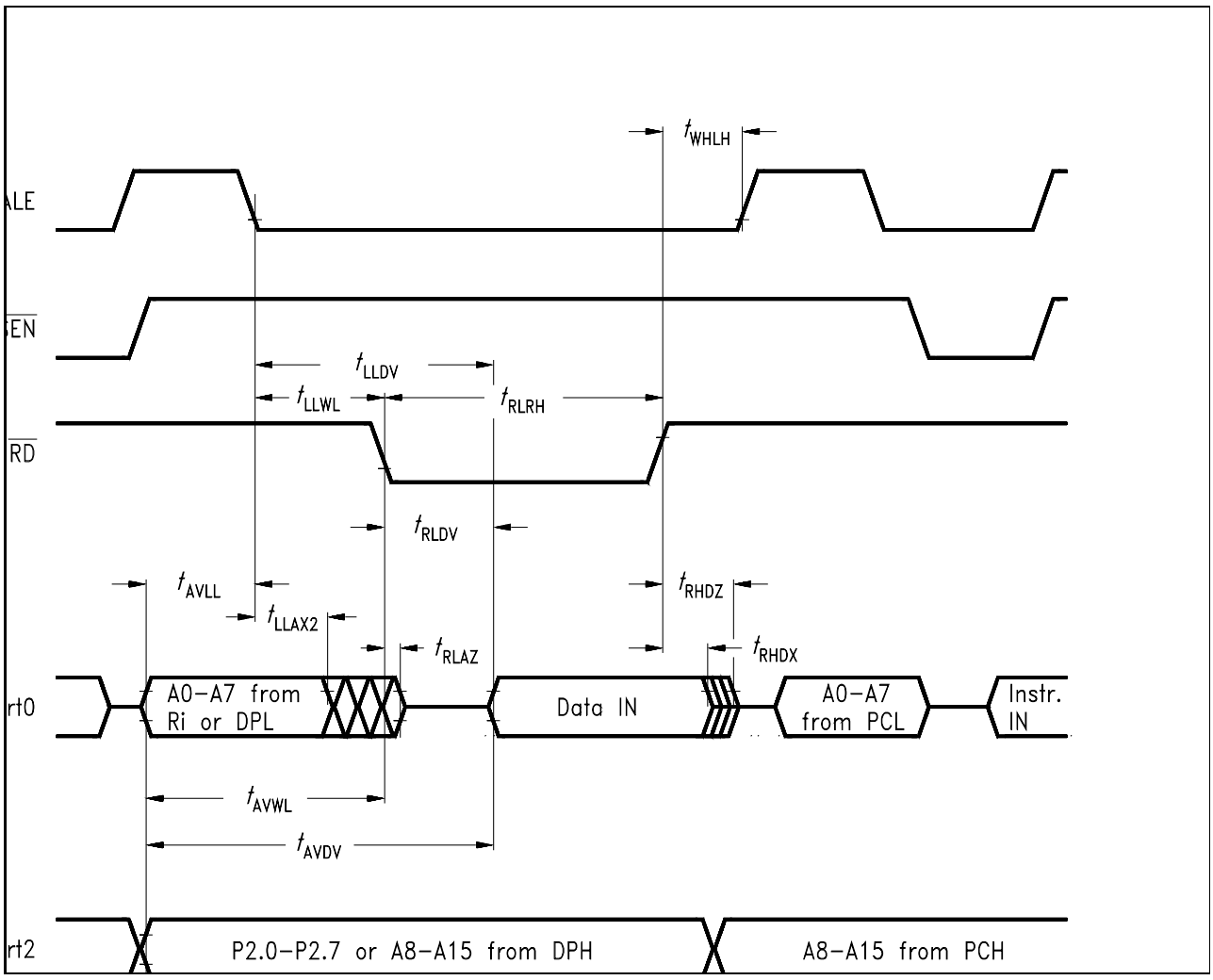
Parameter	Symbol	Limit Values				Unit
		20 MHz clock 0.5 Duty Cycle		Variable Clock 1/CLP = 2 MHz to 20 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	120	–	3 CLP - 30	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	120	–	3 CLP - 30	–	ns
Address hold after ALE	t_{LLAX2}	35	–	CLP - 15	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	75	–	5/2 CLP- 50	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	38	–	CLP - 12	ns
ALE to valid data in	t_{LLDV}	–	150	–	4 CLP - 50	ns
Address to valid data in	t_{AVDV}	–	150	–	9/2 CLP - 75	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	60	90	3/2 CLP - 15	3/2 CLP + 15	ns
Address valid to $\overline{WR}$	t_{AVWL}	70	–	2 CLP - 30	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	CLP/2 - 15	CLP/2 + 15	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	CLP/2 - 20	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	125	–	7/2 CLP - 50	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	5	–	CLP/2 - 20	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive Characteristics

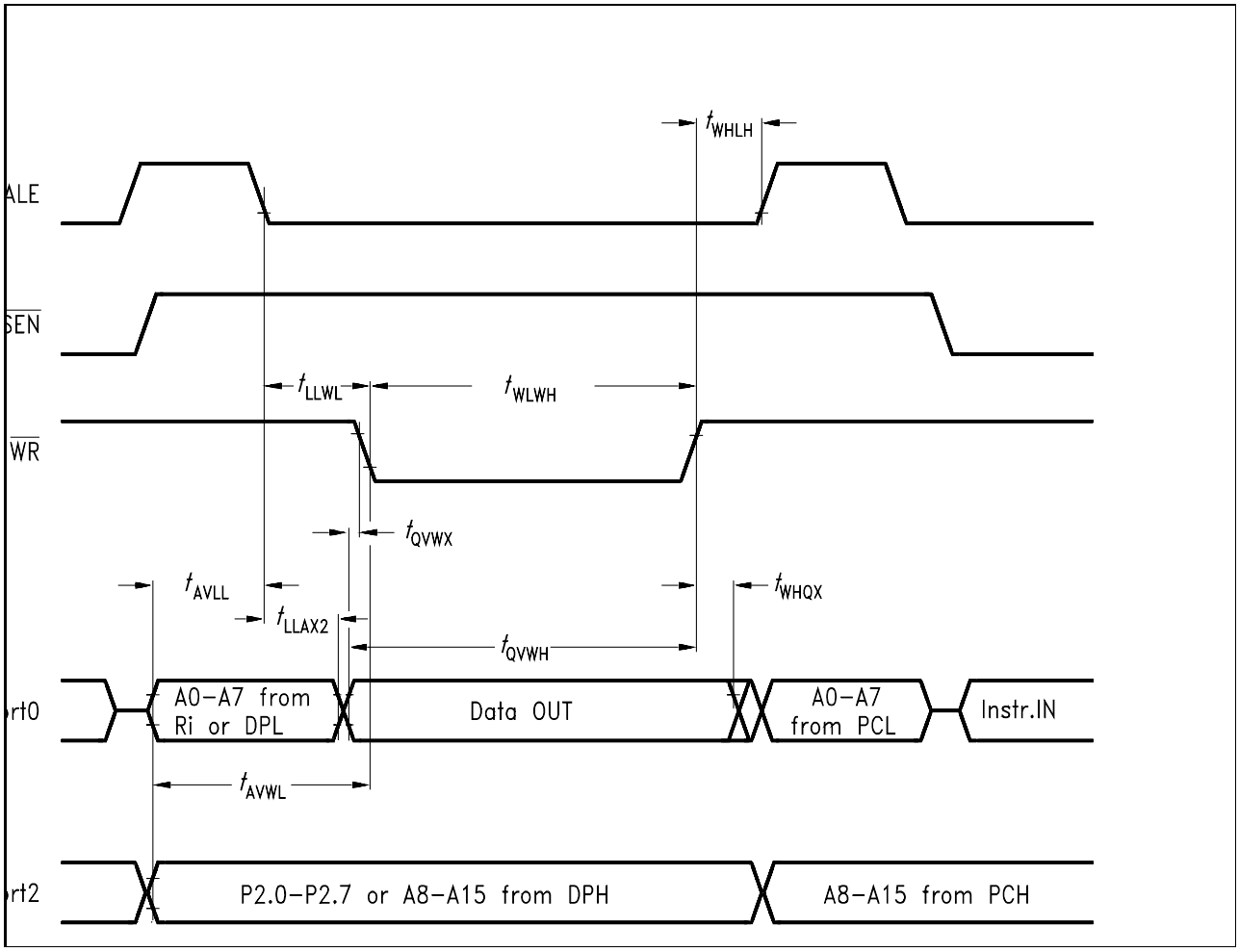
Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 2 MHz to 20 MHz		
		min.	max.	
Oscillator period	CLP	50	500	ns
High time	TCL_H	15	$CLP-TCL_L$	ns
Low time	TCL_L	15	$CLP-TCL_H$	ns
Rise time	t_R	–	10	ns
Fall time	t_F	–	10	ns
Oscillator duty cycle	DC	0.5	0.5	–



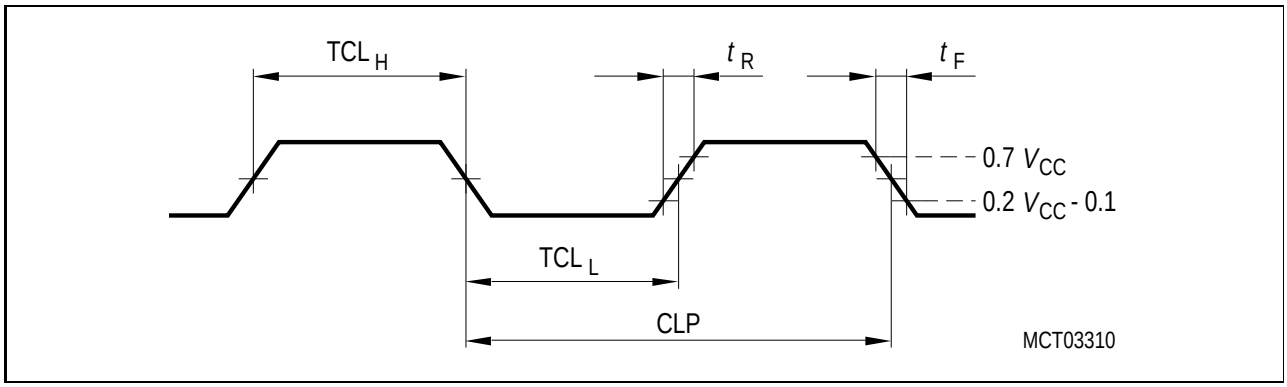
Program Memory Read Cycle



Data Memory Read Cycle



Data Memory Write Cycle



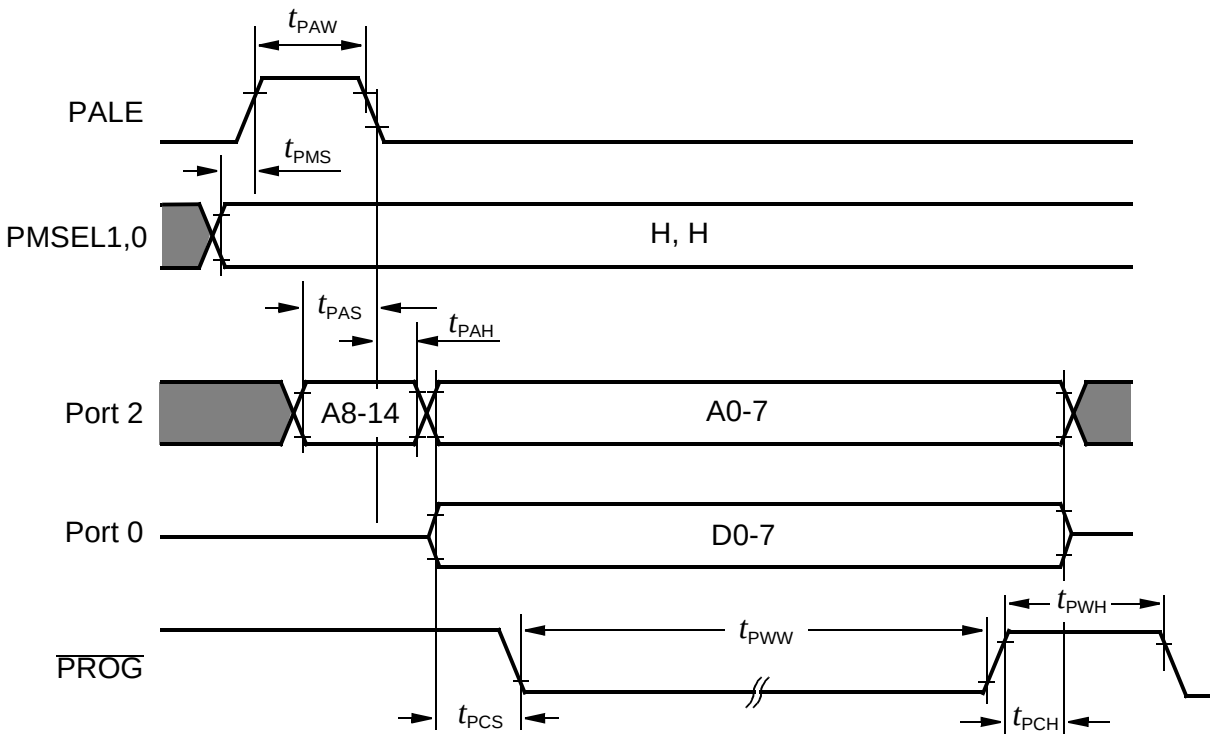
External Clock Drive on XTAL1

5.7 OTP Memory Characteristics

5.7.1 Programming Mode Timing Characteristics

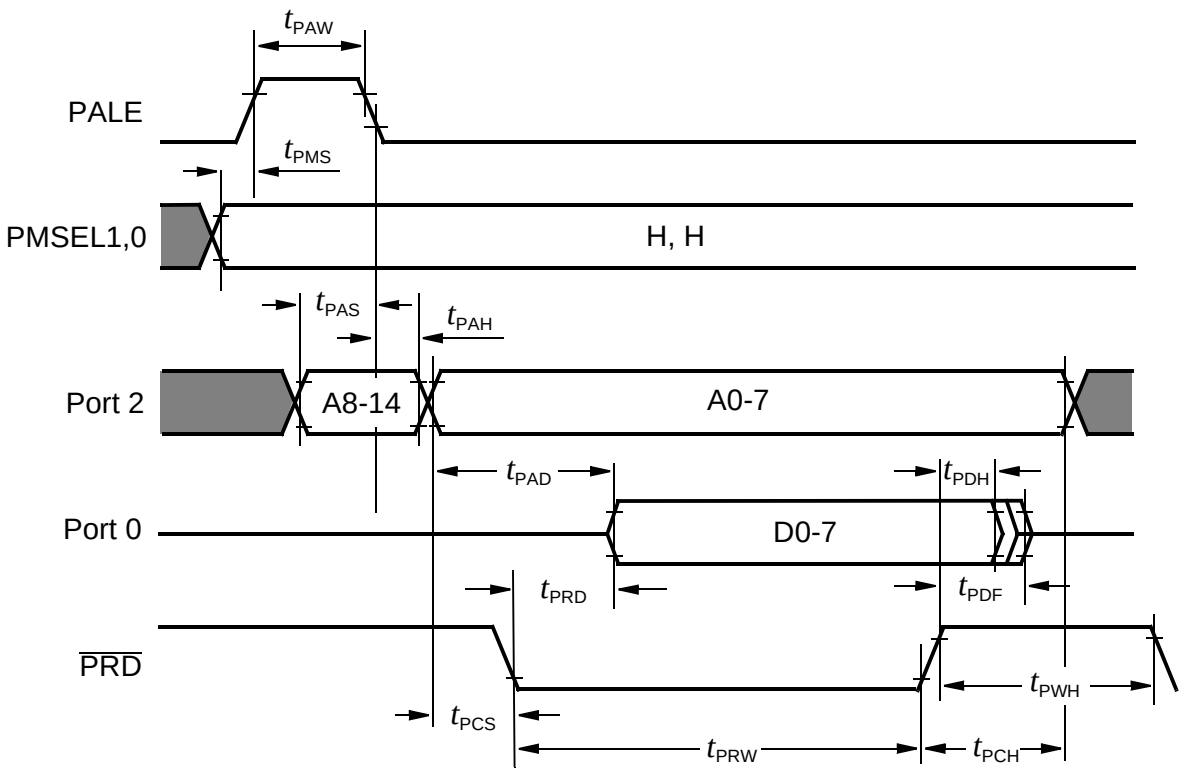
V_{CC} = 5 V ± 10 %; V_{PP} = 11.5 V ± 5 %; T_A = 25 °C ± 10 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
PALE pulse width	t_{PAW}	35	–	ns
PMSEL setup to PALE rising edge	t_{PMS}	10	–	
Address setup to PALE, $\overline{PROG}$, or $\overline{PRD}$ falling edge	t_{PAS}	10	–	ns
Address hold after PALE, $\overline{PROG}$, or $\overline{PRD}$ falling edge	t_{PAH}	10	–	ns
Address, data setup to $\overline{PROG}$ or $\overline{PRD}$	t_{PCS}	100	–	ns
Address, data hold after $\overline{PROG}$ or $\overline{PRD}$	t_{PCH}	0	–	ns
PMSEL setup to $\overline{PROG}$ or $\overline{PRD}$	t_{PMS}	10	–	ns
PMSEL hold after $\overline{PROG}$ or $\overline{PRD}$	t_{PMH}	10	–	ns
$\overline{PROG}$ pulse width	t_{PWW}	100	–	µs
$\overline{PRD}$ pulse width	t_{PRW}	100	–	ns
Address to valid data out	t_{PAD}	–	75	ns
$\overline{PRD}$ to valid data out	t_{PRD}	–	20	ns
Data hold after $\overline{PRD}$	t_{PDH}	0	–	ns
Data float after $\overline{PRD}$	t_{PDF}	–	20	ns
$\overline{PROG}$ high between two consecutive $\overline{PROG}$ low pulses	t_{PWH1}	1	–	µs
$\overline{PRD}$ high between two consecutive $\overline{PRD}$ low pulses	t_{PWH2}	100		ns
XTAL clock period	t_{CLKP}	83.3	500	ns



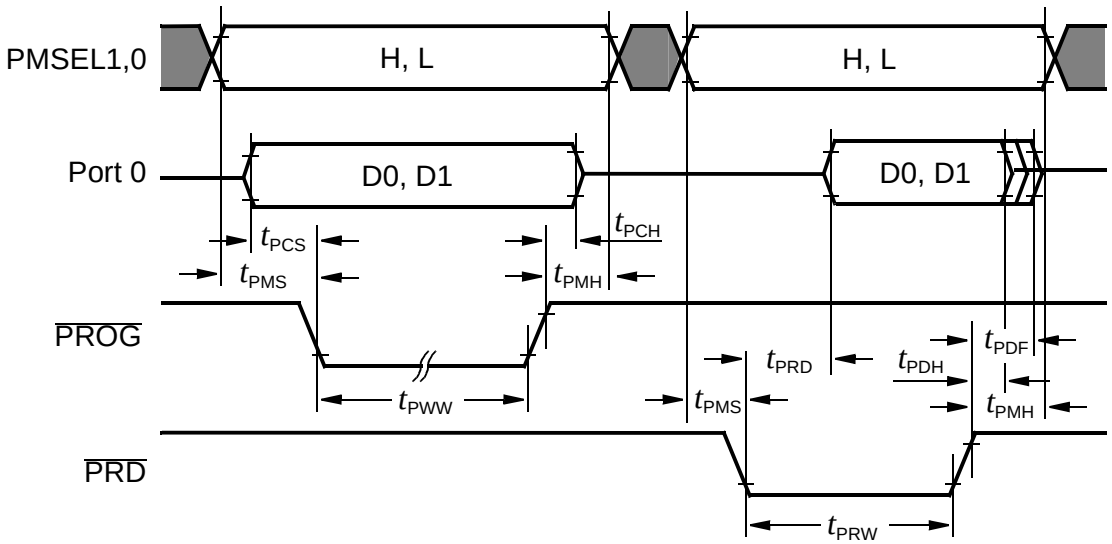
Notes : $\overline{PRD}$ must be high during a programming write cycle

Programming Code Byte - Write Cycle Timing



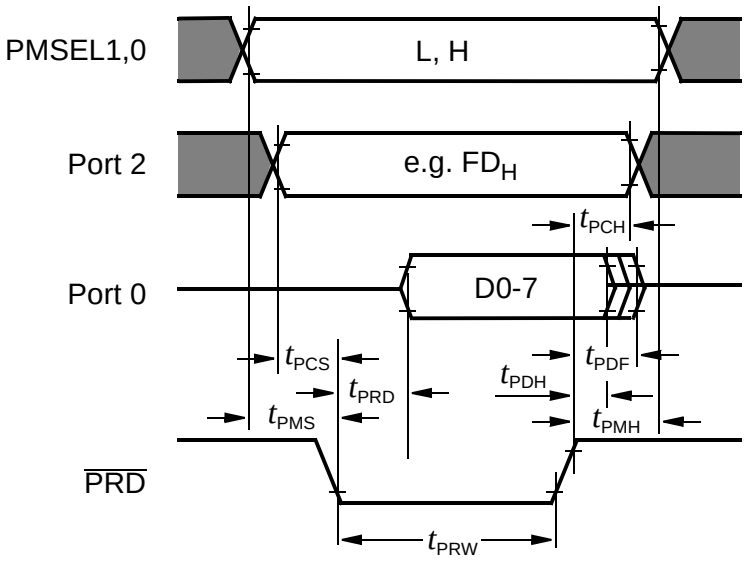
Notes : $\overline{PROG}$ must be high during a programming read cycle

Verify Code Byte - Read Cycle Timing



Note : PALE should be low during a lock bit read/write cycle

Lock Bit Access Timing

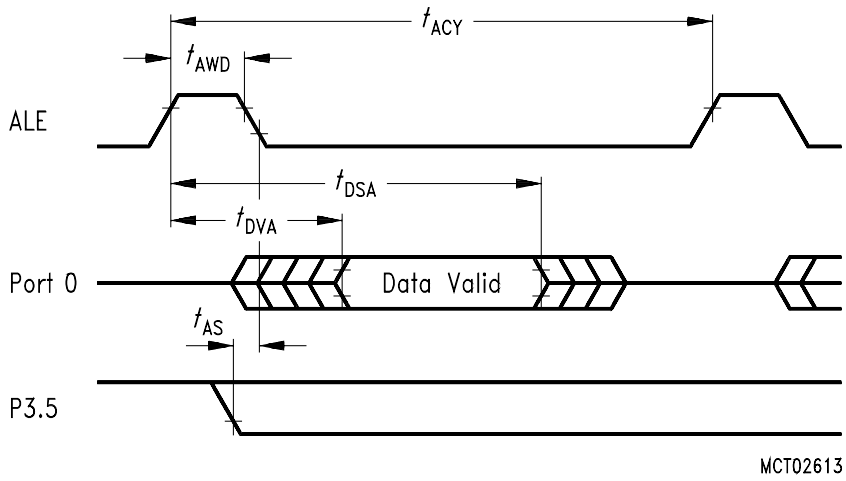


Note : PROG must be high during a programming read cycle

Version Registers - Read Timing

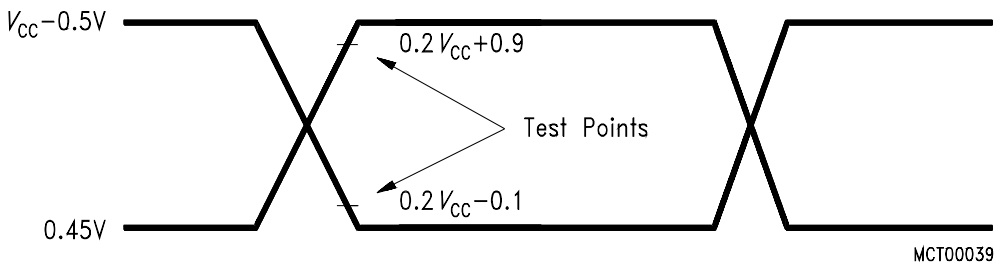
5.7.2 OTP Verification Mode Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ	max.	
ALE pulse width	t_{AWD}	–	CLP	–	ns
ALE period	t_{ACY}	–	6 CLP	–	ns
Data valid after ALE	t_{DVA}	–	–	2 CLP	ns
Data stable after ALE	t_{DSA}	4 CLP	–	–	ns
P3.5 setup to ALE low	t_{AS}	–	TCL_H	–	ns
Oscillator frequency	1/ CLP	4	–	6	MHz



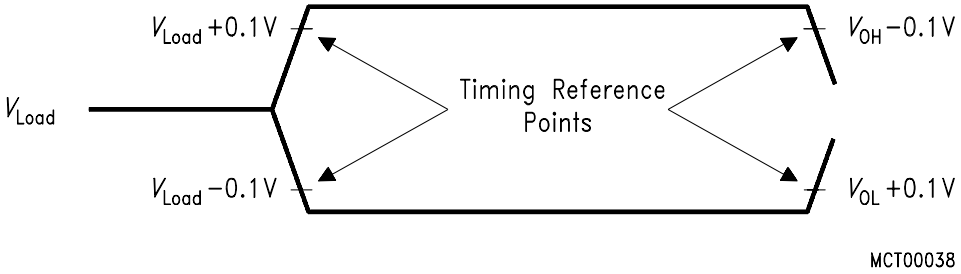
OTP Verification Mode

Note: This mode cannot be entered into if OTP protection levels of 1 to 3 are programmed.



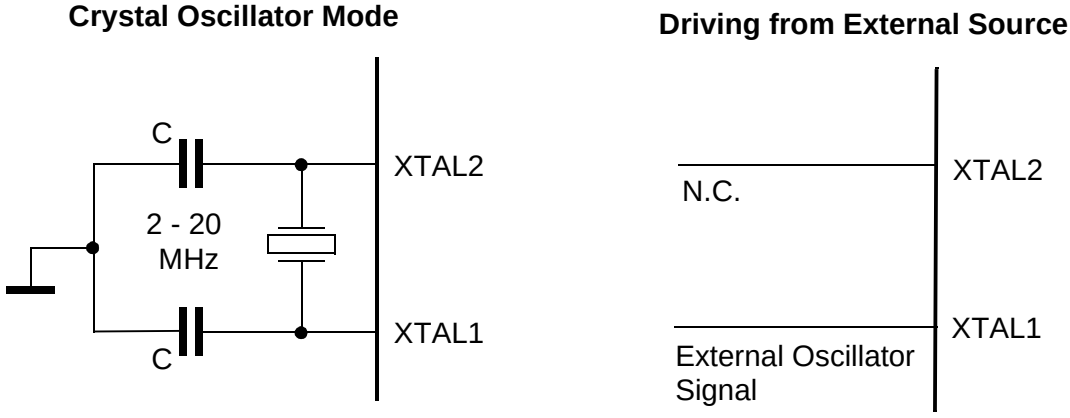
AC Inputs during testing are driven at V_{CC} - 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

AC Testing : Float Waveforms

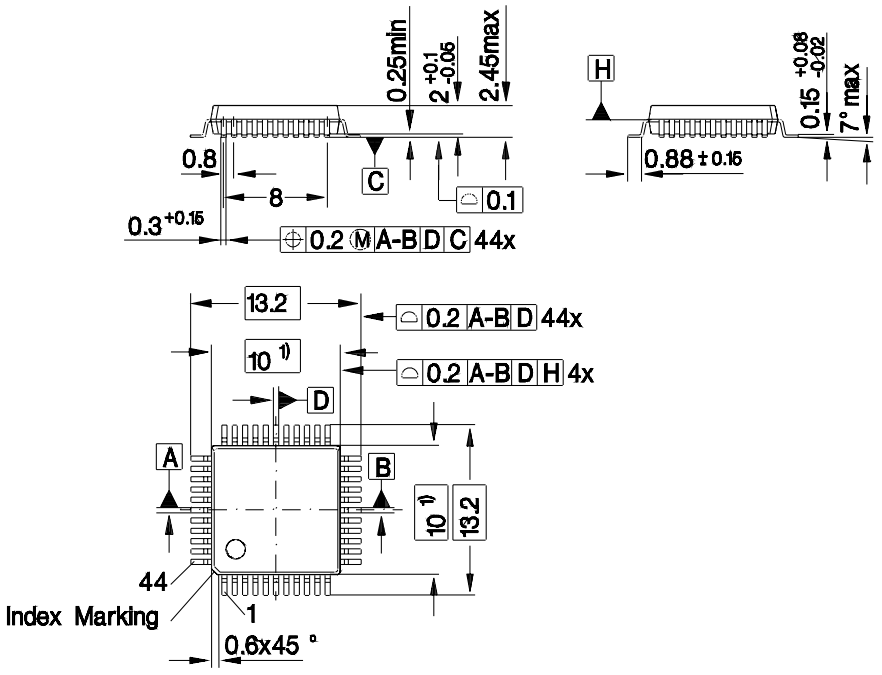


Crystal Mode : C = 20 pF ± 10 pF (incl. stray capacitance)

Recommended Oscillator Circuits for Crystal Oscillator

5.8 Package Information

Plastic Package, P-MQFP-44-2 (SMD)
(Plastic Metric Quad Flat Pack)



Dimensions in mm

P-MQFP-44-2 Outline

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our
Data Book “Package Information”.
SMD = Surface Mounted Device

6 Index

Note: Bold page numbers refer to the main definition part of SFRs or SFR bits.