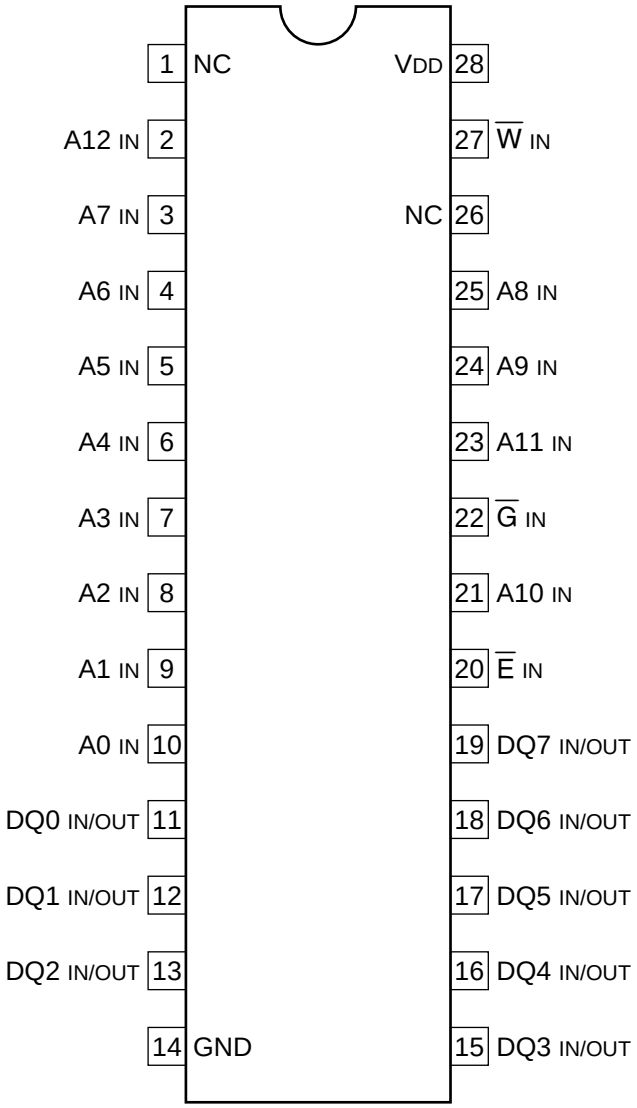
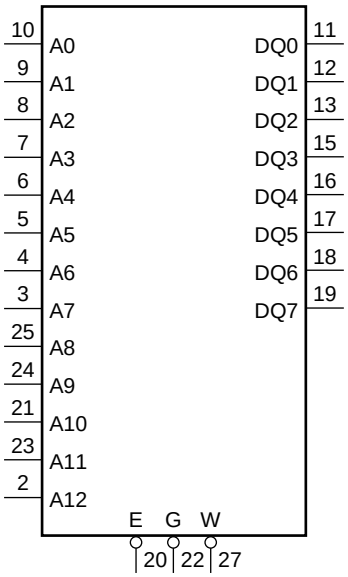
C-MOS 64 K (8 K × 8)-BIT SRAM

—TOP VIEW—

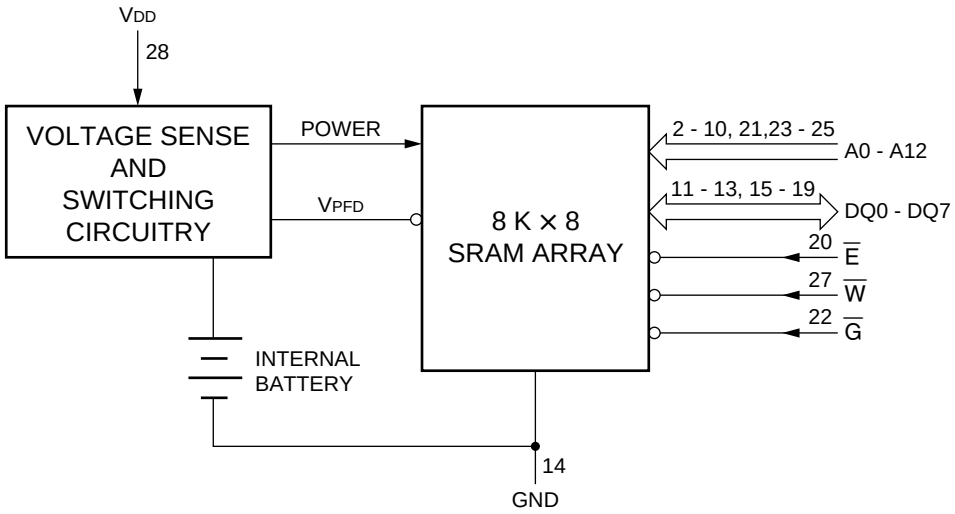




A0 - A12 : ADDRESS INPUTS
DQ0 - DQ7 : DATA INPUTS/OUTPUTS
$\overline{E}$: CHIP ENABLE
$\overline{G}$: OUTPUT ENABLE
$\overline{W}$: WRITE ENABLE

MODE	E	G	W	DQ0 - DQ7	POWER
DESELECT	1	×	×	HI-Z	STANDBY
WRITE	0	×	0	D IN	ACTIVE
READ	0	0	1	D OUT	ACTIVE
READ	0	1	1	HI-Z	ACTIVE
DESELECT	×	×	×	HI-Z	CMOS STANDBY
DESELECT	×	×	×	HI-Z	BATTERY BACK-UP MODE

1 : HIGH LEVEL
0 : LOW LEVEL
× : DON'T CARE
HI-Z : HIGH IMPEDANCE


VDD
28
VOLTAGE SENSE AND SWITCHING CIRCUITRY
POWER
VPFD
8 K × 8 SRAM ARRAY
2 - 10, 21,23 - 25
A0 - A12
11 - 13, 15 - 19
DQ0 - DQ7
20
E
27
W
22
G
INTERNAL BATTERY
14
GND