

1Mb (128K x 8) ZEROPOWER[®] SRAM

DATA BRIEFING

- INTEGRATED LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER
- MICROPROCESSOR POWER-ON RESET (Valid even during battery back-up mode)
- BATTERY LOW PIN PROVIDES EARLY WARNING of BATTERY END-OF-LIFE
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGE (V_{PFD} = Power-fail Deselect Voltage):
 - M48Z129Y: $4.20V \leq V_{PFD} \leq 4.50V$
 - M48Z129V: $2.70V \leq V_{PFD} \leq 3.00V$
- BATTERY INTERNALLY ISOLATED UNTIL POWER IS APPLIED
- COMPATIBLE with STANDARD 128Kx8 SRAMs

DESCRIPTION

The M48Z129Y/129V ZEROPOWER[®] RAM is a non-volatile 1,048,576 bit Static RAM organized as 131,072 words by 8 bits. The device combines an internal lithium battery, a CMOS SRAM and a control circuit in a plastic 32 pin DIP Module.

A Battery Low ($\overline{BL}$) pin warns the user of battery end-of-life, providing true data non-volatility. The open-drain Reset ($\overline{RST}$) output pin is used to provide a reset pulse, insuring proper system operation. Due to the ultra-low power required by the M48Z129Y/129V, nominal battery life exceeds 10 years, thus outlasting the useful lifetime of most end-user equipment.

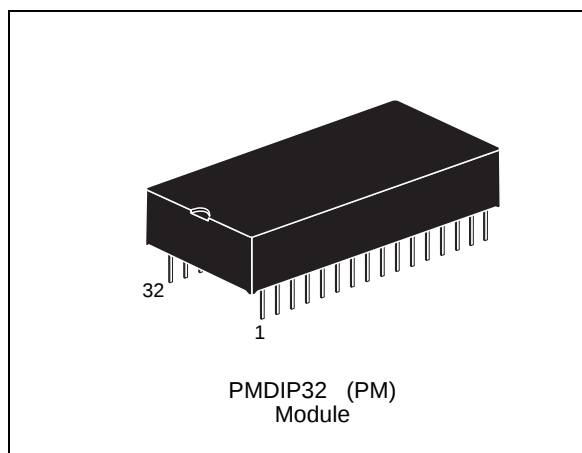
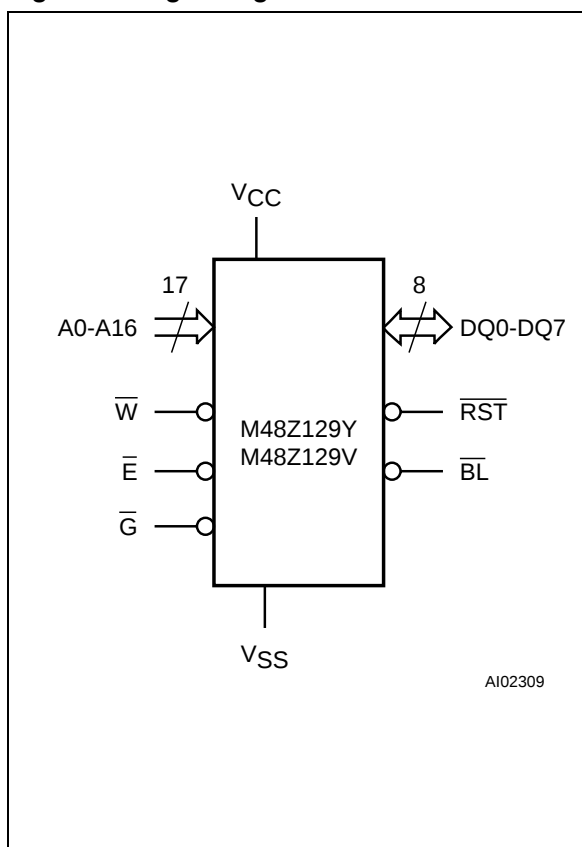
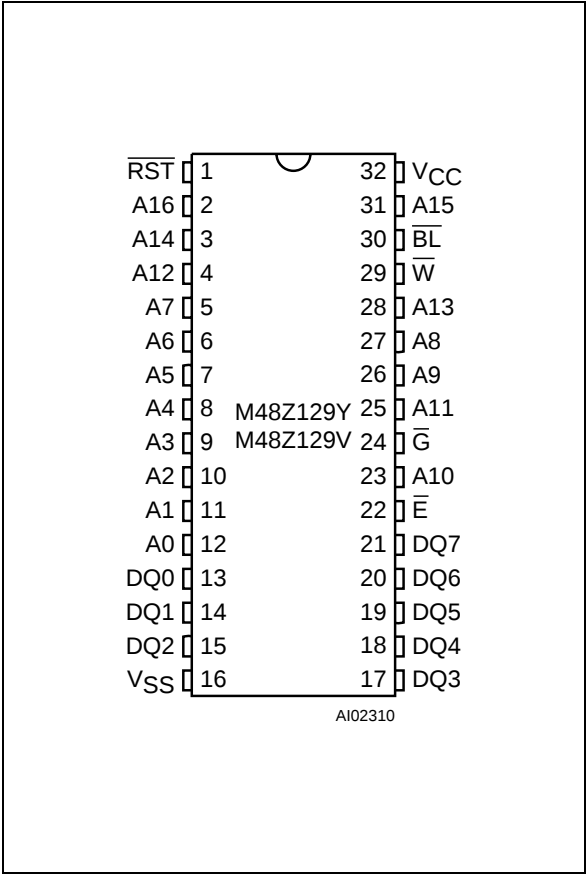


Figure 1. Logic Diagram



M48Z129Y, M48Z129V

DIP Pin Connections



Ordering Information Scheme

For a list of available options or for further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

Example: M48Z129Y -70 PM 1

Supply Voltage and Write Protect Voltage	
129Y	$V_{CC} = 4.5V$ to $5.5V$ $V_{PFD} = 4.2V$ to $4.5V$
129V	$V_{CC} = 3.0V$ to $3.6V$ $V_{PFD} = 2.7V$ to $3.0V$
Speed	
-70	70ns
Package	
PM	PMDIP32
Temperature Range	
1	0 to 70 °C

Signal Names

A0-A16	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RST}$	Reset Output (Open Drain)
$\overline{BL}$	Battery Low Output
VCC	Supply Voltage
VSS	Ground