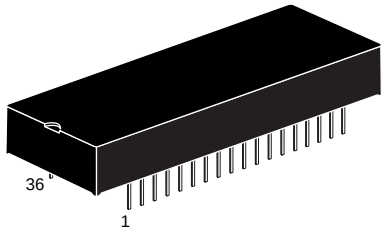
M48T513Y
M48T513V

3.3V-5V 4 Mb (512K x 8) TIMEKEEPER® SRAM

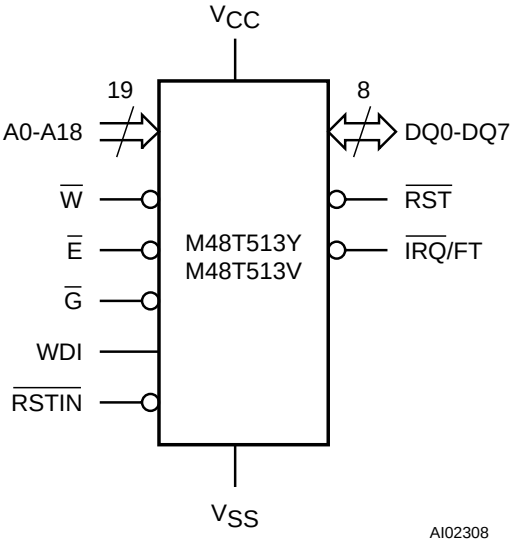
DATA BRIEFING

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, POWER-FAIL CONTROL CIRCUIT, BATTERY and CRYSTAL
- YEAR 2000 COMPLIANT-CENTURY REGISTER
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES and SECONDS
- BATTERY LOW WARNING FLAG
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGES (V_{PFD} = Power-fail Deselect Voltage):
  - M48T513Y: $4.20V \leq V_{PFD} \leq 4.50V$
  - M48T513V: $2.70V \leq V_{PFD} \leq 3.00V$
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- SOFTWARE CONTROLLED CLOCK CALIBRATION for HIGH ACCURACY APPLICATIONS
- 10 YEARS of DATA RETENTION and CLOCK OPERATION in the ABSENCE of POWER
- SELF-CONTAINED BATTERY and CRYSTAL in DIP PACKAGE
- MICROPROCESSOR POWER-ON RESET (Valid even during battery back-up mode)
- PROGRAMMABLE ALARM OUTPUT ACTIVE in the BATTERY BACK-UP MODE



PMLDIP36 (PL)
Module

Logic Diagram

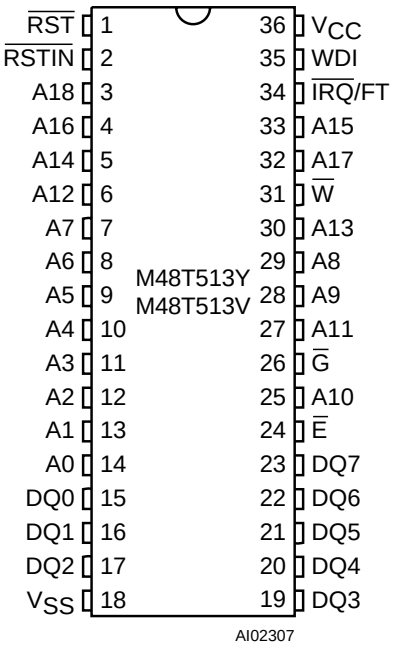


DESCRIPTION

The M48T513Y/513V TIMEKEEPER® RAM is a non-volatile 4,194,304 bit static RAM and real time clock organized as 524,288 words by 8 bits. System integration features include Programmable Alarms, Battery Low status Flag and a Power-on Reset. The special 36-pin DIP package provides a highly integrated battery back-up memory and real time clock solution.

The memory locations providing user accessible BYTEWIDE™ clock information are in the bytes with addresses 7FF1h and 7FF9h-7FFFh. These clock locations contain the century, year, month, date, day, hour, minute and second in 24 hour BCD format. Corrections for 28, 29 (leap year, including year 2000), 30, and 31 day months are made automatically. Reference the M48T201 data sheet for complete register map.

DIP Pin Connections



Ordering Information Scheme

For a list of available options or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

Example: M48T513Y -70 PL 1

Supply Voltage and Write Protect Voltage

513Y V_{CC} = 4.50V to 5.50V
V_{PFD} = 4.20V to 4.50V

513V V_{CC} = 3.00V to 3.60V
V_{PFD} = 2.70V to 3.00V

Speed

-70 70ns (M48T513Y)

-85 85ns (M48T513V)

Package

PL PMLDIP36

Temperature Range

1 0 to 70 °C

Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable Input
$\overline{G}$	Output Enable Input
$\overline{W}$	Write Enable Input
WDI	Watchdog input
$\overline{RST}$	Reset Output (open drain)
$\overline{RSTIN}$	Reset Input
$\overline{IRQ}$/FT	Interrupt / Frequency Test Output (open drain)
V_{CC}	Supply Voltage
V_{SS}	Ground