M35053-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DESCRIPTION

The M35053-XXXSP/FP is TV screen display control IC which can be used to display information such as number of channels, the date and messages and program schedules on the TV screen.
In particular, owing to the built-in SYNC-SEP (synchronous separation) circuit, the synchronous correction circuit, the Decoder circuit, and to the Encoder circuit, external circuits can be decrease and character turbulence that occurs when superimposing can be reduced.
The processor can conform to the EDS broadcast service and is suitable for AV systems such as VTRs, LDs, and so on.
It is a silicon gate CMOS process and M35053-XXXSP is housed in a 20-pin shrink DIP package, M35053-XXXFP is housed in a 20-pin shrink SOP package.
For M35053-001SP/FP that is a standard ROM version of M35053-XXXSP/FP respectively, the character pattern is also mentioned.

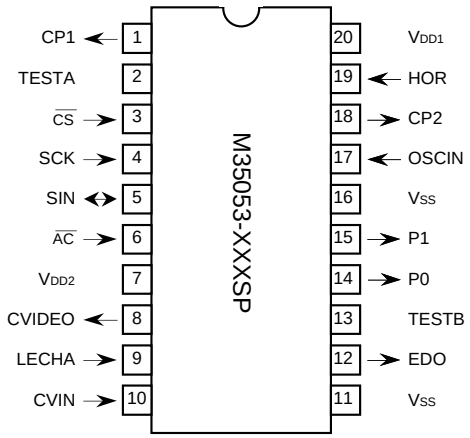
FEATURES

- Screen composition ..... 24 characters × 10 lines, 32 characters × 7 lines
- Number of characters displayed ..... 240 (Max.)
- Character composition ..... 12 × 18 dot matrix
- Characters available ..... 256 characters
- Character sizes available ..... 4 (horizontal) × 4 (vertical)
- Display locations available
  - Horizontal direction ..... 240 locations
  - Vertical direction ..... 256 locations
- Blinking ..... Character units
  - Cycle : approximately 1 second, or approximately 0.5 seconds
  - Duty : 25%, 50%, or 75%
- Data input ..... By the serial input function (16 bits)
- Coloring
  - Background coloring (composite video signal)
- Blanking
  - Total blanking (14 × 18 dots)
  - Border size blanking
  - Character size blanking
- Synchronizing signal
  - Composite synchronizing signal generation (PAL, NTSC, M-PAL)
- 2 output ports (1 digital line)
- Oscillation stop function
  - It is possible to stop the oscillation for synchronizing signal generation
- Built-in half-tone display function
- Built-in reversed character display function
- Built-in Decoder (NTSC only)
- Built-in Encoder (NTSC only)
- Built-in synchronous correction circuit
- Built-in synchronous separation circuit

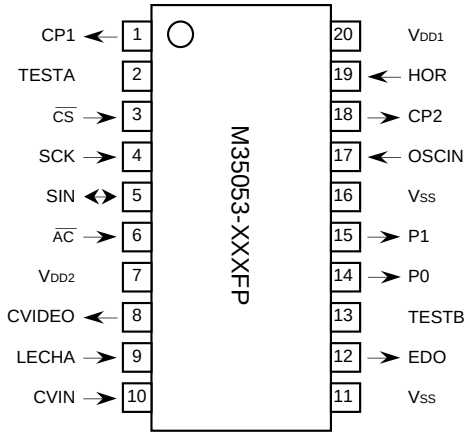
APPLICATION

TV, VCR, Movie

PIN CONFIGURATION (TOP VIEW)



Outline 20P4B

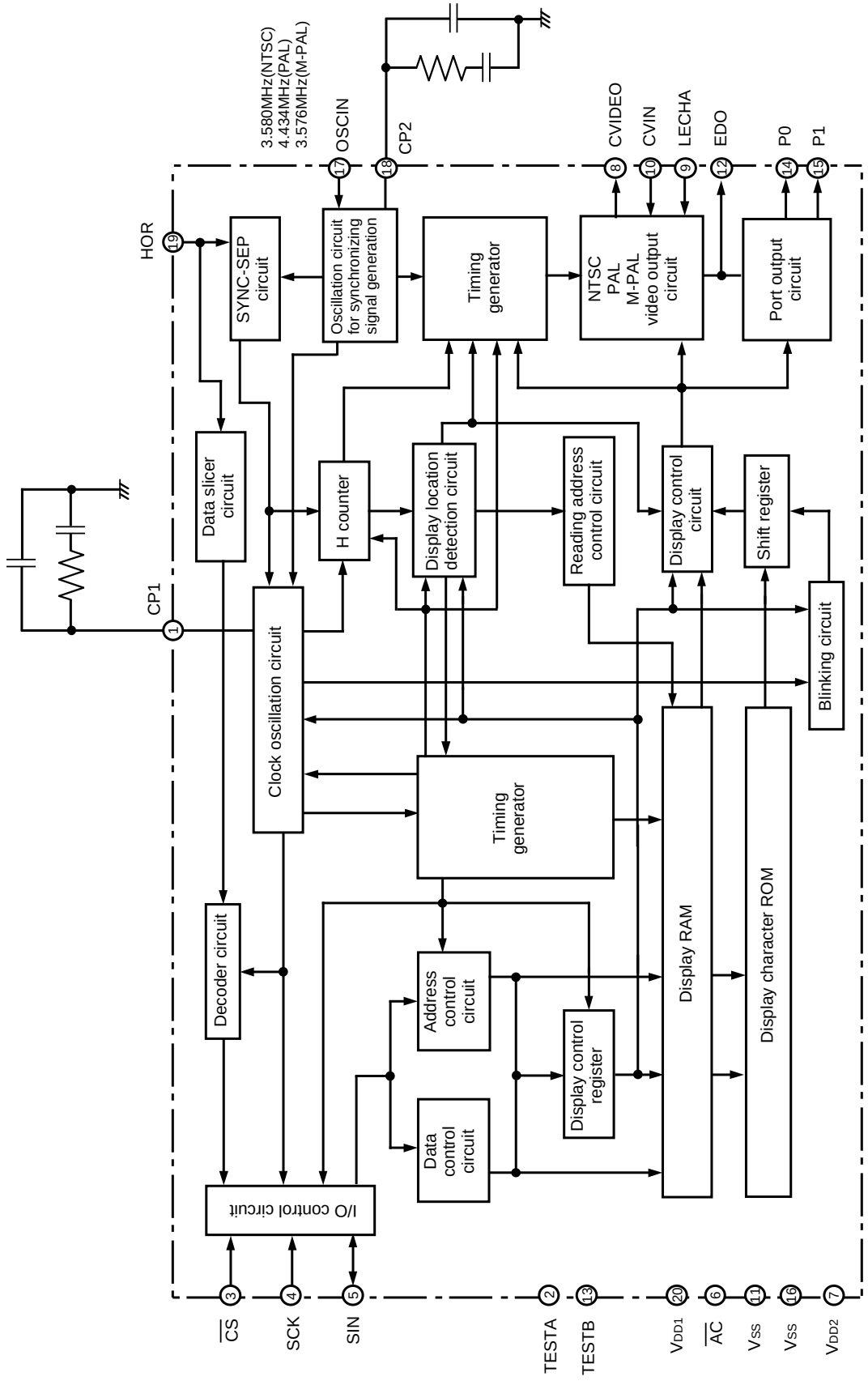


Outline 20P2Q-A

PIN DESCRIPTION

Symbol	Pin name	Input/ Output	Function
OSC1	Clock input	Input	This is the filter output pin 1.
TESTA	Test pin	—	This is the pin for test. Connect this pin to GND during normal operation.
$\overline{CS}$	Chip select input	Input	This is the chip select pin, and when serial data transmission is being carried out, it goes to “L”. Hysteresis input. Includes built-in pull-up resistor.
SCK	Serial clock input	Input	When $\overline{CS}$ pin is “L”, SIN serial data is taken in when SCK rises. Hysteresis input. Built-in pull-up resistor is included.
SIN	Serial data input/ output	Input/ Output	This is the pin for serial input of data and addresses for the display control register and the display data memory. Also, serially outputs decode data according to the settings in the relevant registers (serial I/O).
$\overline{AC}$	Auto-clear input	Input	When “L”, this pin resets the internal IC circuit. Hysteresis input. Includes built-in pull-up resistor.
V_{DD2}	Power pin	—	Please connect to +5V with the analog circuit power pin.
CVIDEO	Composite video signal output	Output	This is the output pin for composite video signals. It outputs $2V_{P-P}$ composite video signals. In superimpose mode, character output etc. is superimposed on the external composite video signals from CVIN.
LECHA	Character level input	Input	This is the input pin which determines the “white” character color level in the composite video signal.
CVIN	Composite video signal input	Input	This is the input pin for external composite video signals. In superimpose mode, character output etc. is superimposed on these external composite video signals.
V_{SS}	Earthing pin	—	Please connect to GND using circuit earthing pin.
EDO	Encode data output	Output	This is the output pin for encode data. It outputs digital three-value data or composite video signals.
TESTB	Test pin	—	This is the pin for test. Connect this pin to GND during normal operation.
P0	Port P0 output	Output	This pin outputs the port output or BLNK1 (character background) signal.
P1	Port P1 output	Output	This pin outputs the port output or CO1(character) signal.
V_{SS}	Earthing pin	—	Please connect to GND using circuit earthing pin (Analog side).
OSCIN	f_{SC} input pin for synchronous signal generation	Input	This is the input pin for the sub-carrier frequency (f_{SC}) for generating a synchronous signal. A frequency of 3.580MHz is needed for NTSC, and a frequency of 4.434MHz in needed for PAL and 3.576MHz is needed for M-PAL.
CP2	Filter output	Output	Filter output pin 2.
HOR	Horizontal synchro-nizing signal input	Input	This is the input pin for external composite video signals. This pin inputs the external video signal clamped sync-chip to 1.5V, and internally carries out synchronous separa-tion.
V_{DD1}	Power pin	—	Please connect to +5V with the digital circuit power pin.

BLOCK DIAGRAM



MEMORY CONSTITUTION

Address 00_{16} to EF_{16} are assigned to the display RAM, address $F0_{16}$ to $F8_{16}$ are assigned to the display control registers.
The internal circuit is reset and all display control registers (address $F0_{16}$ to $F8_{16}$) are set to "0" and display RAM (address 00_{16} to EF_{16}) are RAM erased when the $\overline{AC}$ pin level is "L".

Set "0" in any of bits DAD through DAF of addresses 00_{16} through EF_{16}, and of bits DAE and DAF of addresses $F0_{16}$ through $F8_{16}$.
TESTn (n : a number) is MITSUBISHI test memory, so be sure to observe the setting conditions.

Bit / Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Remarks
00_{16}	0	0	0	REV	BLINK	EC2	EC1	EC0	C7	C6	C5	C4	C3	C2	C1	C0	Display RAM
↓	⋮	⋮	⋮	Reversed character	Blinking	Encode data or character color			Character code								
EF_{16}	0	0	0	REV	BLINK	EC2	EC1	EC0	C7	C6	C5	C4	C3	C2	C1	C0	
$F0_{16}$	0	0	TEST25	$\overline{W/R}$	TEST11	TEST10	DECB1	DECB0	SYSEP1	SYSEP0	SEPV1	SEPV0	PTD1	PTD0	PTC1	PTC0	Port output specify and so on
$F1_{16}$	0	0	TEST26	DVP4	DVP3	DVP2	DVP1	DVP0	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display start position and Decode position specify
$F2_{16}$	0	0	TEST27	EVP4	EVP3	EVP2	EVP1	EVP0	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display start position and Encode position specify
$F3_{16}$	0	0	TEST28	$\overline{D/V}$	EFLD1	EFLD0	DFLD1	DFLD0	VSZ21	VSZ20	VSZ11	VSZ10	HSZ21	HSZ20	HSZ11	HSZ10	Character size and Encode·Decode specify
$F4_{16}$	0	0	TEST29	TEST14	TEST13	SPACE	DSP9	DSP8	DSP7	DSP6	DSP5	DSP4	DSP3	DSP2	DSP1	DSP0	Display mode specify
$F5_{16}$	0	0	TEST30	TEST19	$\overline{MB/LB}$	TEST17	TEST16	TEST15	EQP	PALH	MPAL	$\overline{INT/NON}$	$\overline{N/P}$	BLINK2	BLINK1	BLINK0	Blinking specify and so on
$F6_{16}$	0	0	TEST31	TEST2	TEST1	TEST0	LBLACK	$\overline{LIN24/32}$	BLKHF	BB	BG	BR	LEVEL0	PHASE2	PHASE1	PHASE0	Raster color specify
$F7_{16}$	0	0	TEST32	TEST24	RGBON	TEST22	$\overline{CL17/18}$	CBLINK	CURS7	CURS6	CURS5	CURS4	CURS3	CURS2	CURS1	CURS0	Cursor display specify
$F8_{16}$	0	0	LEVEL1	EHP4	EHP3	EHP2	EHP1	EHP0	RAMERS	DSPON	STOP1	STOPIN	SCOR	EX	BLK1	BLK0	Control display and so on

Fig. 1 Memory constitution (M35053-XXXSP/FP)

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM. The screen consitution (24 characters × 10 lines) is shown in Figure 2 the screen constitution (32 characters × 7 lines) is shown in 3.

Lines \ Rows	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	00₁₆	01₁₆	02₁₆	03₁₆	04₁₆	05₁₆	06₁₆	07₁₆	08₁₆	09₁₆	0A₁₆	0B₁₆	0C₁₆	0D₁₆	0E₁₆	0F₁₆	10₁₆	11₁₆	12₁₆	13₁₆	14₁₆	15₁₆	16₁₆	17₁₆
2	18₁₆	19₁₆	1A₁₆	1B₁₆	1C₁₆	1D₁₆	1E₁₆	1F₁₆	20₁₆	21₁₆	22₁₆	23₁₆	24₁₆	25₁₆	26₁₆	27₁₆	28₁₆	29₁₆	2A₁₆	2B₁₆	2C₁₆	2D₁₆	2E₁₆	2F₁₆
3	30₁₆	31₁₆	32₁₆	33₁₆	34₁₆	35₁₆	36₁₆	37₁₆	38₁₆	39₁₆	3A₁₆	3B₁₆	3C₁₆	3D₁₆	3E₁₆	3F₁₆	40₁₆	41₁₆	42₁₆	43₁₆	44₁₆	45₁₆	46₁₆	47₁₆
4	48₁₆	49₁₆	4A₁₆	4B₁₆	4C₁₆	4D₁₆	4E₁₆	4F₁₆	50₁₆	51₁₆	52₁₆	53₁₆	54₁₆	55₁₆	56₁₆	57₁₆	58₁₆	59₁₆	5A₁₆	5B₁₆	5C₁₆	5D₁₆	5E₁₆	5F₁₆
5	60₁₆	61₁₆	62₁₆	63₁₆	64₁₆	65₁₆	66₁₆	67₁₆	68₁₆	69₁₆	6A₁₆	6B₁₆	6C₁₆	6D₁₆	6E₁₆	6F₁₆	70₁₆	71₁₆	72₁₆	73₁₆	74₁₆	75₁₆	76₁₆	77₁₆
6	78₁₆	79₁₆	7A₁₆	7B₁₆	7C₁₆	7D₁₆	7E₁₆	7F₁₆	80₁₆	81₁₆	82₁₆	83₁₆	84₁₆	85₁₆	86₁₆	87₁₆	88₁₆	89₁₆	8A₁₆	8B₁₆	8C₁₆	8D₁₆	8E₁₆	8F₁₆
7	90₁₆	91₁₆	92₁₆	93₁₆	94₁₆	95₁₆	96₁₆	97₁₆	98₁₆	99₁₆	9A₁₆	9B₁₆	9C₁₆	9D₁₆	9E₁₆	9F₁₆	A0₁₆	A1₁₆	A2₁₆	A3₁₆	A4₁₆	A5₁₆	A6₁₆	A7₁₆
8	A8₁₆	A9₁₆	AA₁₆	AB₁₆	AC₁₆	AD₁₆	AE₁₆	AF₁₆	B0₁₆	B1₁₆	B2₁₆	B3₁₆	B4₁₆	B5₁₆	B6₁₆	B7₁₆	B8₁₆	B9₁₆	BA₁₆	BB₁₆	BC₁₆	BD₁₆	BE₁₆	BF₁₆
9	C0₁₆	C1₁₆	C2₁₆	C3₁₆	C4₁₆	C5₁₆	C6₁₆	C7₁₆	C8₁₆	C9₁₆	CA₁₆	CB₁₆	CC₁₆	CD₁₆	CE₁₆	CF₁₆	D0₁₆	D1₁₆	D2₁₆	D3₁₆	D4₁₆	D5₁₆	D6₁₆	D7₁₆
10	D8₁₆	D9₁₆	DA₁₆	DB₁₆	DC₁₆	DD₁₆	DE₁₆	DF₁₆	E0₁₆	E1₁₆	E2₁₆	E3₁₆	E4₁₆	E5₁₆	E6₁₆	E7₁₆	E8₁₆	E9₁₆	EA₁₆	EB₁₆	EC₁₆	ED₁₆	EE₁₆	EF₁₆

Note : The hexadecimal numbers in the boxes show the display RAM address.

Fig. 2 Screen constitution (24 characters × 10 lines)

Lines \ Rows	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
1	00₁₆	01₁₆	02₁₆	03₁₆	04₁₆	05₁₆	06₁₆	07₁₆	08₁₆	09₁₆	0A₁₆	0B₁₆	0C₁₆	0D₁₆	0E₁₆	0F₁₆	10₁₆	11₁₆	12₁₆	13₁₆	14₁₆	15₁₆	16₁₆	17₁₆	18₁₆	19₁₆	1A₁₆	1B₁₆	1C₁₆	1D₁₆	1E₁₆	1F₁₆
2	20₁₆	21₁₆	22₁₆	23₁₆	24₁₆	25₁₆	26₁₆	27₁₆	28₁₆	29₁₆	2A₁₆	2B₁₆	2C₁₆	2D₁₆	2E₁₆	2F₁₆	30₁₆	31₁₆	32₁₆	33₁₆	34₁₆	35₁₆	36₁₆	37₁₆	38₁₆	39₁₆	3A₁₆	3B₁₆	3C₁₆	3D₁₆	3E₁₆	3F₁₆
3	40₁₆	41₁₆	42₁₆	43₁₆	44₁₆	45₁₆	46₁₆	47₁₆	48₁₆	49₁₆	4A₁₆	4B₁₆	4C₁₆	4D₁₆	4E₁₆	4F₁₆	50₁₆	51₁₆	52₁₆	53₁₆	54₁₆	55₁₆	56₁₆	57₁₆	58₁₆	59₁₆	5A₁₆	5B₁₆	5C₁₆	5D₁₆	5E₁₆	5F₁₆
4	60₁₆	61₁₆	62₁₆	63₁₆	64₁₆	65₁₆	66₁₆	67₁₆	68₁₆	69₁₆	6A₁₆	6B₁₆	6C₁₆	6D₁₆	6E₁₆	6F₁₆	70₁₆	71₁₆	72₁₆	73₁₆	74₁₆	75₁₆	76₁₆	77₁₆	78₁₆	79₁₆	7A₁₆	7B₁₆	7C₁₆	7D₁₆	7E₁₆	7F₁₆
5	80₁₆	81₁₆	82₁₆	83₁₆	84₁₆	85₁₆	86₁₆	87₁₆	88₁₆	89₁₆	8A₁₆	8B₁₆	8C₁₆	8D₁₆	8E₁₆	8F₁₆	90₁₆	91₁₆	92₁₆	93₁₆	94₁₆	95₁₆	96₁₆	97₁₆	98₁₆	99₁₆	9A₁₆	9B₁₆	9C₁₆	9D₁₆	9E₁₆	9F₁₆
6	A0₁₆	A1₁₆	A2₁₆	A3₁₆	A4₁₆	A5₁₆	A6₁₆	A7₁₆	A8₁₆	A9₁₆	AA₁₆	AB₁₆	AC₁₆	AD₁₆	AE₁₆	AF₁₆	B0₁₆	B1₁₆	B2₁₆	B3₁₆	B4₁₆	B5₁₆	B6₁₆	B7₁₆	B8₁₆	B9₁₆	BA₁₆	BB₁₆	BC₁₆	BD₁₆	BE₁₆	BF₁₆
7	C0₁₆	C1₁₆	C2₁₆	C3₁₆	C4₁₆	C5₁₆	C6₁₆	C7₁₆	C8₁₆	C9₁₆	CA₁₆	CB₁₆	CC₁₆	CD₁₆	CE₁₆	CF₁₆	D0₁₆	D1₁₆	D2₁₆	D3₁₆	D4₁₆	D5₁₆	D6₁₆	D7₁₆	D8₁₆	D9₁₆	DA₁₆	DB₁₆	DC₁₆	DD₁₆	DE₁₆	DF₁₆

Notes 1. The hexadecimal numbers in the boxes show the display RAM address.
2. When 32 characters × 7 lines are displayed, set blank code "FF₁₆" to character code of addresses E0₁₆ to EF₁₆.

Fig. 3 Screen constitution (32 characters × 7 lines)

Display RAM DESCRIPTION

Display RAM Address 00_{16} to EF_{16}

DA 0~C	Name	Contents		Remarks
		Status	Function	
0	C0 (LSB)	0	Set ROM-held character code of a character needed to display.	
		①		
1	C1	0		
		①		
2	C2	0		
		①		
3	C3	0		
		①		
4	C4	0		
		①		
5	C5	0		
		①		
6	C6	0		
		①		
7	C7 (MSB)	0		
		①		
8	EC0	0	When EFILD1, 0=1, 0 or 0, 1, set code of the data needed to encode. When RGBON=1, set background color by character unit.	Refer to encode function. Refer to supplemental explanation (4).
		①		
9	EC1	0		
		①		
A	EC2	0		
		①		
B	BLINK	0	No blinking	Refer to BLINK2 to 0 (address $F5_{16}$)
		①	Blinking	
C	REV	⓪	Normal character	
		1	Reversed character	

Note. Resetting at the AC pin RAM-erases the display RAM, and the status turns as indicated by the mark ◯ around in the status column.

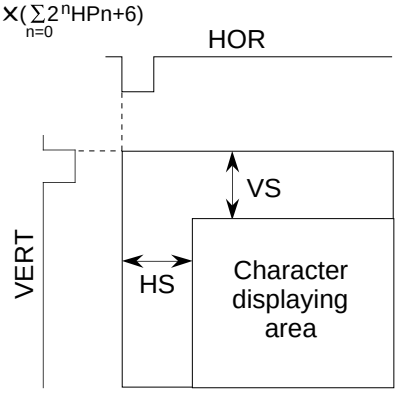
Display control register

(1) Address F0$_{16}$

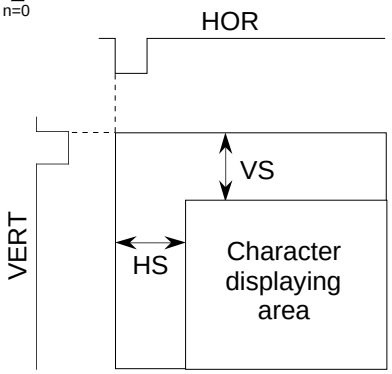
<table>
<tr><th rowspan="2">DA
0~D</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">PTC0</td><td>⓪</td><td>P0 output (port 0)</td><td rowspan="2">Port output control</td></tr>
<tr><td>1</td><td>BLNK1 output</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">PTC1</td><td>⓪</td><td>P1 output (port 1)</td><td rowspan="2">Refer to supplemental explanation (5).</td></tr>
<tr><td>1</td><td>CO1 output</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">PTD0</td><td>⓪</td><td>It is negative polarity at P0 output “L”, BLINK1 output.</td><td rowspan="2">Control the port data</td></tr>
<tr><td>1</td><td>It is positive polarity at P0 output “H”, BLINK1 output.</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">PTD1</td><td>⓪</td><td>It is negative polarity at P01 output “L”, CO1 output.</td><td rowspan="2">Refer to supplemental explanation (5).</td></tr>
<tr><td>1</td><td>It is positive polarity at P01 output “H”, CO1 output.</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">SEPV0</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2">Specifies the vertical synchronous separation criterion</td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">SEPV1</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2">Refer to supplemental explanation (1).</td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">SYSEP0</td><td>⓪</td><td rowspan="4"><table><tr><th>SYSEP1</th><th>SYSEP0</th><th>Bias potential</th></tr><tr><td>0</td><td>0</td><td>Can not be used.</td></tr><tr><td>0</td><td>1</td><td>Can not be used.</td></tr><tr><td>1</td><td>0</td><td>1.75V</td></tr><tr><td>1</td><td>1</td><td>Can not be used.</td></tr></table></td><td rowspan="4">Specifies the sync-bias potential</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">SYSEP1</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">DECB0</td><td>⓪</td><td rowspan="4"><table><tr><th>DECB1</th><th>DECB0</th><th>Bias potential</th></tr><tr><td>0</td><td>0</td><td>2.35V</td></tr><tr><td>0</td><td>1</td><td>Can not be used.</td></tr><tr><td>1</td><td>0</td><td>Can not be used.</td></tr><tr><td>1</td><td>1</td><td>Can not be used.</td></tr></table></td><td rowspan="4">Specifies the decoding bias potential</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">DECB1</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">TEST10</td><td>⓪</td><td>Can not be used.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>It should be fixed to “1”.</td></tr>
<tr><td rowspan="2">B</td><td rowspan="2">TEST11</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">C</td><td rowspan="2">$\overline{W}$/R</td><td>⓪</td><td>Input data from SIN pin</td><td>Control data I/O</td></tr>
<tr><td>1</td><td>Output data from SIN pin (Note 2)</td><td>Refer to decode data output timing.</td></tr>
<tr><td rowspan="2">D</td><td rowspan="2">TEST25</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
</table>

Notes 1. The mark ◯ around the status value means the reset status by the “L” level is input to $\overline{AC}$ pin.
2. Not necessary to release after setting $\overline{W}$/R to “1”. Turn $\overline{CS}$ to “H” to switch over to input mode.

(2) Address F1$_{16}$

DA 0~D	Register	Contents		Remarks
		Status	Function	
0	HP0 (LSB)	⓪	Let horizontal display start position be HS, $HS=T\times(\sum_{n=0}^{7}2^{n}HPn+6)$  T : The oscillation cycle of display clock	Set the horizontal display start position by use of HP7 through HP0. HP7 to HP0 = (00000000) to (00001111) setting is forbidden. It can be set this up to 240 steps in increments of one T.
		1		
1	HP1	⓪		
		1		
2	HP2	⓪		
		1		
3	HP3	⓪		
		1		
4	HP4	⓪		
		1		
5	HP5	⓪		
		1		
6	HP6	⓪		
		1		
7	HP7 (MSB)	⓪		
		1		
8	DVP0 (LSB)	⓪	Let the slice lines be DVS, $DVS=\sum_{n=0}^{4}2^{n}DVPn+6$	Set the slice lines (horizontal scanning lines) under decoding by use of DVP4 through DVP0. DVP4 to DVP0 = (00000) to (00011) setting is forbidden. Thus, it can be defined a setting up to 26 steps covered by a range from line 10 to line 35. Refer to supplemental explanation (2) about slice lines (DVS).
		1		
9	DVP1	⓪		
		1		
A	DVP2	⓪		
		1		
B	DVP3	⓪		
		1		
C	DVP4 (MSB)	⓪		
		1		
D	TEST26	⓪	It should be fixed to “0”.	
		1	Can not be used.	

(3) Address F2$_{16}$

DA 0~D	Register	Contents		Remarks
		Status	Function	
0	VP0 (LSB)	⓪	Let vertical display start position be VS, $VS=H\times\sum_{n=0}^{7}2^{n}VPn$  H : The oscillation cycle of horizontal synchronous signal	Set the vertical display start position by use of VP7 through VP0. VP7 to VP0 = (00000000) to (00000110) setting is forbidden. It can be set this up to 249 steps in increments of one H. VP7 to VP0 = (00000000) to (00100011) setting is forbidden under encoding or decoding.
		1		
1	VP1	⓪		
		1		
2	VP2	⓪		
		1		
3	VP3	⓪		
		1		
4	VP4	⓪		
		1		
5	VP5	⓪		
		1		
6	VP6	⓪		
		1		
7	VP7 (MSB)	⓪		
		1		
8	EVP0 (LSB)	⓪	Let the encode lines be EVS, $EVS=\sum_{n=0}^{4}2^{n}EVPn+6$	Sets the lines (horizontal scanning lines) under encoding by use of EVP4 through EVP0. EVP4 to EVP0 = (00000) to (00011) setting is forbidden. Thus, it can be defined a setting up to 26 steps covered by a range from line 10 to line 35. Refer to supplemental explanation (2) about the encode lines (EVS).
		1		
9	EVP1	⓪		
		1		
A	EVP2	⓪		
		1		
B	EVP3	⓪		
		1		
C	EVP4 (MSB)	⓪		
		1		
D	TEST27	⓪	It should be fixed to “0”.	
		1	Can not be used.	

(4) Address F3$_{16}$

<table>
<tr><th>DA
0~D</th><th>Register</th><th colspan="2">Contents</th><th>Remarks</th></tr>
<tr><th></th><th></th><th>Status</th><th>Function</th><th></th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">HSZ10</td><td>⓪</td><td rowspan="5"><table><tr><th>HSZ11</th><th>HSZ10</th><th>Horizontal direction size</th></tr><tr><td>0</td><td>0</td><td>1T/dot</td></tr><tr><td>0</td><td>1</td><td>2T/dot</td></tr><tr><td>1</td><td>0</td><td>3T/dot</td></tr><tr><td>1</td><td>1</td><td>4T/dot</td></tr></table></td><td rowspan="2">Character size setting in the horizontal direction for the first line.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">HSZ11</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">HSZ20</td><td>⓪</td><td rowspan="5"><table><tr><th>HSZ21</th><th>HSZ20</th><th>Horizontal direction size</th></tr><tr><td>0</td><td>0</td><td>1T/dot</td></tr><tr><td>0</td><td>1</td><td>2T/dot</td></tr><tr><td>1</td><td>0</td><td>3T/dot</td></tr><tr><td>1</td><td>1</td><td>4T/dot</td></tr></table></td><td rowspan="4">Character size setting in the horizontal direction for the 2nd line to 10th line.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">HSZ21</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">VSZ10</td><td>⓪</td><td rowspan="5"><table><tr><th>VSZ11</th><th>VSZ10</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="4">Character size setting in the vertical direction for the first line.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">VSZ11</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">VSZ20</td><td>⓪</td><td rowspan="5"><table><tr><th>VSZ21</th><th>VSZ20</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="4">Character size setting in the vertical direction for the 2nd line to 10th line.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">VSZ21</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">DFLD0</td><td>⓪</td><td rowspan="5"><table><tr><th>DFLD1</th><th>DFLD0</th><th>Field detection</th></tr><tr><td>0</td><td>0</td><td>OFF</td></tr><tr><td>0</td><td>1</td><td>The first field</td></tr><tr><td>1</td><td>0</td><td>The second field</td></tr><tr><td>1</td><td>1</td><td>Can not be used</td></tr></table></td><td rowspan="4">Specifies the field determination procedure in relation to the Decoding functions.
Refer to supplemental explanation (2).</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">DFLD1</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">EFILD0</td><td>⓪</td><td rowspan="5"><table><tr><th>EFLD1</th><th>EFLD0</th><th>Field detection</th></tr><tr><td>0</td><td>0</td><td>OFF</td></tr><tr><td>0</td><td>1</td><td>The first field</td></tr><tr><td>1</td><td>0</td><td>The second field</td></tr><tr><td>1</td><td>1</td><td>Can not be used</td></tr></table></td><td rowspan="4">Specifies the field determination procedure in relation to the Encoding functions.
Refer to supplemental explanation (2).</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">B</td><td rowspan="2">EFLD1</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">C</td><td rowspan="2">$\overline{D/V}$</td><td>⓪</td><td>It outputs digital signal.</td><td rowspan="2">Encode (EDO) output control.
Refer to encode function (3).</td></tr>
<tr><td>1</td><td>It outputs composite video signal (Note).</td></tr>
<tr><td rowspan="2">D</td><td rowspan="2">TEST28</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
</table>

Note. Output buffer is needed with EDO (12-pin) at $\overline{D/V}$= “1”. (Refer to example of peripheral circuit)

(5) Address F4$_{16}$

<table>
<tr><th rowspan="2">DA
0~D</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>DSP0</td><td>⓪</td><td rowspan="20">
<table>
<tr><th>BLK1</th><th>BLK0</th><th>DSPn= “1”</th><th>DSPn= “0”</th></tr>
<tr><td>0</td><td>0</td><td>Matrix-outline border size</td><td>Matrix-outline size</td></tr>
<tr><td>0</td><td>1</td><td>Border size</td><td>Character size</td></tr>
<tr><td>1</td><td>0</td><td>Matrix-outline size</td><td>Border size</td></tr>
<tr><td>1</td><td>1</td><td>Character size</td><td>Matrix-outline size</td></tr>
</table>
Depends on BLK0 and BLK1 (address F8$_{16}$)
DSPn in the generic name for DSP0 to DSP9.
DSP0 to DSP9 are each controlled independently.
</td><td rowspan="2">Set the display mode of line 1.</td></tr>
<tr><td>1</td></tr>
<tr><td>1</td><td>DSP1</td><td>⓪</td><td rowspan="2">Set the display mode of line 2.</td></tr>
<tr><td>1</td></tr>
<tr><td>2</td><td>DSP2</td><td>⓪</td><td rowspan="2">Set the display mode of line 3.</td></tr>
<tr><td>1</td></tr>
<tr><td>3</td><td>DSP3</td><td>⓪</td><td rowspan="2">Set the display mode of line 4.</td></tr>
<tr><td>1</td></tr>
<tr><td>4</td><td>DSP4</td><td>⓪</td><td rowspan="2">Set the display mode of line 5.</td></tr>
<tr><td>1</td></tr>
<tr><td>5</td><td>DSP5</td><td>⓪</td><td rowspan="2">Set the display mode of line 6.</td></tr>
<tr><td>1</td></tr>
<tr><td>6</td><td>DSP6</td><td>⓪</td><td rowspan="2">Set the display mode of line 7.</td></tr>
<tr><td>1</td></tr>
<tr><td>7</td><td>DSP7</td><td>⓪</td><td rowspan="2">Set the display mode of line 8.</td></tr>
<tr><td>1</td></tr>
<tr><td>8</td><td>DSP8</td><td>⓪</td><td rowspan="2">Set the display mode of line 9.</td></tr>
<tr><td>1</td></tr>
<tr><td>9</td><td>DSP9</td><td>⓪</td><td rowspan="2">Set the display mode of line 10.</td></tr>
<tr><td>1</td></tr>
<tr><td>A</td><td>SPACE</td><td>⓪</td><td>Normal display</td><td rowspan="2">Put a space line between line 2 and line 3 in displaying 32 characters.</td></tr>
<tr><td>1</td><td>Put a space line between line 2 and line 3, and between line 8 and line 9.</td></tr>
<tr><td>B</td><td>TEST13</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td>C</td><td>TEST14</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td>D</td><td>TEST29</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
</table>

(6) Address F5$_{16}$

<table>
<tr><th rowspan="2">DA
0~D</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td rowspan="2">BLINK0</td><td>⓪</td><td rowspan="5"><table><tr><th>BLINK0</th><th>BLINK1</th><th>Duty</th></tr><tr><td>0</td><td>0</td><td>Blinking off</td></tr><tr><td>0</td><td>1</td><td>25%</td></tr><tr><td>1</td><td>0</td><td>50%</td></tr><tr><td>1</td><td>1</td><td>75%</td></tr></table></td><td rowspan="2">Blinking duty ratio can be altered. (Note)</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td>1</td><td rowspan="2">BLINK1</td><td>⓪</td><td rowspan="2">Blinking cycle can be altered.</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td>2</td><td rowspan="2">BLINK2</td><td>⓪</td><td>Division of vertical synchronizing signal into 1/64. Cycle approximately 1 second.</td></tr>
<tr><td>1</td><td>1</td><td>Division of vertical synchronizing signal into 1/32. Cycle approximately 0.5 second.</td></tr>
<tr><td>3</td><td rowspan="2">$\overline{N}$/P</td><td>⓪</td><td>NTSC, M-PAL mode</td><td rowspan="2">Refer to register MPAL</td></tr>
<tr><td>1</td><td>1</td><td>PAL mode</td></tr>
<tr><td>4</td><td rowspan="2">$\overline{INT}$/NON</td><td>⓪</td><td>Interlace</td><td rowspan="2">Scanning lines control (only in internal synchronization)</td></tr>
<tr><td>1</td><td>1</td><td>Non interlace</td></tr>
<tr><td>5</td><td>MPAL</td><td>⓪
1</td><td><table><tr><th>$\overline{N}$/P</th><th>MPAL</th><th>Synchronous mode</th></tr><tr><td>0</td><td>0</td><td>NTSC</td></tr><tr><td>0</td><td>1</td><td>M-PAL</td></tr><tr><td>1</td><td>0</td><td>PAL</td></tr><tr><td>1</td><td>1</td><td>Not available</td></tr></table></td><td>Synchronizing signal is selected with this register and N/P register.</td></tr>
<tr><td>6</td><td>PALH</td><td>⓪
1</td><td><table><tr><th>PALH</th><th>$\overline{INT}$/NON</th><th>Number of scanning lines</th></tr><tr><td rowspan="2">0</td><td>0</td><td>625H lines</td></tr><tr><td>1</td><td>626H lines</td></tr><tr><td rowspan="2">1</td><td>0</td><td>627H lines</td></tr><tr><td>1</td><td>628H lines</td></tr></table></td><td>It should be fixed to “0” at NTSC</td></tr>
<tr><td>7</td><td>EQP</td><td>⓪</td><td>Not include the equivalent pulse.</td><td rowspan="2">Effective only at non-interlace</td></tr>
<tr><td>1</td><td>1</td><td>Include the equivalent pulse.</td></tr>
<tr><td>8</td><td>TEST15</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>1</td><td>Can not be used.</td></tr>
<tr><td>9</td><td>TEST16</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>1</td><td>Can not be used.</td></tr>
<tr><td>A</td><td>TEST17</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>1</td><td>Can not be used.</td></tr>
<tr><td>B</td><td>$\overline{MB}$/LB</td><td>⓪</td><td>Output from MSB side</td><td rowspan="2">Setting the decode data output form</td></tr>
<tr><td>1</td><td>1</td><td>Output from LSB side</td></tr>
<tr><td>C</td><td>TEST19</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>1</td><td>Can not be used.</td></tr>
<tr><td>D</td><td>TEST30</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>1</td><td>Can not be used.</td></tr>
</table>

Note. To blink a character, set 1 to DAB (the blinking bit) of the display RAM.

(7) Address F6$_{16}$

<table>
<tr><th rowspan="2">DA
0~D</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="8">0
1
2</td><td rowspan="8">PHASE0
PHASE1
PHASE2</td><td>⓪</td><td rowspan="8"><table><tr><th>PHASE2</th><th>PHASE1</th><th>PHASE0</th><th>Raster</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table></td><td rowspan="8">Raster color setting
Refer to supplemental explanation (3) about video signal level</td></tr>
<tr><td>1</td></tr>
<tr><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">LEVEL0</td><td>⓪</td><td>Internal bias off</td><td rowspan="2">Generates bias potential for composite video signals</td></tr>
<tr><td>1</td><td>Internal bias on</td></tr>
<tr><td rowspan="8">4
5
6</td><td rowspan="8">BR
BG
BB</td><td>⓪</td><td rowspan="8"><table><tr><th>BB</th><th>BG</th><th>BR</th><th>Character back-ground color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table></td><td rowspan="8">Character background color setting.
Refer to supplemental explanation (3) about video signal level</td></tr>
<tr><td>1</td></tr>
<tr><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">BLKHF</td><td>⓪</td><td>The halftone displaying “OFF” in superimpose</td><td rowspan="2">This register is available in the superimpose displaying only. (Note)</td></tr>
<tr><td>1</td><td>The halftone displaying “ON” in superimpose</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">$\overline{\text{LIN}}$24/32</td><td>⓪</td><td>24 characters 5 10 lines display</td><td rowspan="2">“1” setting is forbidden under encoding.</td></tr>
<tr><td>1</td><td>32 characters 5 7 lines display</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">LBLACK</td><td>⓪</td><td>Blanking level I 2.3V</td><td rowspan="2">Set a blackness level</td></tr>
<tr><td>1</td><td>Blanking level II 2.1V</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">TEST0</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">B</td><td rowspan="2">TEST1</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">C</td><td rowspan="2">TEST2</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">D</td><td rowspan="2">TEST31</td><td>⓪</td><td>Can not be used.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>It should to be fixed to “1”.</td></tr>
</table>

Note. It is neccessary to input the external composite video signal to the CVIN pin, and externally connect a 100 to 200Ω register in series.

(8) Address F7$_{16}$

DA 0~D	Register	Contents		Remarks
		Status	Function	
0	CUR0	⓪	Let cursor displaying address be CURS, $CURS=\sum_{n=0}^{7} 2^n CURn$	Set the cursor displaying address by use of CUR7 through CUR0. CUR7 to CUR0 ≥ (11110000) setting is forbidden under 24 characters display. CUR7 to CUR0 ≥ (11100000) setting is forbidden under 32 characters display. Set CUR7 to CUR0 = (11111111) under cursor is not be displayed. The cursor displaying address (CURS) is correspond to display construction.
		1		
1	CUR1	⓪		
		1		
2	CUR2	⓪		
		1		
3	CUR3	⓪		
		1		
4	CUR4	⓪		
		1		
5	CUR5	⓪		
		1		
6	CUR6	⓪		
		1		
7	CUR7	⓪		
		1		
8	CBLINK	⓪	No blinking	The cursor blinking setting
		1	Blinking	
9	$\overline{CL17}$/18	⓪	Cursor displaying at the 17th dot by vertical direction.	Refer to character construction.
		1	Cursor displaying at the 18th dot by vertical direction.	
A	TEST22	⓪	It should be fixed to “0”.	
		1	Can not be used.	
B	RGBON	⓪	Normal	Refer to supplemental explanation (4).
		1	Character background coloring	
C	TEST24	⓪	It should be fixed to “0”.	
		1	Can not be used.	
D	TEST32	⓪	It should be fixed to “0”.	
		1	Can not be used.	

(9) Address F8$_{16}$

<table>
<tr><th rowspan="2">DA
0~D</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">BLK0</td><td>⓪</td><td rowspan="4"><table><tr><th>BLK1</th><th>BLK0</th><th>DSPn= “1”</th><th>DSPn= “0”</th></tr><tr><td>0</td><td>0</td><td>Matrix-outline border size</td><td>Matrix-outline size</td></tr><tr><td>0</td><td>1</td><td>Border size</td><td>Character size</td></tr><tr><td>1</td><td>0</td><td>Matrix-outline size</td><td>Border size</td></tr><tr><td>1</td><td>1</td><td>Character size</td><td>Matrix-outline size</td></tr></table></td><td rowspan="4">Display mode
(BLNK output) variable</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">BLK1</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">EX</td><td>⓪</td><td>External synchronization</td><td rowspan="2">Synchronizing signal switching (Note1)</td></tr>
<tr><td>1</td><td>Internal synchronization</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">SCOR</td><td>⓪</td><td>Superimpose monotone display</td><td rowspan="2">“1” setting is forbidden at internal synchronous or PAL, M-PAL mode displaying.</td></tr>
<tr><td>1</td><td>Superimpose coloring display (only NTSC)</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">STOPIN</td><td>⓪</td><td>fSC input mode</td><td rowspan="2">OSCIN oscillation control</td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">STOP1</td><td>⓪</td><td>Oscillation VCO for display</td><td rowspan="2">Control oscillation VCO for display</td></tr>
<tr><td>1</td><td>Stop oscillation VCO for display</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">DSPON</td><td>⓪</td><td>Display OFF</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Display ON</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">RAMERS</td><td>⓪</td><td>RAM not erased</td><td rowspan="2">This register does not exist (Note 3).</td></tr>
<tr><td>1</td><td>RAM erased</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">EHP0</td><td>⓪</td><td rowspan="10">Let encode data programming start position be EHS,

$EHS = \sum_{n=0}^{4} 2^n EHPn + 6$</td><td rowspan="10">Set encode start position by use of EHP4 through EHP0.

EHP4 to EHP0 = (00000) to (01111) is setting forbidden.

Refer to encode function (3)</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">EHP1</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">EHP2</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">B</td><td rowspan="2">EHP3</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">C</td><td rowspan="2">EHP4</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">D</td><td rowspan="2">LEVEL1</td><td>⓪</td><td>Internal bias OFF</td><td rowspan="2">Generates bias potential for decoding and synchronous separation.</td></tr>
<tr><td>1</td><td>Internal bias ON</td></tr>
</table>

Notes 1. In dealing with the internal synchronization, cut off external video signals outside the IC. The leakage of external input video signals can be avoided.

2. In displaying color superimposition, enter into the OSCIN pin the fSC signal that phase-synchronizes with the color burst of the composite video signals (input to the CVIN pin).

3. Erases all the display RAM. The character code turns to blank-FF$_{16}$, the encode data bit and the blinking bit turn to “1” respectively, and reversed character bit turns to “0”.

Supplemental explanation about display control register

(1) How to effect synchronous separation from composite video signals

Synchronous separation is effected as follows depending on the width of L-level of the vertical synchronous period.

1. Less than 8.4 µs ····· Not to be determined to be a vertical synchronous signal.
2. Equal to or higher than 8.4 µs but less than 15.6 µs ····· When two clocks continue, if take place, it is "L" period is determined to be a vertical synchronization signal.
3. Equal to or higher than 15.6 µs ····· It is "L" period is determined to be a vertical synchronous signal with no condition.

The determination is made at the timing indicated by V in Fig.3 either in case 2 or in case 3.

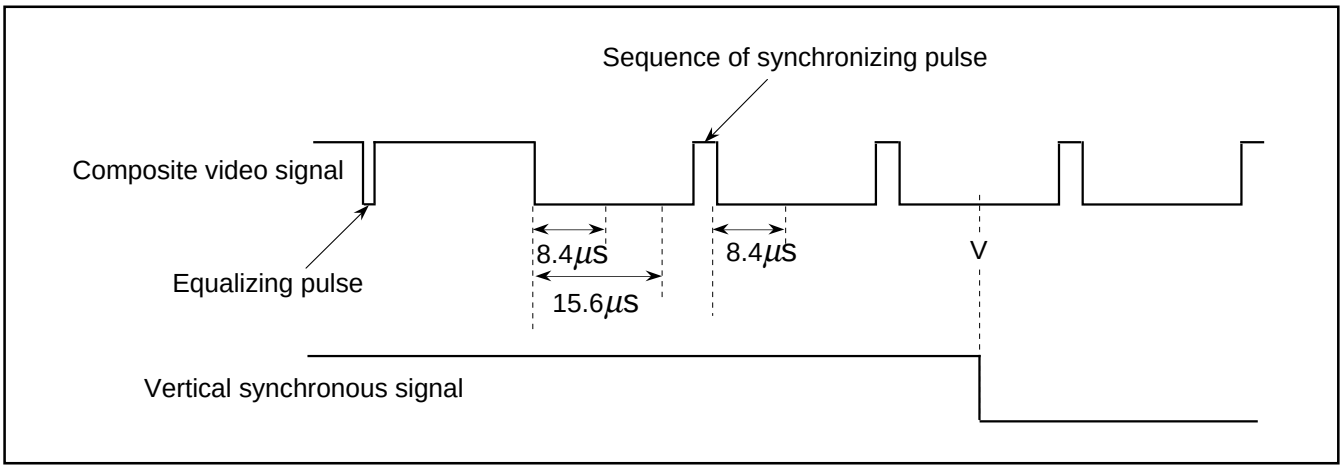


Fig. 4 The method of synchronous separation from composite video signal.

(2) Field definition

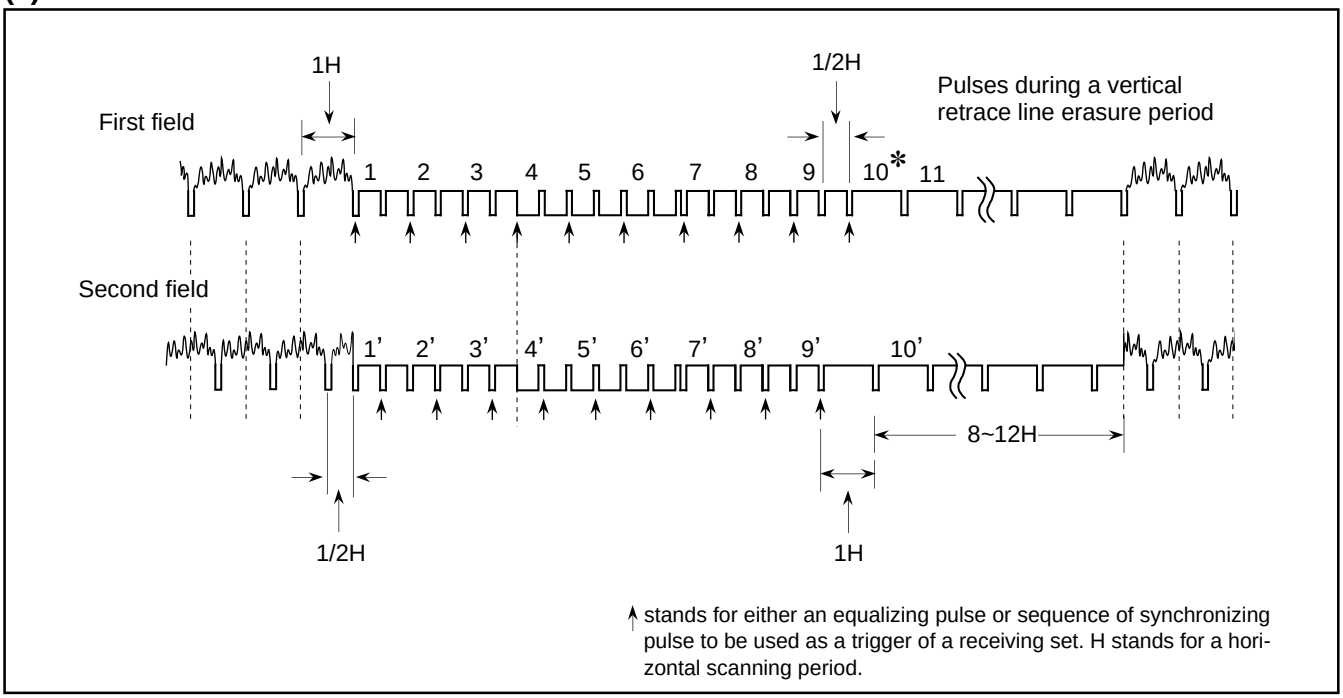


Fig. 5 Field definition

* A horizontal scanning line number corresponds to slice lines DVP4 through DVP0 (address $F1_{16}$) and to encode lines EVP4 through EVP0 (address $F2_{16}$).

(3) Video signal level

V_{DD} : 5.0V, Ta : 25°C

Color	Phase angle (rad)		Brightness level (V)			Amplitude ratio (to color burst)		
	NTSC method	PAL, M-PAL method	Min.	Typ.	Max.	Min.	Typ.	Max.
Sync-chip	—	—	1.3	1.5	1.7	—	—	—
Pedestal	—	—	1.9	2.1	2.3	—	—	—
Color burst	0	± 4π /16	1.9	2.1	2.3	—	1.0	—
Black	—	—	2.1	2.3	2.5	—	—	—
Red	7π /16 ± 2π /16	± 7π /16 ± 2π /16	2.3	2.5	2.7	1.5	3.0	4.5
Green	27π /16 ± 2π /16	∓ 5π /16 ± 2π /16	2.7	2.9	3.1	1.4	2.8	4.2
Yellow	π /16 ± 2π /16	±π /16 ± 2π /16	3.1	3.3	3.5	1.0	2.0	3.0
Blue	17π /16 ± 2π /16	∓15π /16 ± 2π /16	2.0	2.2	2.4	1.0	2.0	3.0
Magenta	11π /16 ± 2π /16	±11π /16 ± 2π /16	2.5	2.7	2.9	1.4	2.8	4.2
Cyan	23π /16 ± 2π /16	∓ 9π /16 ± 2π /16	2.9	3.1	3.3	1.5	3.0	4.5
White	—	—	3.1	3.3	3.5	—	—	—

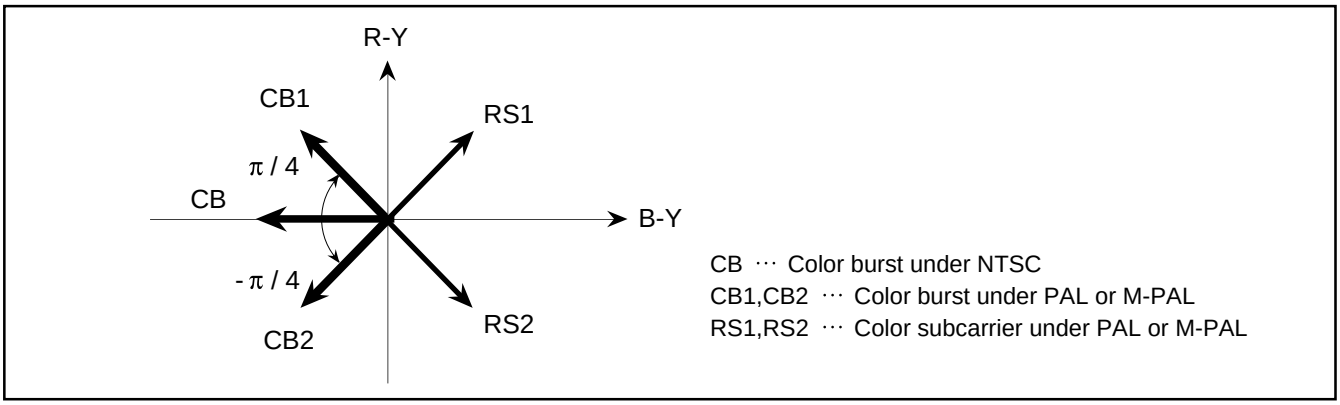


Fig. 6 Bector phases

(4) Setting RGBON (address $F7_{16}$)

a) When encode is off .... EFILD1, 0 (address $F3_{16}$) = 0,0
Encode setting .... Not effected
RGBON = "0" ..... Sets background colors depending on BB, BG, and BR (address $F6_{16}$), screen by screen.
RGBON = "1" ..... Sets background colors depending on EC2 to EC0 (address 00_{16} to EF_{16}), character by character. The color setting is shown below.

b) When encode is on ... EFILD1, 0 (address $F3_{16}$) = 0, 1 or 1, 0
Encode setting .... Sets encode data depending on EC2 through EC0. (Refer to the encode functions for details.)
RGBON = "0" ..... Sets background colors depending on BB, BG and BR (address $F6_{16}$) screen by screen.
RGBON = "1" ..... This setting can not be used.
(When encode is on, setting RGBON to "1" results in setting both encode data and background colors depending on the same memory (EC2 through EC0), so this setting can not be used.

Color Setting

EC2	EC1	EC0	Color
0	0	0	Black
0	0	1	Red
0	1	0	Green
0	1	1	Yellow
1	0	0	Blue
1	0	1	Magenta
1	1	0	Cyan
1	1	1	White

(5) Port output and BLNK1, CO1 output

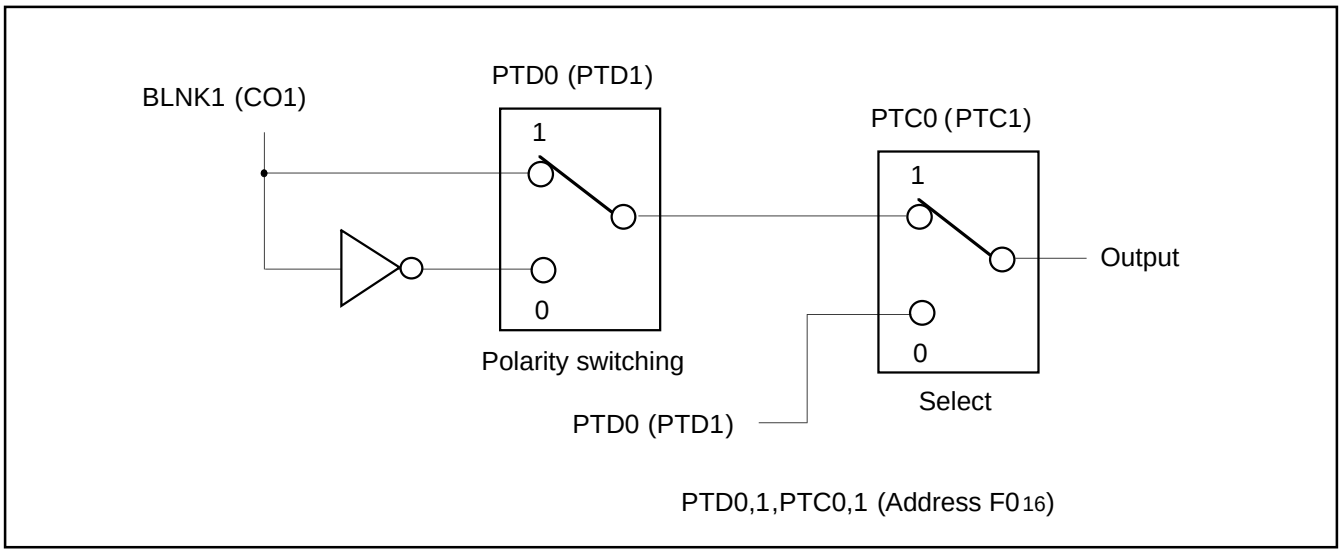


Fig. 7 Example of port control

(6) Setting conditions for oscillating or stopping the display clock

	at display clock operating	at display clock stop
STOP1	0	1
DSPON	1	0
CS pin	L	H

STOP1,DSPON (Address F8$_{16}$)

(7) Setting condition at LEVEL0,1

	Operation state (Character display)		Now-working condition (no characters are displayed)
	Internal synchronous	External synchronous	
LEVEL0	1	1	0
LEVEL1	0	1	0

LEVEL0 (address F6$_{16}$), LEVEL1 (address F8$_{16}$)

DISPLAY FORMS

M35052-XXXSP/FP has the following four display forms as the blanking function, when CO1 and BLNK1 are output.

(1) Character size : Blanking same as the character size.
(2) Border size : Blanking the background as a size from character.
(3) Matrix-outline size: Blanking the background as a size from all character font size.
(4) Matrix-outline border size : Blanking the background as a size from all character font size.
Border display.

This display format allows each line to be controlled independently, so that two kinds of display formats can be combined on the same screen.

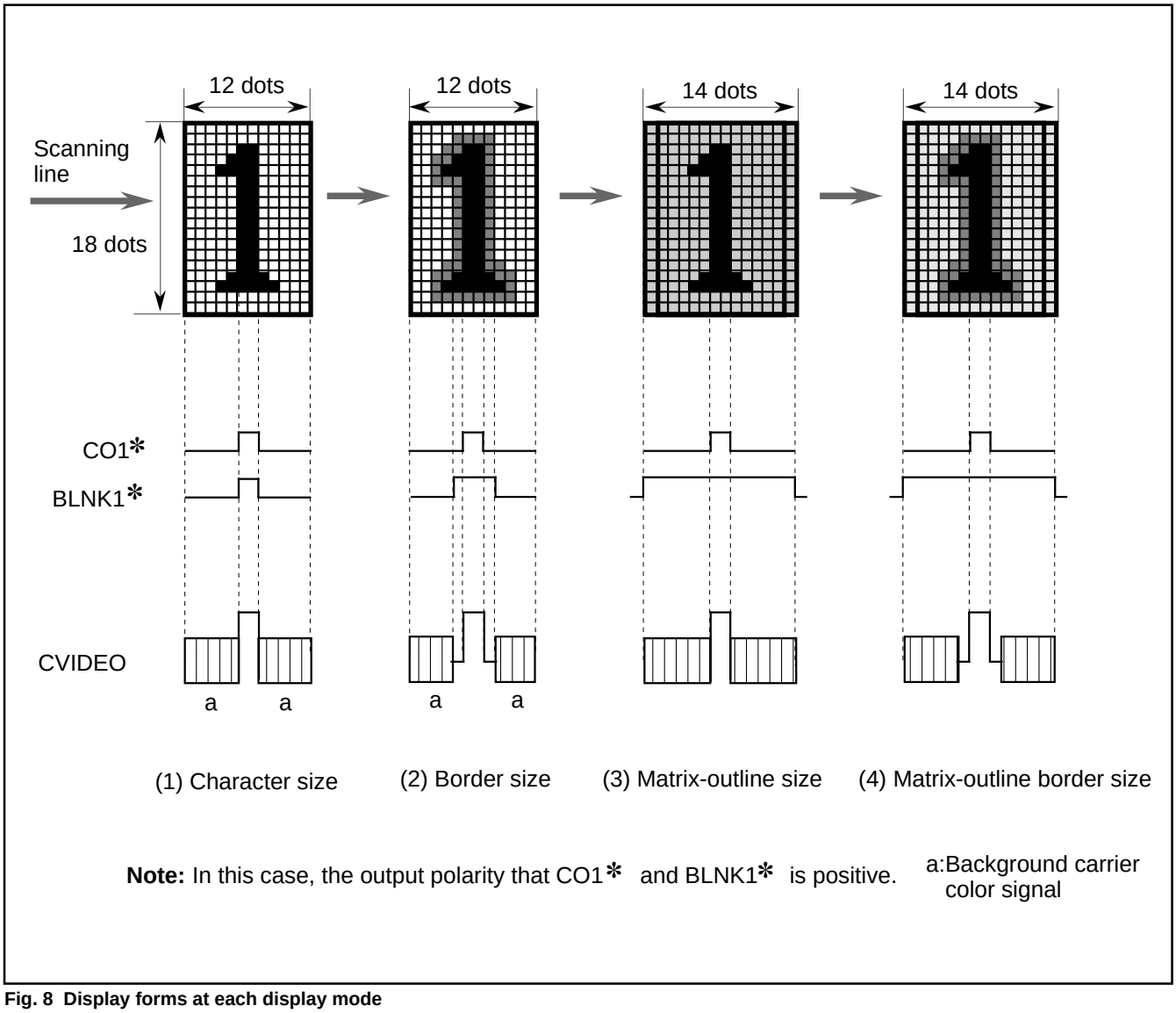


Fig. 8 Display forms at each display mode

DATA INPUT EXAMPLE

Data of display RAM and display control registers can be set by then serial input function. Example of data setting is shown in Figure 9.
Owing to automatic address increment, not necessary to enter addresses for the second and subsequent data.
In automatically, the next of address $F8_{16}$ is assigned to address 00_{16}.
Fig. 9 shows an example of data serially entered.

Address /Data	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Remarks
Address ($F8_{16}$)	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	Specify address
Data ($F8_{16}$)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Display OFF
Data (00_{16})	0	0	0	REV	BLINK	EC2	EC1	EC0	C7	C6	C5	C4	C3	C2	C1	C0	Specify address display RAM 0 to EF_{16}.
Data (01_{16})	0	0	0	REV	BLINK	EC2	EC1	EC0	C7	C6	C5	C4	C3	C2	C1	C0	
≀	≀								≀								
Data (EE_{16})	0	0	0	REV	BLINK	EC2	EC1	EC0	C7	C6	C5	C4	C3	C2	C1	C0	
Data (EF_{16})	0	0	0	REV	BLINK	EC2	EC1	EC0	C7	C6	C5	C4	C3	C2	C1	C0	
Data ($F0_{16}$)	0	0	0	$\overline{W}$/R	0	1	0	0	1	0	0	0	PTD 1	PTD 0	PTC 1	PTC 0	Specify address register $F0_{16}$ to $F7_{16}$.
Data ($F1_{16}$)	0	0	0	DVP 4	DVP 3	DVP 2	DVP 1	DVP 0	HP 7	HP 6	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0	
Data ($F2_{16}$)	0	0	0	EVP 4	EVP 3	EVP 2	EVP 1	EVP 0	VP 7	VP 6	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0	
Data ($F3_{16}$)	0	0	0	$\overline{D}$/V	EFLD 1	EFLD 0	DFLD 1	DFLD 0	VSZ 21	VSZ 20	VSZ 11	VSZ 10	HSZ 21	HSZ 20	HSZ 11	HSZ 10	
Data ($F4_{16}$)	0	0	0	0	0	SPACE	DSP 9	DSP 8	DSP 7	DSP 6	DSP 5	DSP 4	DSP 3	DSP 2	DSP 1	DSP 0	
Data ($F5_{16}$)	0	0	0	0	$\overline{MB}$/LB	0	0	0	EQP	PALH	MPAL	$\overline{INT}$ /NON	$\overline{N}$/P	BLINK 2	BLINK 1	BLINK 0	
Data ($F6_{16}$)	0	0	1	0	0	0	LBLACK	$\overline{LIN}$ 24/32	BLKHF	BB	BG	BR	LEVEL 0	PHASE 2	PHASE 1	PHASE 0	
Data ($F7_{16}$)	0	0	0	0	RGBON	0	$\overline{CL}$ 17/18	CBLINK	CURS 7	CURS 6	CURS 5	CURS 4	CURS 3	CURS 2	CURS 1	CURS 0	
Data ($F8_{16}$)	0	0	LEVEL 1	EHP 4	EHP 3	EHP 2	EHP 1	EHP 0	RAM ERS	DSPON	STOP 1	STOP IN	SCOR	EX	BLK 1	BLK 0	Display ON

Fig. 9 Example of data setting by the serial input function

SERIAL DATA INPUT TIMING

(1) The address consists of 16 bits.
(2) The data consists of 16 bits.
(3) The 16 bits in the SCK after the $\overline{CS}$ signal has fallen are the address, and for succeeding input data, the address is incremented every 16 bits.

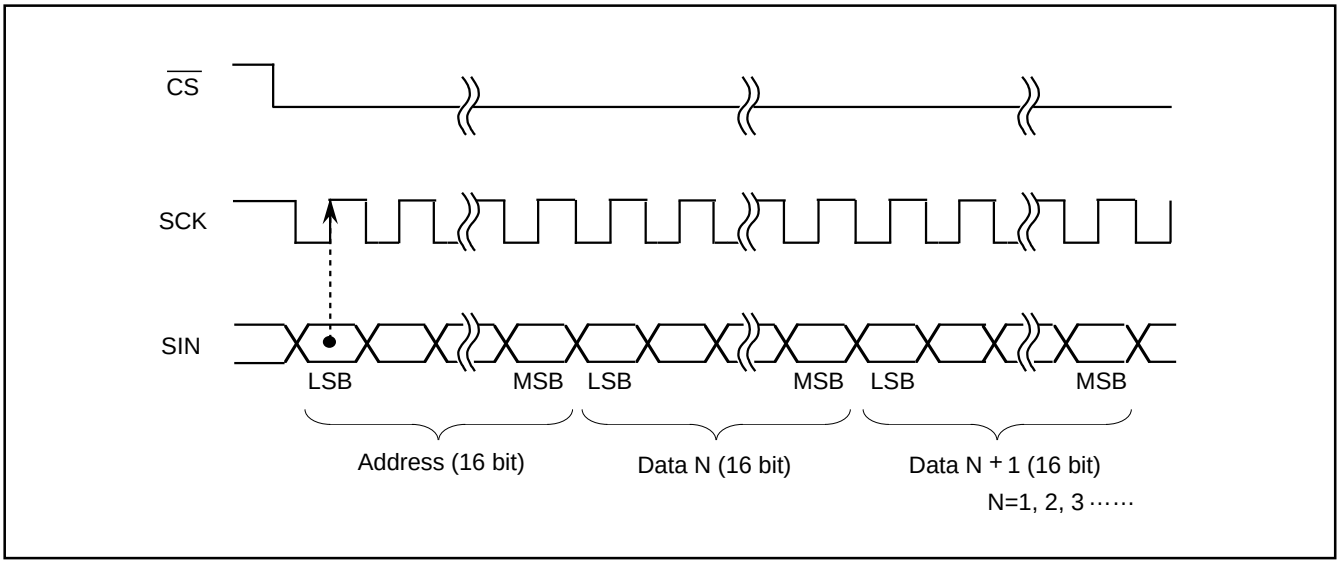


Fig. 10 Serial input timing

Output timing of decode data

(1) Setting "1" in the $\overline{W}$/R register activates output mode.
(2) Outputs decode data in 16 clocks of the SCK after switching over to output mode. (Don't enter the SCK for more than 16 clocks.)
(3) Raising the $\overline{CS}$ signal deactivates output mode.
(To switch over to input mode, cause $\overline{CS}$ to fall.)
(4) If no data are present, or if data have already been read, 0000_{16} is output.

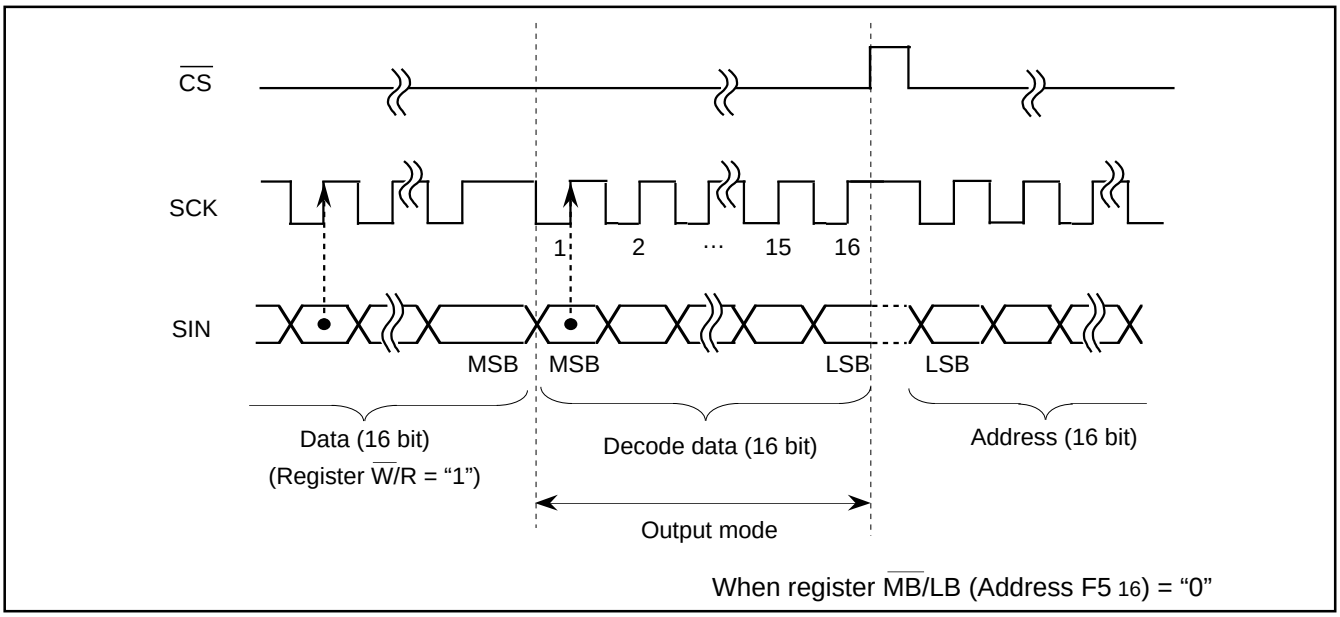


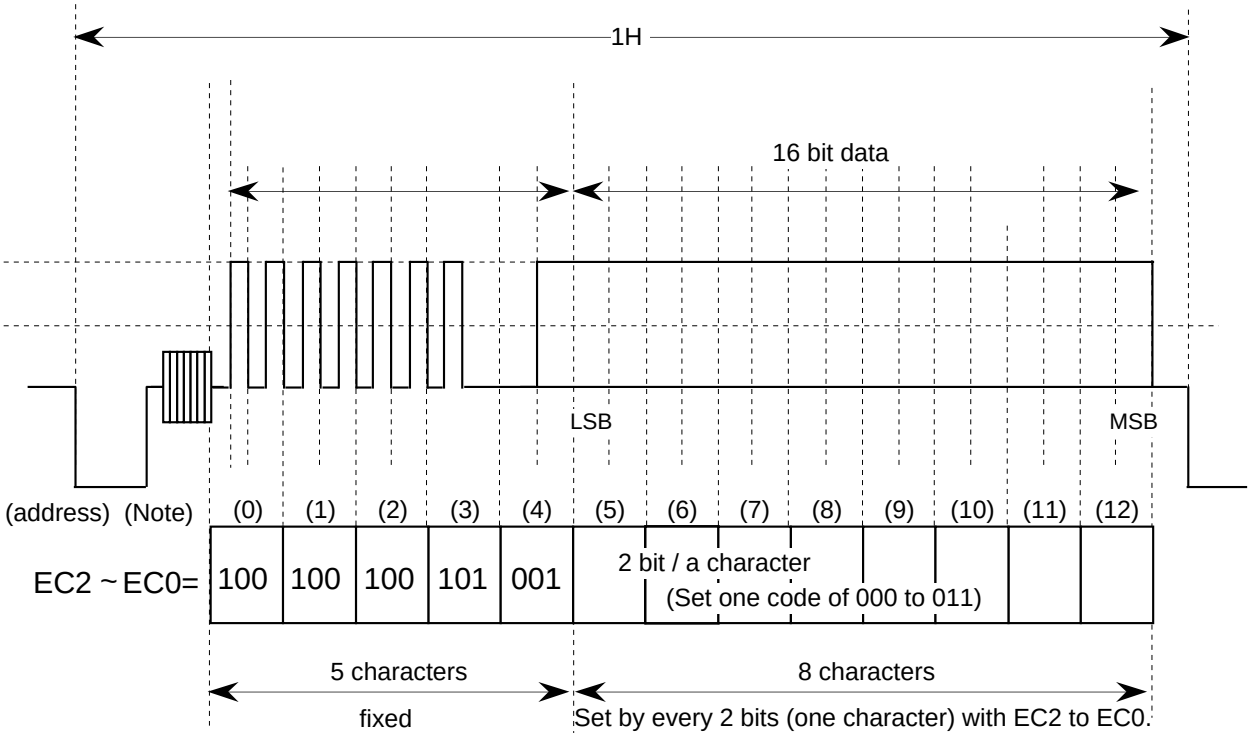
Fig. 11 Decode data output timing

Encode functions (effective for NTSC only)

(1) Setting encode data

Setting data code (000 – 111) in EC0 through EC2 (bits DA8 through DAA) of the display RAM (addresses 0 through EF_{16}) encodes. A sample setting and data code are shown below.

An example of setting



A suite of data code (000 – 111) for encoding to be set in EC2 through EC0 are assigned as given below.

EC2	EC1	EC0	Data
0	0	0	L L
0	0	1	L H
0	1	0	H L
0	1	1	H H
1	0	0	L H L H
1	0	1	L H L } 18 dots
1	1	0	Can not be used
1	1	1	No encoding

12 dots

(The oscillation frequency when encoding: 3 MHz✻
1 clock cycle: 0.333μs
1 character (12 dots): 3.996μs
2 bits/1 character: 3.996μs
1 bit: 1.998μs)

✻····· 192× f_H (horizontal synchronous frequency)
for f_H = 15.625 kHz

Note: Refer to the next page about address setting.

Fig. 12 An example of data code setting

(2) Setting addresses

Set encode data in EC0 through EC2 of addresses (that correspond to an extent from the first character to the thirteenth character in each line as appearing on the screen.) Set “111” to EC2 through EC0 of all the addresses in which you set no encode data.

Screen

	The first character ..... The 13th character													The 13th character ..... The 24th character									
line 1	00_{16}	01_{16}	02_{16}	03_{16}	04_{16}	05_{16}	06_{16}	07_{16}	08_{16}	09_{16}	$0A_{16}$	$0B_{16}$	$0C_{16}$	$0D_{16}$	$0E_{16}$	$0F_{16}$	10_{16}	11_{16}	12_{16}	13_{16}	14_{16}	15_{16}	16_{16}	17_{16}
line 2	18_{16}	19_{16}	$1A_{16}$	$1B_{16}$	$1C_{16}$	$1D_{16}$	$1E_{16}$	$1F_{16}$	20_{16}	21_{16}	22_{16}	23_{16}	24_{16}	25_{16}	26_{16}	27_{16}	28_{16}	29_{16}	$2A_{16}$	$2B_{16}$	$2C_{16}$	$2D_{16}$	$2E_{16}$	$2F_{16}$
line 3	30_{16}	31_{16}	32_{16}	33_{16}	34_{16}	35_{16}	36_{16}	37_{16}	38_{16}	39_{16}	$3A_{16}$	$3B_{16}$	$3C_{16}$	$3D_{16}$	$3E_{16}$	$3F_{16}$	40_{16}	41_{16}	42_{16}	43_{16}	44_{16}	45_{16}	46_{16}	47_{16}
line 4	48_{16}	49_{16}	$4A_{16}$	$4B_{16}$	$4C_{16}$	$4D_{16}$	$4E_{16}$	$4F_{16}$	50_{16}	51_{16}	52_{16}	53_{16}	54_{16}	55_{16}	56_{16}	57_{16}	58_{16}	59_{16}	$5A_{16}$	$5B_{16}$	$5C_{16}$	$5D_{16}$	$5E_{16}$	$5F_{16}$
line 5	60_{16}	61_{16}	62_{16}	63_{16}	64_{16}	65_{16}	66_{16}	67_{16}	68_{16}	69_{16}	$6A_{16}$	$6B_{16}$	$6C_{16}$	$6D_{16}$	$6E_{16}$	$6F_{16}$	70_{16}	71_{16}	72_{16}	73_{16}	74_{16}	75_{16}	76_{16}	77_{16}
line 6	78_{16}	79_{16}	$7A_{16}$	$7B_{16}$	$7C_{16}$	$7D_{16}$	$7E_{16}$	$7F_{16}$	80_{16}	81_{16}	82_{16}	83_{16}	84_{16}	85_{16}	86_{16}	87_{16}	88_{16}	89_{16}	$8A_{16}$	$8B_{16}$	$8C_{16}$	$8D_{16}$	$8E_{16}$	$8F_{16}$
line 7	90_{16}	91_{16}	92_{16}	93_{16}	94_{16}	95_{16}	96_{16}	97_{16}	98_{16}	99_{16}	$9A_{16}$	$9B_{16}$	$9C_{16}$	$9D_{16}$	$9E_{16}$	$9F_{16}$	$A0_{16}$	$A1_{16}$	$A2_{16}$	$A3_{16}$	$A4_{16}$	$A5_{16}$	$A6_{16}$	$A7_{16}$
line 8	$A8_{16}$	$A9_{16}$	AA_{16}	AB_{16}	AC_{16}	AD_{16}	AE_{16}	AF_{16}	$B0_{16}$	$B1_{16}$	$B2_{16}$	$B3_{16}$	$B4_{16}$	$B5_{16}$	$B6_{16}$	$B7_{16}$	$B8_{16}$	$B9_{16}$	BA_{16}	BB_{16}	BC_{16}	BD_{16}	BE_{16}	BF_{16}
line 9	$C0_{16}$	$C1_{16}$	$C2_{16}$	$C3_{16}$	$C4_{16}$	$C5_{16}$	$C6_{16}$	$C7_{16}$	$C8_{16}$	$C9_{16}$	CA_{16}	CB_{16}	CC_{16}	CD_{16}	CE_{16}	CF_{16}	$D0_{16}$	$D1_{16}$	$D2_{16}$	$D3_{16}$	$D4_{16}$	$D5_{16}$	$D6_{16}$	$D7_{16}$
line 10	$D8_{16}$	$D9_{16}$	DA_{16}	DB_{16}	DC_{16}	DD_{16}	DE_{16}	DF_{16}	$E0_{16}$	$E1_{16}$	$E2_{16}$	$E3_{16}$	$E4_{16}$	$E5_{16}$	$E6_{16}$	$E7_{16}$	$E8_{16}$	$E9_{16}$	EA_{16}	EB_{16}	EC_{16}	ED_{16}	EE_{16}	EF_{16}

Using area for encode data setting

Useless area

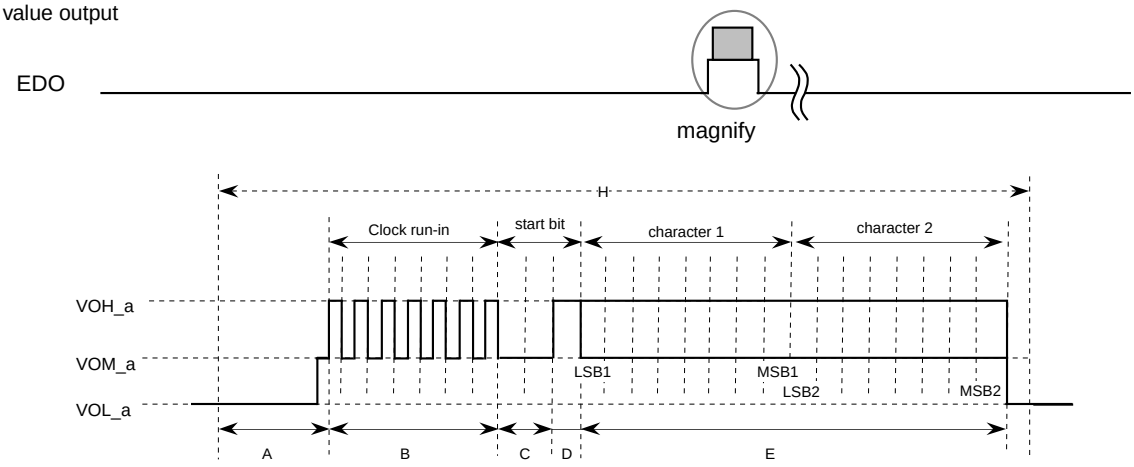
Start setting data from the first line. Data set in the lines specified by registers EVP0 through EVP3 (address $F2_{16}$) will be encoded.
Setting data in the second and subsequent lines, it is possible to set encode data to ten consecutive lines from those secified by registers EVP0 to EVP2.
Similarly to encode line N specified by registers EVP0 through EVP2, extending encode lines to line N-1 and to line N+1, it is possible to read encode data more certainly.

Fig.13 Display monitor

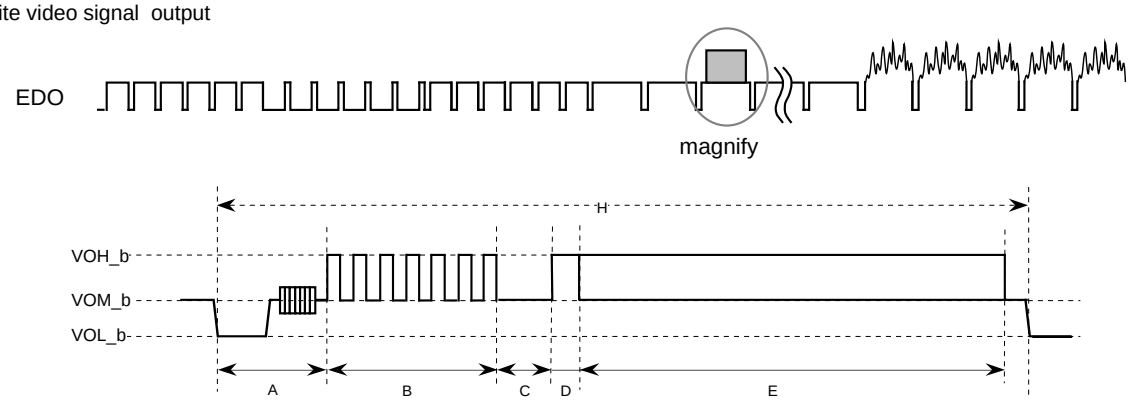
(3) Encode data output

Control encode data (EDO) output by register D/V (address F3$_{16}$)

a) Register D/V (address F3$_{16}$)="0"
Digital 3 value output



b) Register D/V (address F3$_{16}$)="1"
Composite video signal output



VDD : 5.0V, Ta : 25°C

Symbol		Min.	Typ.	Max.	Unit
A		—	(EHS+9)×1/(fH×192)✵	—	μs
B		—	6.5P	—	μs
C		—	2P	—	μs
D		—	1P	—	μs
E		—	16P	—	μs
H		—	1/fH	—	μs
(a)	VOH_a	—	5.0	—	V
	VOM_a	0.4	2.3	4.0	V
	VOL_a	—	0	—	V
(b)	VOH_b	3.1	3.3	3.5	V
	VOM_b	1.9	2.1	2.3	V
	VOL_b	1.3	1.5	1.7	V

1P=1/(fH×32)
fH : Horizontal synchronous frequency(MHz)

✵ It is possible to make a fine adjustment (EHS=16 to 31. 16 settings. in increments of 1/(fH × 192)) by use of EHS (registers EHP4 to EHP0 of address F8$_{16}$).
(EHS≤15 setting is forbidden.)

Fig. 14 Encode data output

CHARACTER FONT

Images are composed on a 12 × 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

Character code "FF16" is so fixed as to be blank and to have no background, thus cannot assign a character font to this code.

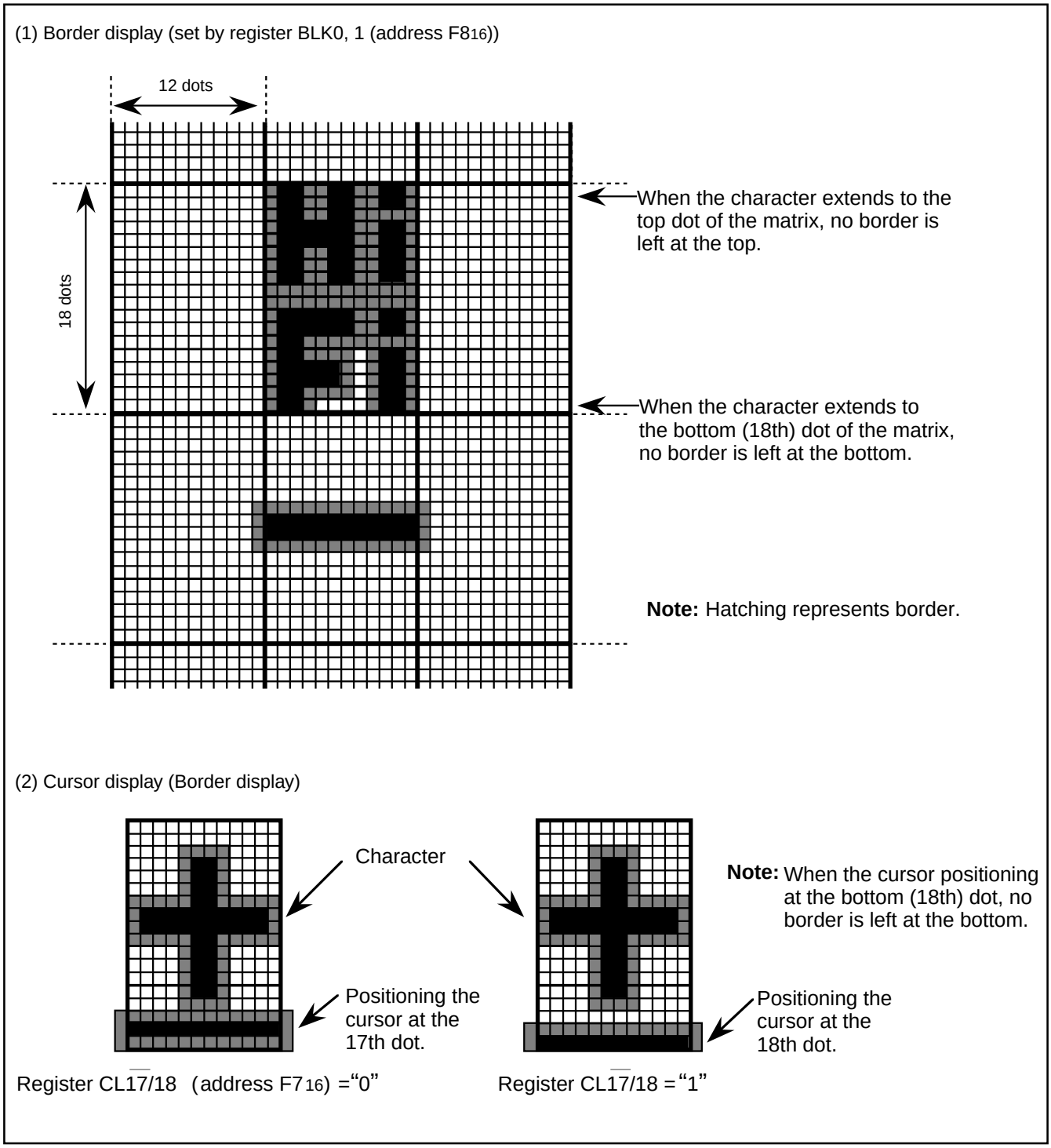


Fig. 15 Character font and border

Precautions

(1) Points to note in setting the display RAMs

a) Be careful to the edges may sway depending on the combination of character's background color and raster color.

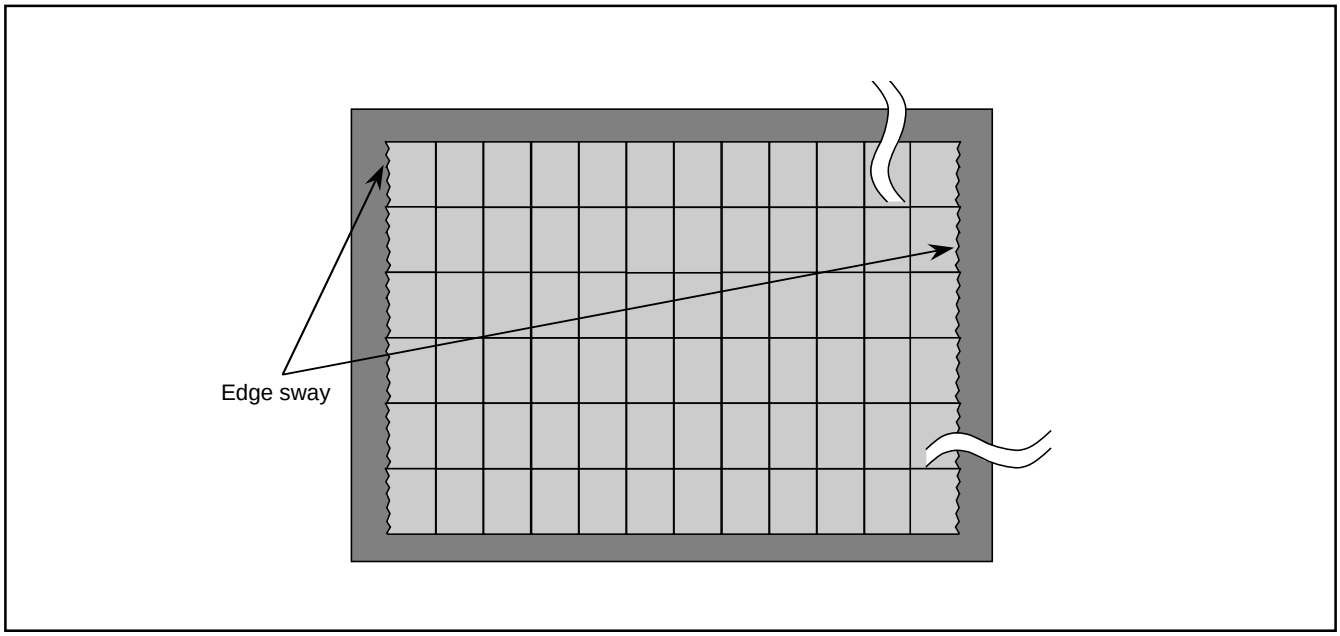


Fig. 16 Example of display

b) If what display exceeds the display area in dealing with external synchronization, (if use double - size characters), set the character code of the addresses lying outside that display area blank code – "FF_{16}".

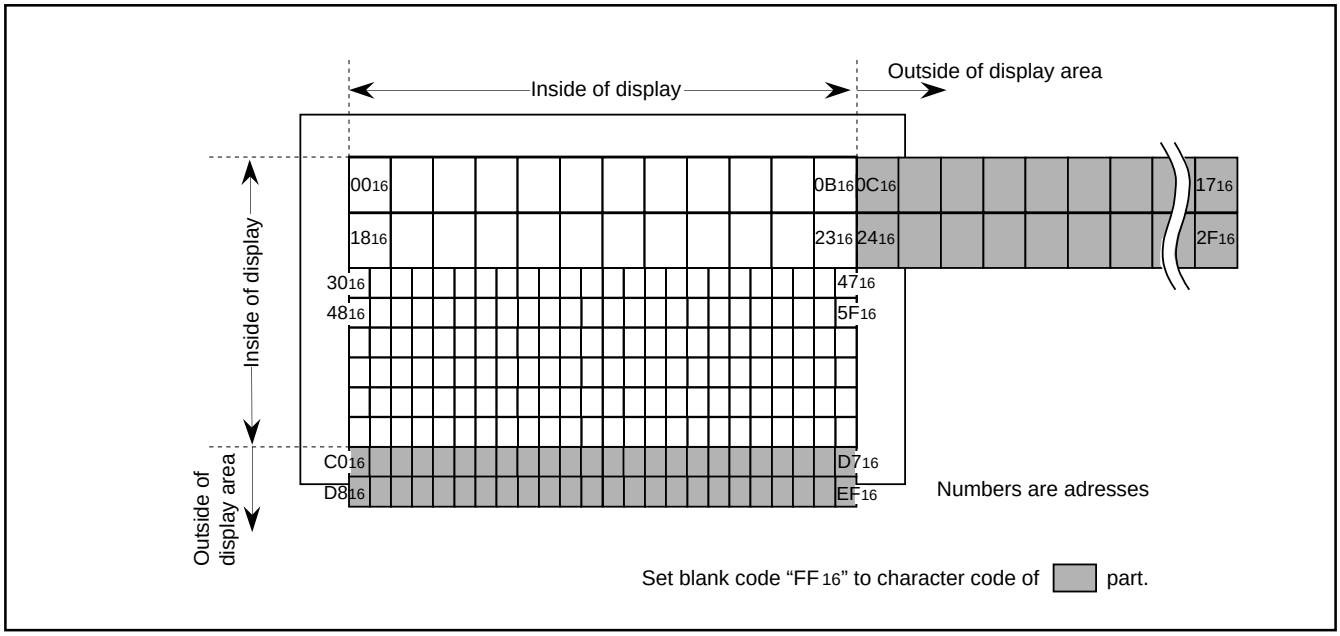


Fig. 17 Example of display

(2) Before setting registers at the starting of system, be sure to reset the M35052-XXXSP/FP by applying "L" level to the $\overline{AC}$ pin.

(3) Power supply noise

When power supply noise is generated, the internal oscillator circuit does not stabilize, whereby causing horizontal jitters across the picture display. Therefore, connect a bypass capacitor between the power supply and GND.

(4) Synchronous correction action

When switching channel or in the special playback mode (quick playback, rewinding, and so on) of VTR, effect of synchronous correction becomes strong, and distortion of a character is apt to occur because the continuity of video signal is suddenly switched. When the continuity of video signal is out of order, erasure of displayed characters is recommended in a extreme short time to raise the quality of displayed characters.

(5) Notes on fSC signal input

This IC amplifies the subcarrier frequency (fSC) signal (NTSC, M-PAL system: 3.58MHz, PAL system: 4.43MHz) input to the OSCIN pin (17-pin) and generates the composite video signal internally. The amplified fSC signal can be destabilized in the following cases.

a) When the fSC signal is outside of recommended operating conditions.
b) When the waveform of the fSC signal is distorted.
c) When DC level in the fSC waveform fluctuates.

When the amplified signal is unstable, the composite video signal generated inside the IC is also unstable in terms of synchronization with the subcarrier and phase.

Consequently, this results in color flicker and lost synchronization when the composite video signal is generated. Make note of the fact that this may prevent a stable blue background from being formed.

(6) Forbidding to stop entering the fSC signal

This IC doesn't properly work if the fSC signal is not entered into the OSCIN pin (pin 17), so don't stop the fSC signal so as to work the IC. To stop the IC, turn the display off (set 0 in the register DSPON (address $F8_{16}$).)

(7) Forbidding to set data during the period in which the internal oscillation circuit stabilizes

a) To start entering the fSC signal when its input is stopped.
b) To start oscillating the oscillation circuit for display when its oscillation is stopped. (to assign "1" to the register STOP1 (address $F8_{16}$) when it is assigned "0", or the like.)
c) To turn on the internal bias when it is turned off. (to assign "1" to the register LEVEL1 (address $F8_{16}$) when it is assigned "0".)

There can be instances in which data are not properly set in the registers until the internal oscillation circuit stabilizes, so follow the steps in sequence as given below.

1) Set "0" in the register DSPON (address $F8_{16}$). (the display is turned off)
2) Effect the settings a), b), and c) given above.
3) Wait 20 ms (the period necessary for the internal oscillation circuit to stabilize) before entering data.
4) Set necessary data in other registers, and make the display RAM ready.

M35053-XXXSP/FP PERIPHERAL CIRCUIT

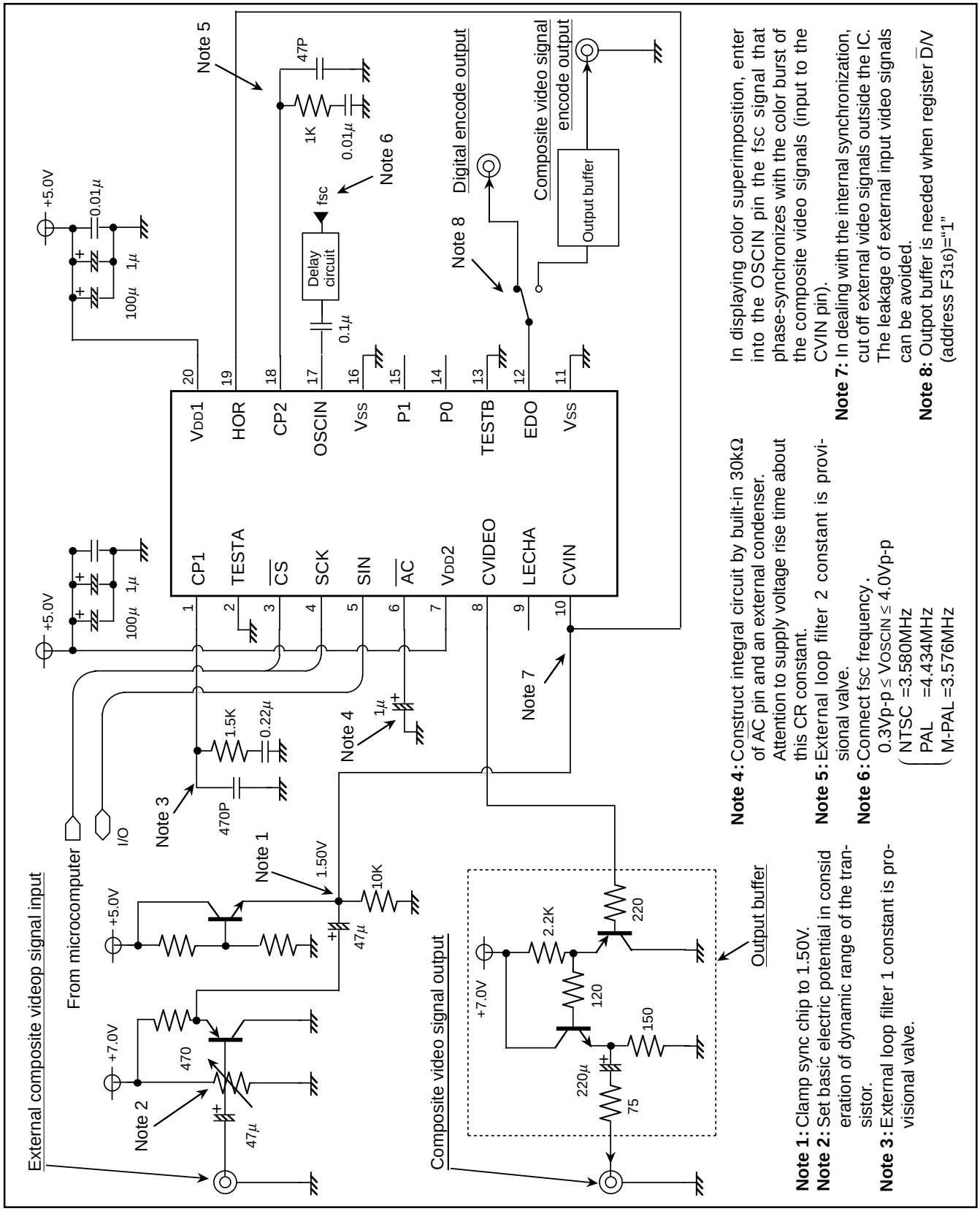


Fig. 18 M35053-XXXSP/FP example of peripheral circuit

TIMING REQUIREMENTS (Ta = –20°C to 70°C, V_{DD} = 5±0.25V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw(SCK)	SCK width	400	–	–	ns
tsu($\overline{CS}$)	$\overline{CS}$ setup time	200	–	–	ns
th(CS)	$\overline{CS}$ hold time	2	–	–	μs
tsu(SIN)	SIN setup time	200	–	–	ns
th(SIN)	SIN hold time	200	–	–	ns
tword	1 word writing time	12.8	–	–	μs

Note. When oscillation stop at register STOR1 (address $F8_{16}$), 1V (field term) or more of $t_{SU(\overline{CS})}$ and $t_{h(\overline{CS})}$ are needed.

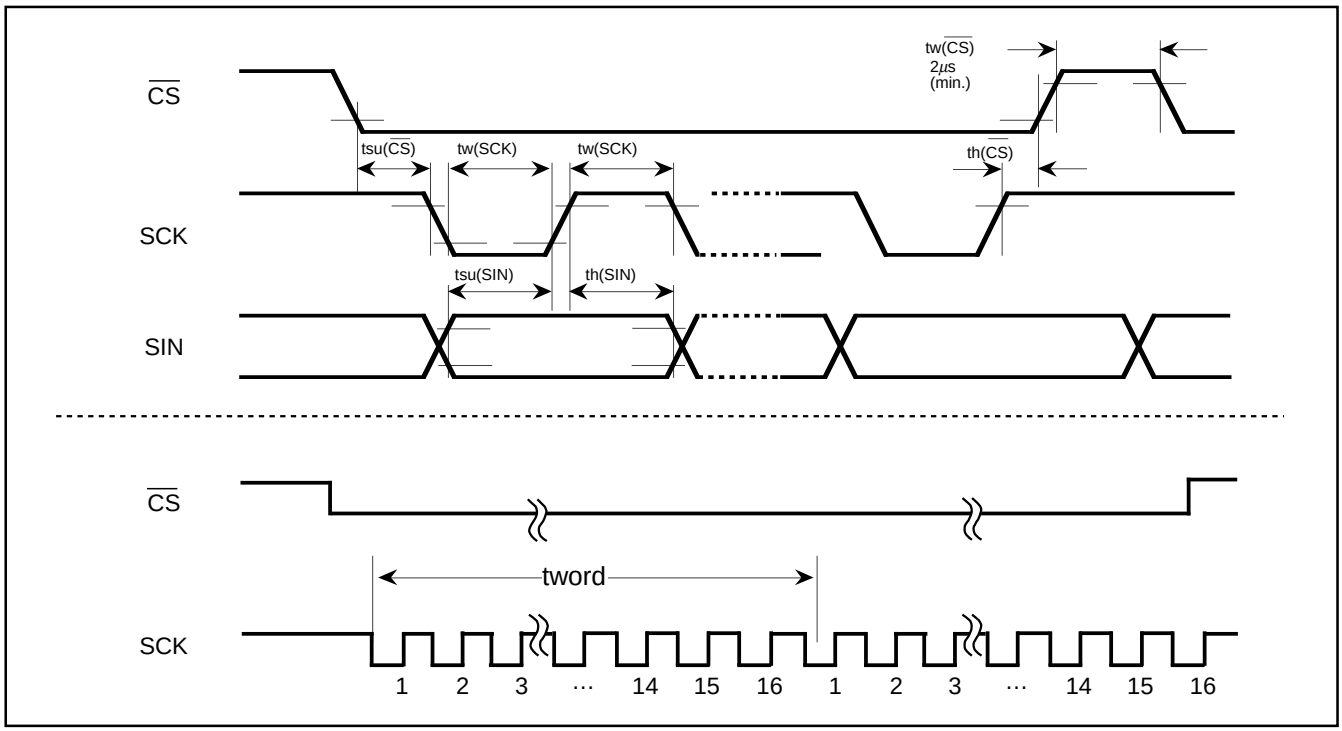


Fig. 19 Serial input timing requirements

ABSOLUTE MAXIMUM RATINGS (V_{DD} = 5V, Ta = –20 to 70°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	–0.3~6.0	V
V_I	Input voltage		V_{SS}–0.3≤V_I≤V_{DD}+0.3	V
V_O	Output voltage		V_{SS}≤V_O≤V_{DD}	V
Pd	Power dissipation	Ta=25°C	300	mW
Topr	Operating temperature		–20~70	°C
Tstg	Storage temperature		–40~125	°C

RECOMMENDED OPERATING CONDITIONS (V_{DD} = 5V, Ta = –20 to 70°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage		4.75	5.00	5.25	V
V_{IH}	"H"level input voltage $\overline{AC}$, $\overline{CS}$, SIN, SCK, TESTA, TESTB		0.8×V_{DD}	V_{DD}	V_{DD}	V
V_{IL}	"L" level input voltage $\overline{AC}$, $\overline{CS}$, SIN, SCK, TESTA, TESTB		0	0	0.2×V_{DD}	V
V_{CVIN}	CVIN, HOR		–	2.0V_{P-P}	–	V
V_{OSCIN}	Input voltage OSCIN (Note 1)		0.3V_{P-P}	–	4.0V_{P-P}	V
f_{OSCIN}	Synchronous signal oscillation frequency (Duty 40~60%)		–	3.580 4.434 3.576	–	MHz
f_{OSC1}	Display oscillation frequency	24 characters×10 lines	–	480×f_H (Note 2)	–	MHz
f_{OSC2}		32 characters×7 lines	–	640×f_H (Note 2)	–	MHz

Notes 1. Noise component is within 30mV.
2. f_H: Horizontal synchronous frequency (MHz).

ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	Ta=–20~70°C	4.75	5.00	5.25	V
I_{DD}	Supply current	V_{DD}=5.00V	–	30	50	mA
V_{OH}	"H"level output voltage P0, P1, SIN	V_{DD}=4.75V, I_{OH}=–0.4mA	3.75	–	–	V
V_{OL}	"L" level output voltage P0, P1, SIN	V_{DD}=4.75V, I_{OL}=0.4mA	–	–	0.4	V
R_I	Pull-up resistance $\overline{AC}$, $\overline{CS}$, SCK, SIN, TESTB	V_{DD}=5.00V	10	30	100	kΩ
V_{OH_a}	"H" level output voltage EDO	V_{DD}=5.00V, I_{OH}=–0.04mA	4.0	–	–	V
V_{OM_a}	"M"level output voltage EDO	V_{DD}=5.00V, I_{OM}=±0.04mA	0.4	2.3	4.0	V
V_{OL_a}	"L" level output voltage EDO	V_{DD}=5.00V, I_{OL}=0.04mA	–	–	0.4	V

VIDEO SIGNAL INPUT CONDITIONS (V_{DD} = 5V, Ta = –20 to 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$V_{IN\text{-}SC}$	Composite video signal input clamp voltage	Sync-chip voltage	–	1.5	–	V

Note for Supplying Power

(1) Timing of power supplying to $\overline{AC}$ pin

The internal circuit of M35052-XXXSP/FP is reset when the level of the auto clear input pin $\overline{AC}$ is "L". This pin is hysteresis input with the pull-up resistor. The timing about power supplying of $\overline{AC}$ pin is shown in Figure 20. tw is the interval after the supply voltage becomes 0.8 × V_{DD} or more and before the supply voltage to the $\overline{AC}$ pin ($V_{\overline{AC}}$) becomes 0.2 × V_{DD} or more.

After supplying the power (V_{DD} and V_{SS}) to M35052-XXXSP/FP, the tw time must be reserved for 1ms or more. Before starting input from the microcomputer, the waiting time (ts) must be reserved for 500ms after the supply voltage to the $\overline{AC}$ pin becomes 0.8 × V_{DD} or more.

(2) Timing of power supplying to $V_{DD}1$ pin and $V_{DD}2$ pin

The power need to supply to $V_{DD}1$ and $V_{DD}2$ at a time, though it is separated perfectly between the $V_{DD}1$ as the digital line and the $V_{DD}2$ as the analog line.

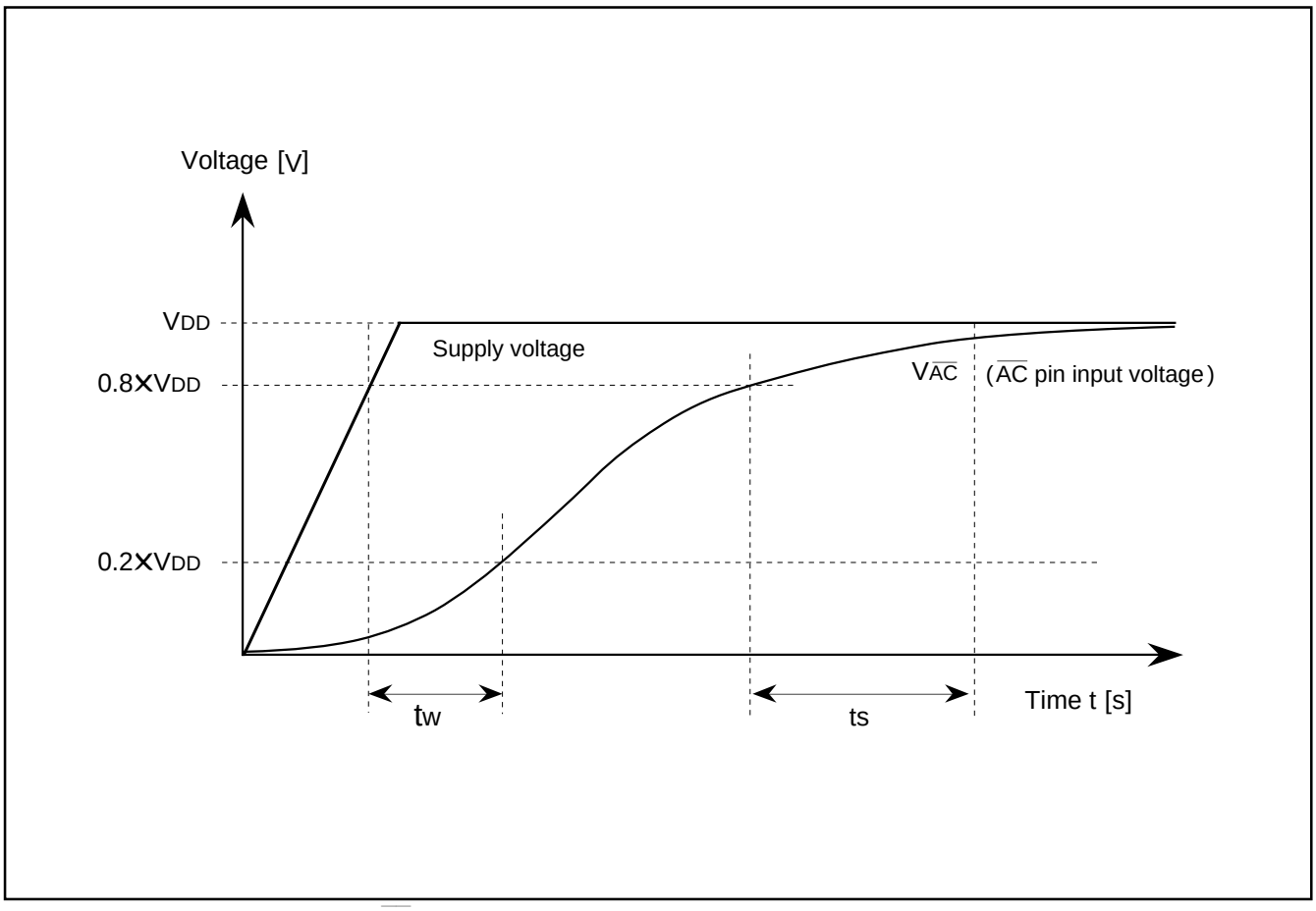


Fig. 20 Timing of power supplying to $\overline{AC}$ pin

PRECAUTION FOR USE

Notes on noise and latch-up

Connect a capacitor (approx. 0.1 µF) between pins V_{DD} and V_{SS} at the shortest distance using relatively thick wire to prevent noise and latch up.

ROM ORDERING METHOD

Please submit the information described below when ordering Mask ROM.

(1) ROM Order Confirmation Form 1
(2) Data to be written into mask ROM ..... EPROM (three sets containing the identical data)
(3) Mark Specification Form 1
(4) Program for character font generating + froppy disk in which character data is input

STANDARD ROM TYPE : M35053-001SP/FP

M35053-001SP/FP is a standard ROM type of M35053-XXXSP/FP character patterns are fixed to the contents of Figure 21 to 24.

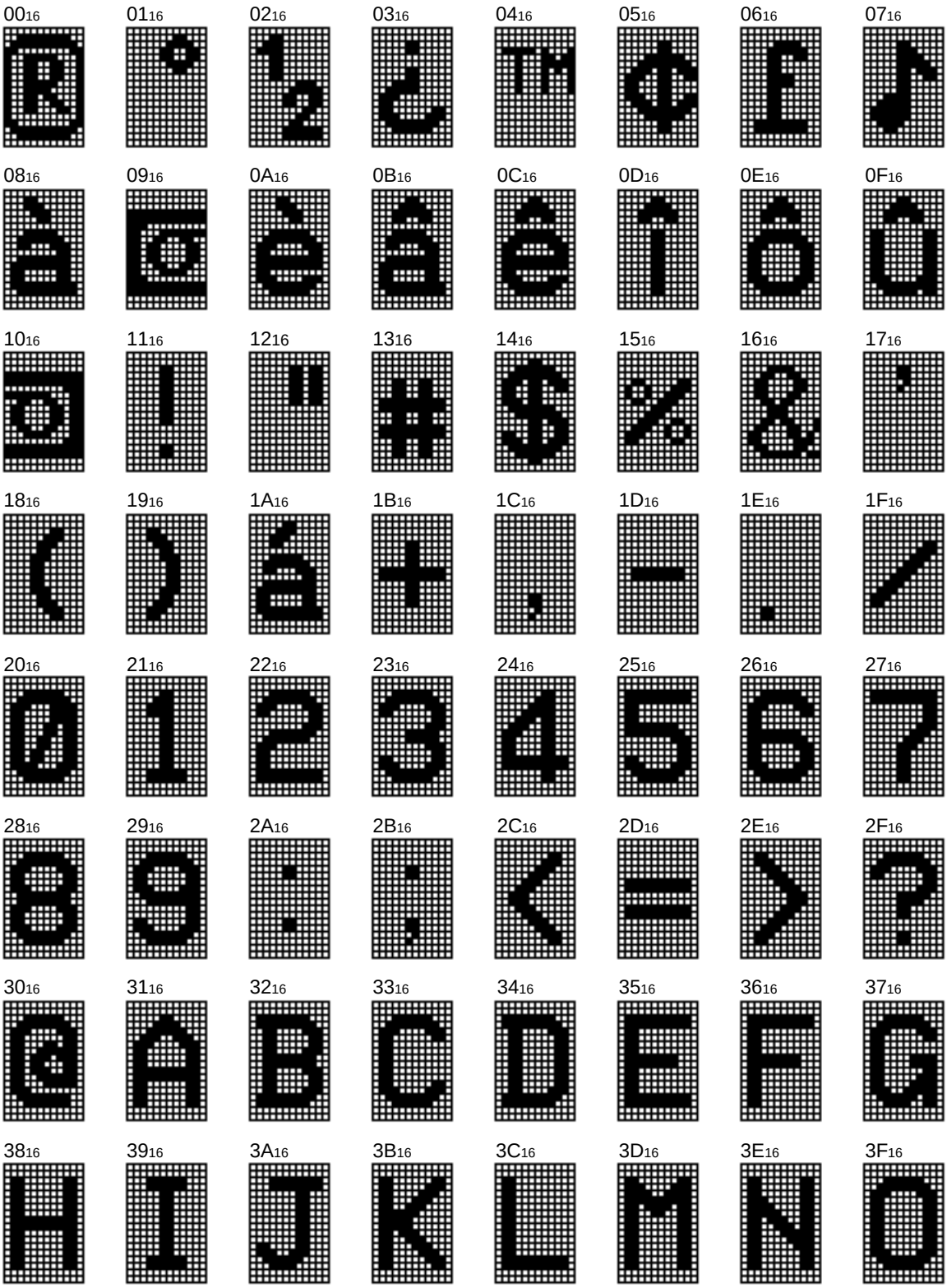


Fig. 21 M35053-001SP/FP character pattern (1)

Fig. 22 M35053-001SP/FP character pattern (2)

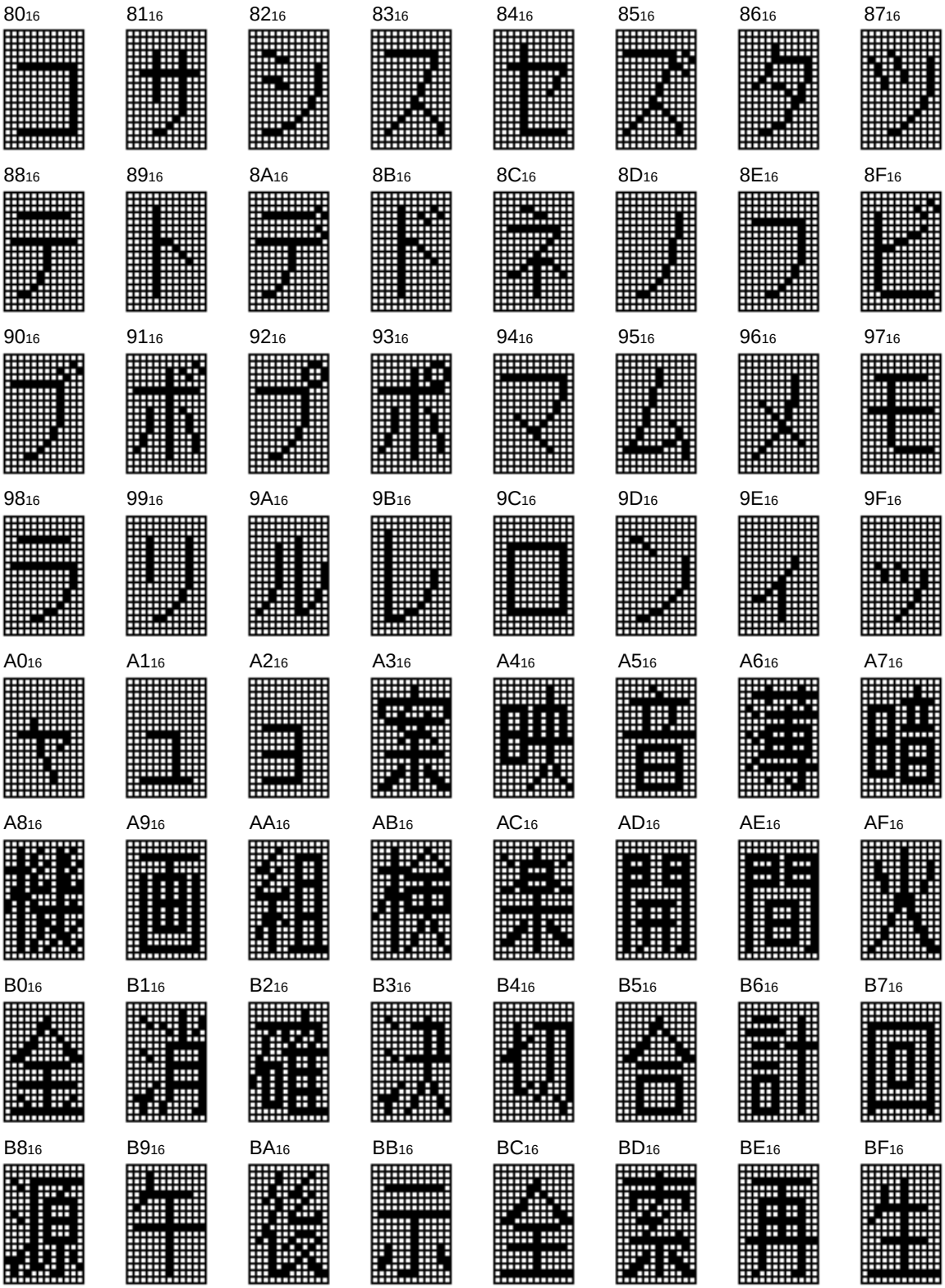


Fig. 23 M35053-001SP/FP character pattern (3)

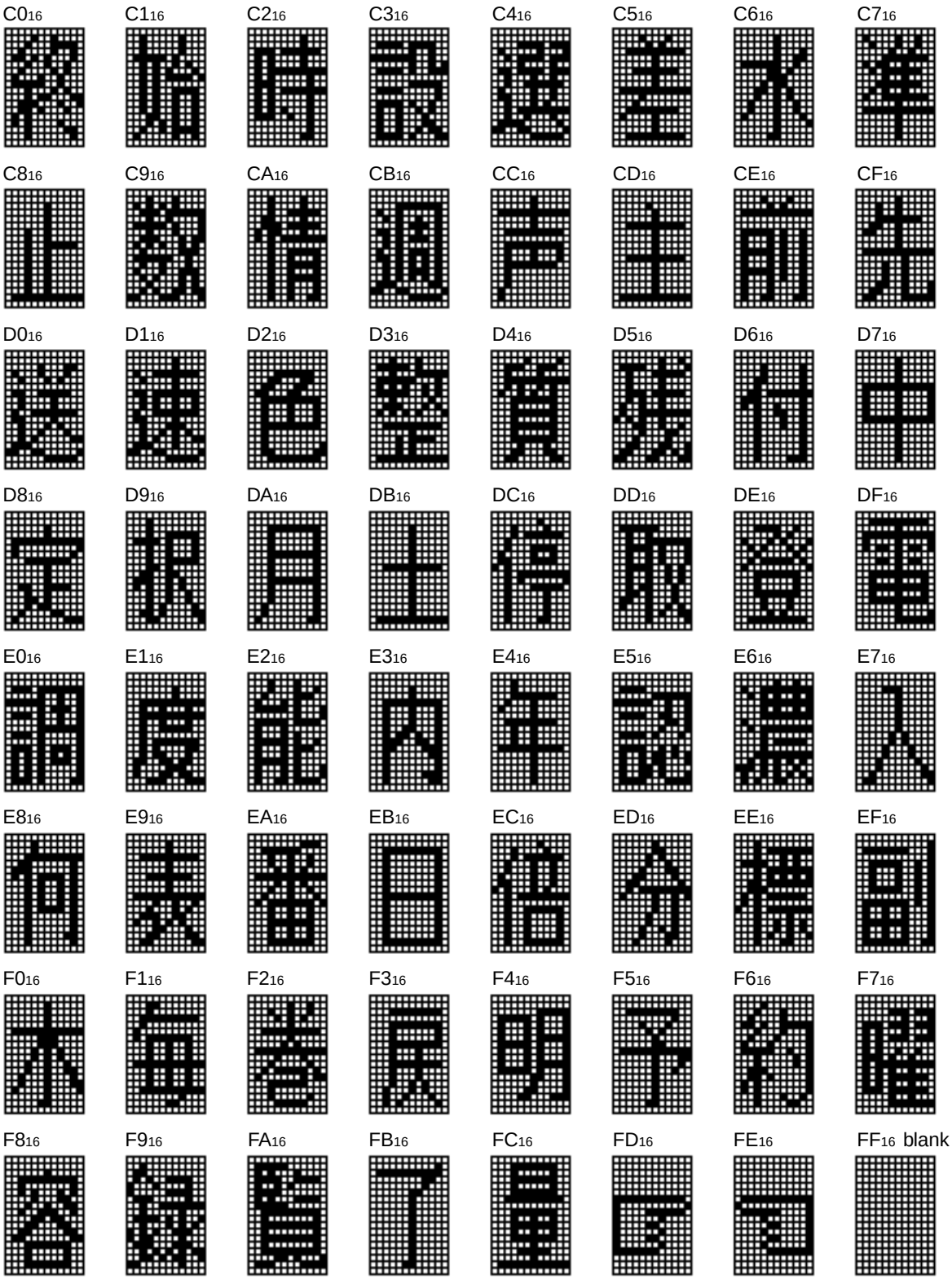


Fig. 24 M35053-001SP/FP character pattern (4)

MASK ROM ORDER CONFIRMATION FORM
GZZ-SH00-51B <69A0>

Mask ROM number	

MASK ROM ORDER CONFIRMATION FORM
SCREEN DISPLAY IC M35053-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Data :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵, □.

✵	Customer	Company name	TEL ( )	Issuance signature	Approval	Verification	Framing
		Data issued	Date :				

✵	Program version name	M053R V

✵Remarks

- Return the Character Font Preparation Program after use.
- Three EPROMs are required. (All the three EPROMs must be same types. Check @ in the appropriate box.)

  □ 27512

  (1) The font data prepared by the Character Font Preparation Program is saved as a binary type object file (addresses 0000h to 7FFFh). Three sets of these EPROMs are required.
  (2) Attach the erase protect seals on three EPROMs. Each seal bears the type name (M35053), and ROM No. (–...SP/FP).
- Write the checksum code (hexadecimal notation) for entire EPROM areas.

  Checksum | | | | |
- Select the marking type (Check @ in the appropriate box).

  Special Mark □.....Fill in the Mark Specification Form (20P4B for M35053-XXXSP, 20P2Q-A for M35053-XXXFP) and attach to the Mask ROM Order Confirmation Form.

  Standard Mark □.....No writing is required.
- The package type

  □..... SDIP type (M35053-XXXSP)

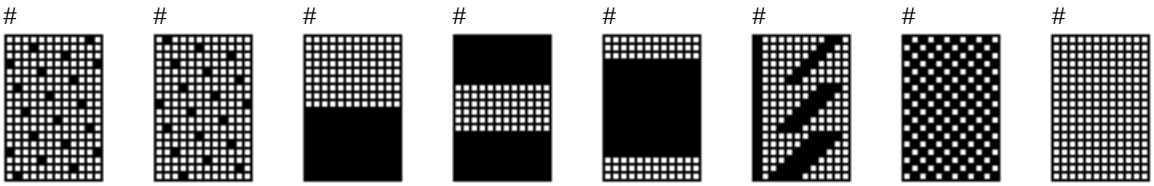
  □..... SSOP type (M35053-XXXFP)

✵● Comments

GZZ-SH00-51B <69A0>

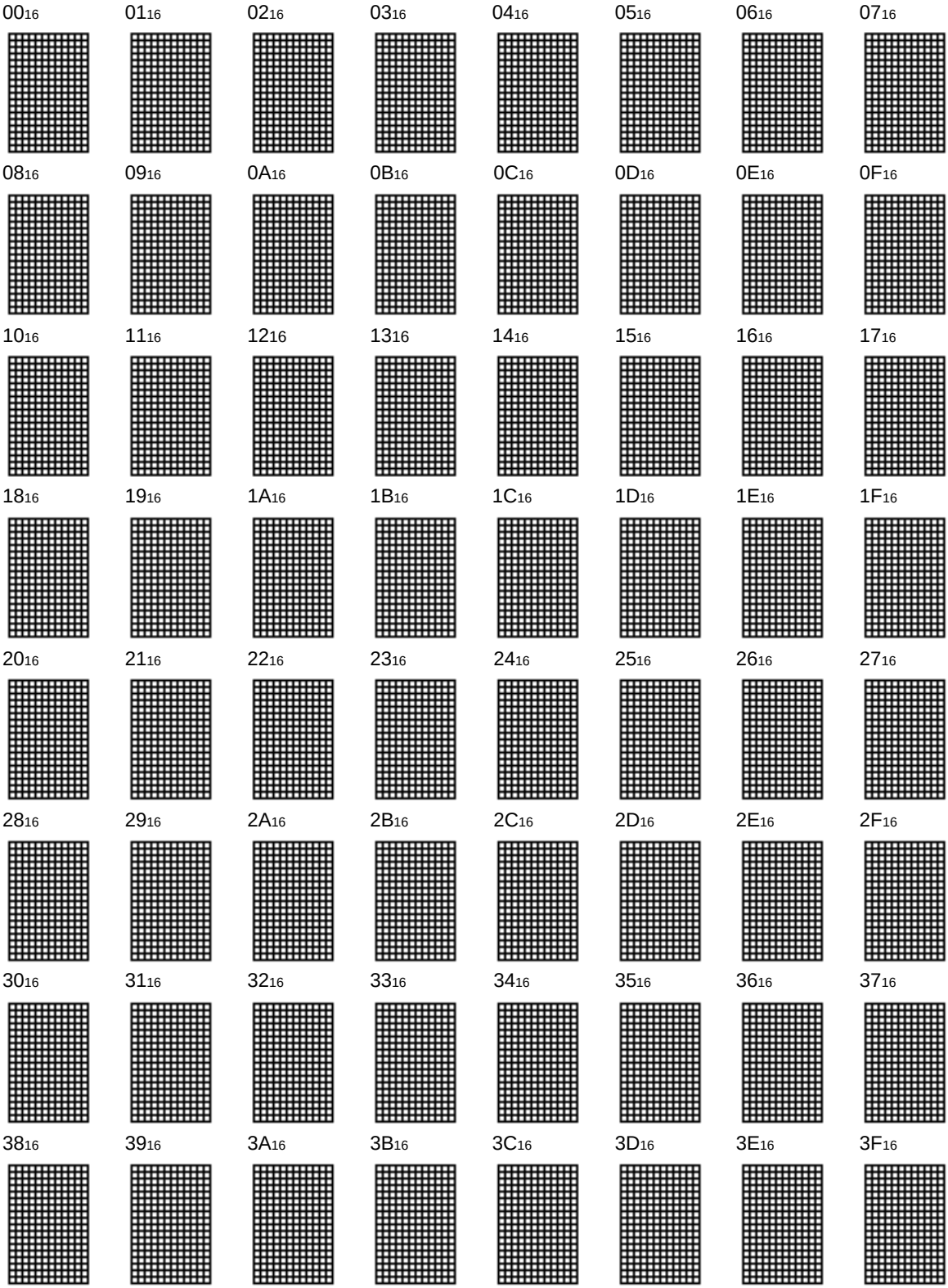
Mask ROM number	

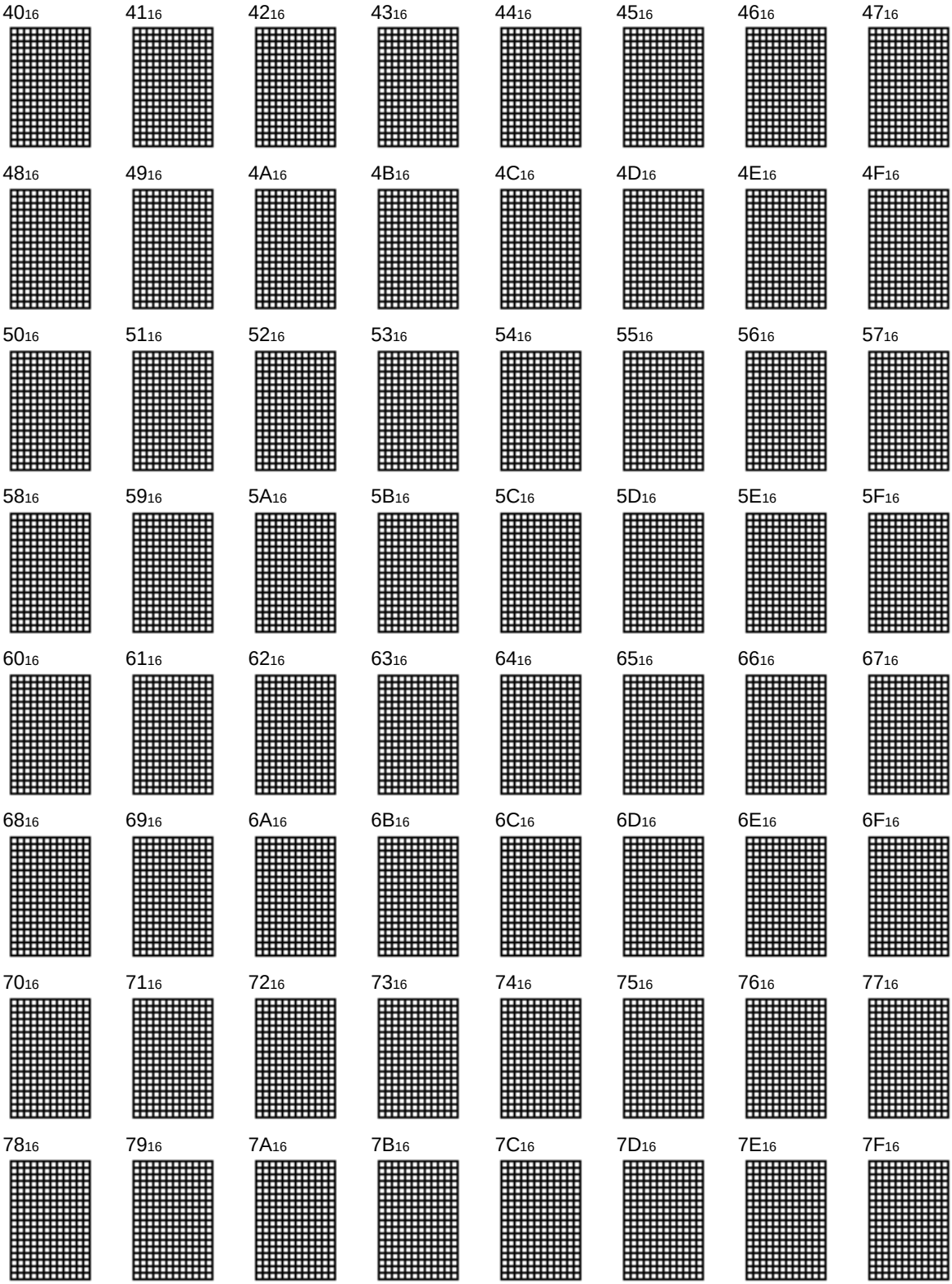
❋1. Test patterns



(The patterns with the mark "#" are test patterns)

❋2. Character patterns
(See the next page)


00₁₆ 01₁₆ 02₁₆ 03₁₆ 04₁₆ 05₁₆ 06₁₆ 07₁₆
08₁₆ 09₁₆ 0A₁₆ 0B₁₆ 0C₁₆ 0D₁₆ 0E₁₆ 0F₁₆
10₁₆ 11₁₆ 12₁₆ 13₁₆ 14₁₆ 15₁₆ 16₁₆ 17₁₆
18₁₆ 19₁₆ 1A₁₆ 1B₁₆ 1C₁₆ 1D₁₆ 1E₁₆ 1F₁₆
20₁₆ 21₁₆ 22₁₆ 23₁₆ 24₁₆ 25₁₆ 26₁₆ 27₁₆
28₁₆ 29₁₆ 2A₁₆ 2B₁₆ 2C₁₆ 2D₁₆ 2E₁₆ 2F₁₆
30₁₆ 31₁₆ 32₁₆ 33₁₆ 34₁₆ 35₁₆ 36₁₆ 37₁₆
38₁₆ 39₁₆ 3A₁₆ 3B₁₆ 3C₁₆ 3D₁₆ 3E₁₆ 3F₁₆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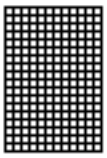
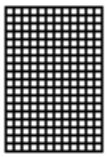
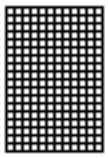
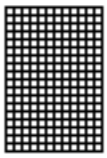
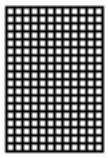
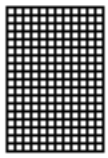
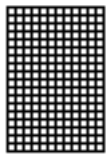
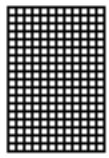
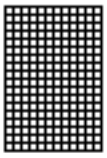
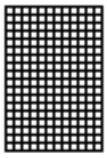
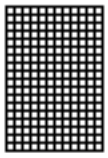
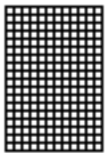
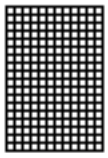
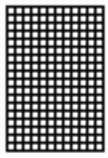
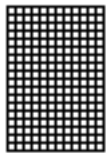
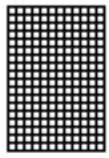
4616
4716
4816
4916
4A16
4B16
4C16
4D16
4E16
4F16
5016
5116
5216
5316
5416
5516
5616
5716
5816
5916
5A16
5B16
5C16
5D16
5E16
5F16
6016
6116
6216
6316
6416
6516
6616
6716
6816
6916
6A16
6B16
6C16
6D16
6E16
6F16
7016
7116
7216
7316
7416
7516
7616
7716
7816
7916
7A16
7B16
7C16
7D16
7E16
7F16

80_{16}	81_{16}	82_{16}	83_{16}	84_{16}	85_{16}	86_{16}	87_{16}
							
88_{16}	89_{16}	$8A_{16}$	$8B_{16}$	$8C_{16}$	$8D_{16}$	$8E_{16}$	$8F_{16}$
							
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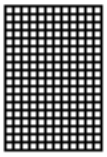	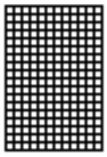	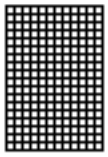	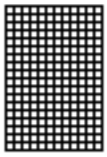	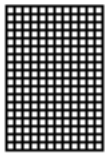	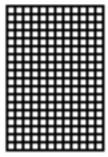	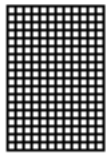	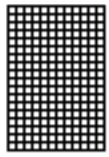
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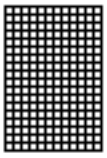	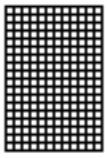	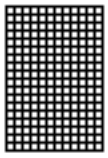	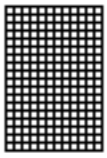	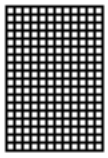	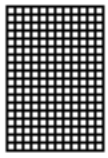	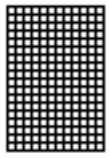	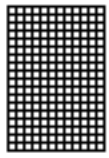
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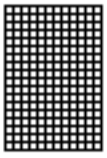	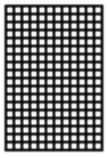	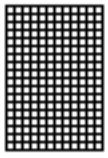	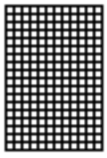	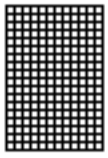	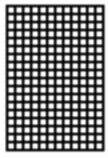	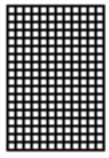	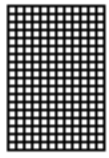
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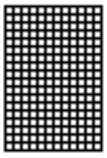	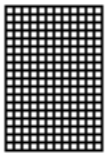	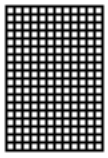	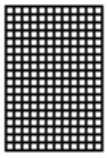	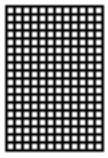	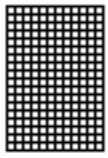	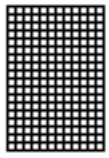	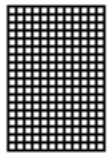
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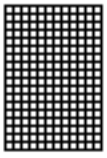	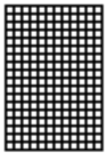	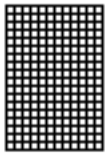	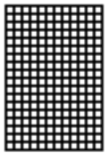	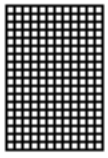	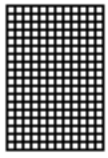	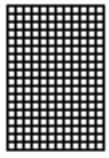	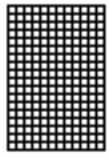
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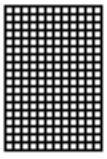
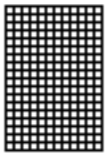
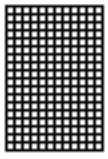
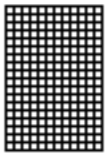
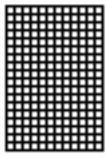
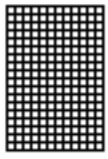
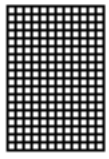
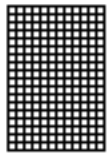
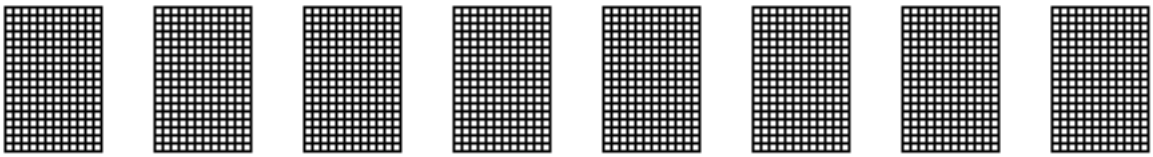
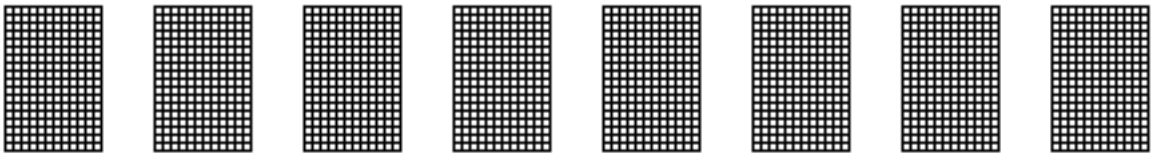
							

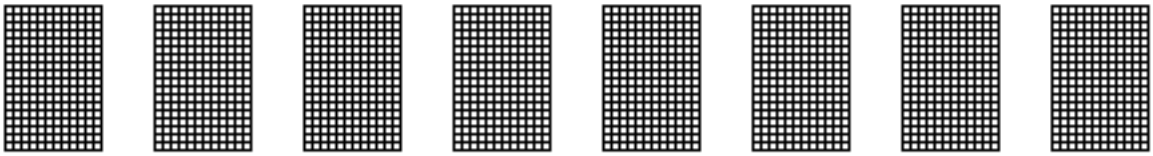
C0$_{16}$ C1$_{16}$ C2$_{16}$ C3$_{16}$ C4$_{16}$ C5$_{16}$ C6$_{16}$ C7$_{16}$



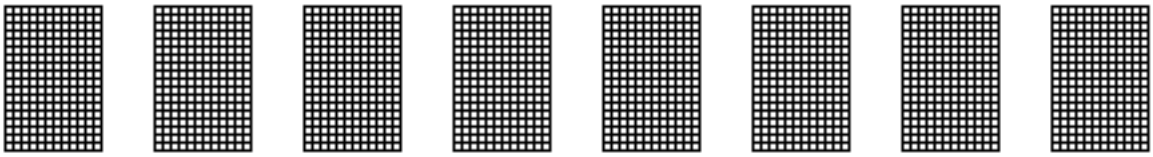
C8$_{16}$ C9$_{16}$ CA$_{16}$ CB$_{16}$ CC$_{16}$ CD$_{16}$ CE$_{16}$ CF$_{16}$



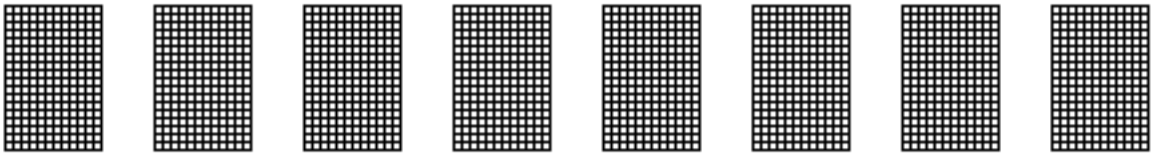
D0$_{16}$ D1$_{16}$ D2$_{16}$ D3$_{16}$ D4$_{16}$ D5$_{16}$ D6$_{16}$ D7$_{16}$



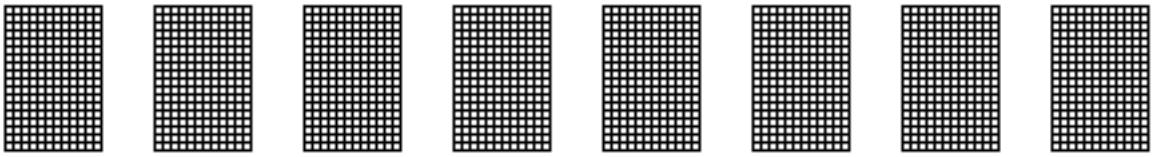
D8$_{16}$ D9$_{16}$ DA$_{16}$ DB$_{16}$ DC$_{16}$ DD$_{16}$ DE$_{16}$ DF$_{16}$



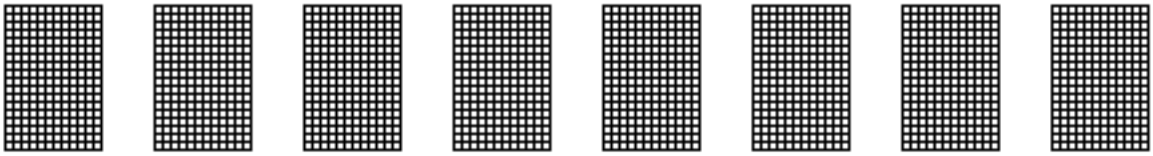
E0$_{16}$ E1$_{16}$ E2$_{16}$ E3$_{16}$ E4$_{16}$ E5$_{16}$ E6$_{16}$ E7$_{16}$



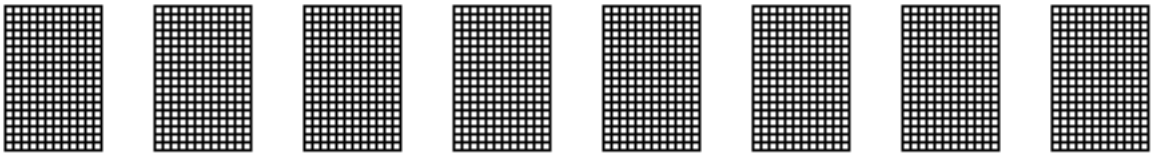
E8$_{16}$ E9$_{16}$ EA$_{16}$ EB$_{16}$ EC$_{16}$ ED$_{16}$ EE$_{16}$ EF$_{16}$



F0$_{16}$ F1$_{16}$ F2$_{16}$ F3$_{16}$ F4$_{16}$ F5$_{16}$ F6$_{16}$ F7$_{16}$



F8$_{16}$ F9$_{16}$ FA$_{16}$ FB$_{16}$ FC$_{16}$ FD$_{16}$ FE$_{16}$ FF$_{16}$ blank

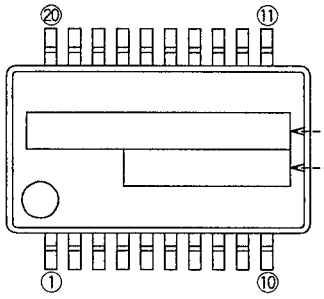


20P2Q-A (20-PIN SHRINK SOP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name

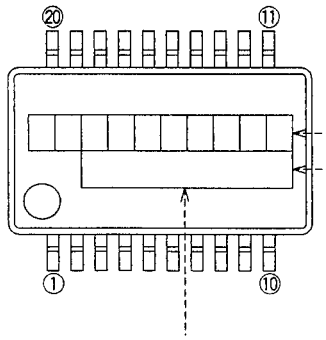
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



Mitsubishi IC catalog name
Mitsubishi IC catalog name (Mitsubishi lot number (6-digit or 7-digit))

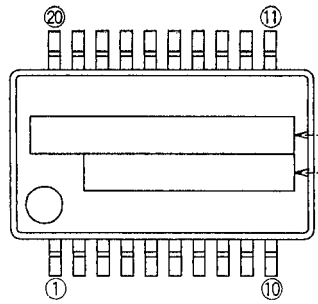
B. Customer's Parts Number + Mitsubishi catalog name



Mask ROM number Mitsubishi lot number (4-digit)

Customer's Parts Number
Note : The fonts and size of characters are standard Mitsubishi type.
Mitsubishi IC catalog name
Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's Parts Number can be up to 10 characters : Only 0 ~ 9, A ~ Z, +, –, /, (,), &, ©, • (periods), , (commas) are usable.

C. Special Mark Required



Note1 : If the Special Mark is to be Printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible.
Mitsubishi lot number (4-digit) and Mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the Special Mark, check the box below.
Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required ☐

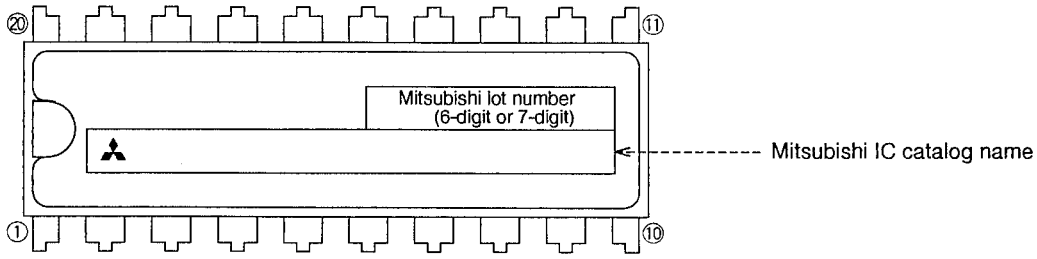
Special Mark (Customer's Trade Mark)
Mitsubishi IC catalog name

20P4B (20-PIN DIP) MARK SPECIFICATION FORM

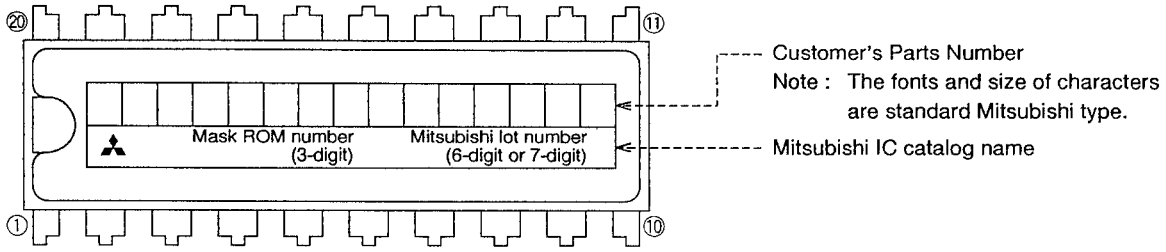
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



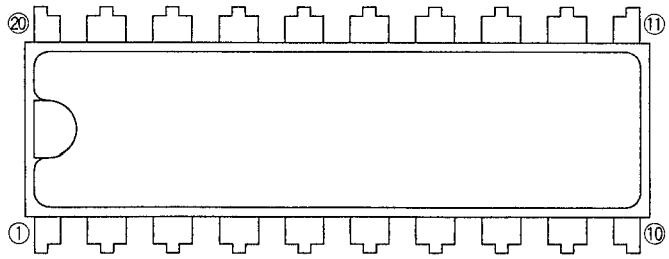
B. Customer's Parts Number + Mitsubishi catalog name



Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's Parts Number can be up to 15 characters : Only 0 ~ 9, A ~ Z, +, –, /, (,), &, ©, • (periods), (commas) are usable.
4 : If the Mitsubishi logo is not required, check the box on the right.

Mitsubishi logo is not required ☐

C. Special Mark Required



Note1 : If the Special Mark is to be Printed, indicate the desired layout of the mark in the upper figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit or 7-digit) and Mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the Special Mark, check the box on the right. Please submit a clean original of the logo. For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required ☐

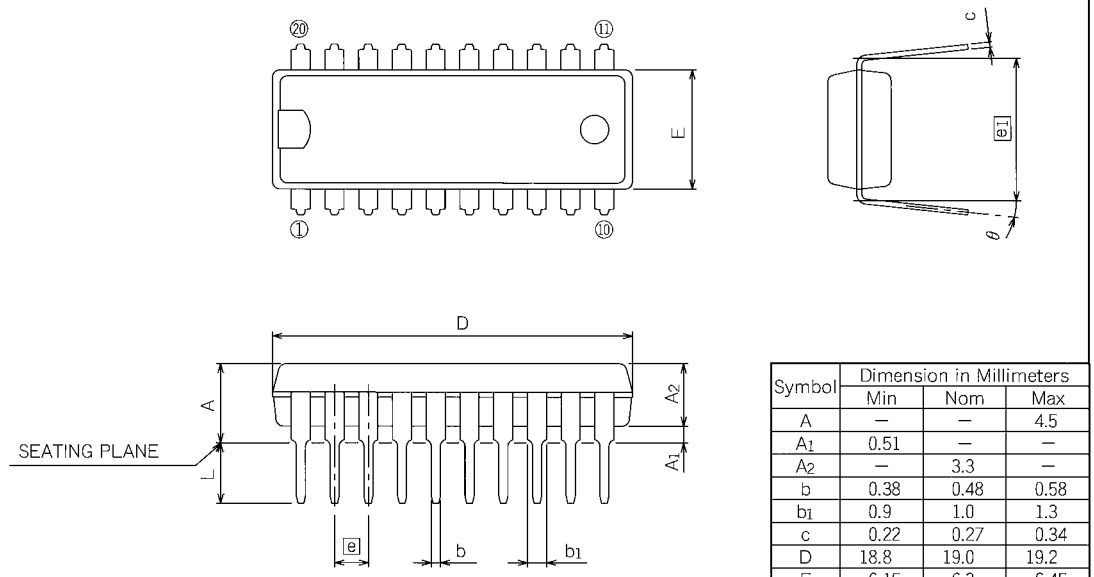
PACKAGE OUTLINE

20P4B

Plastic 20pin 300mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP20-P-300-1.78	—	1.0	

Scale : 2.5/1



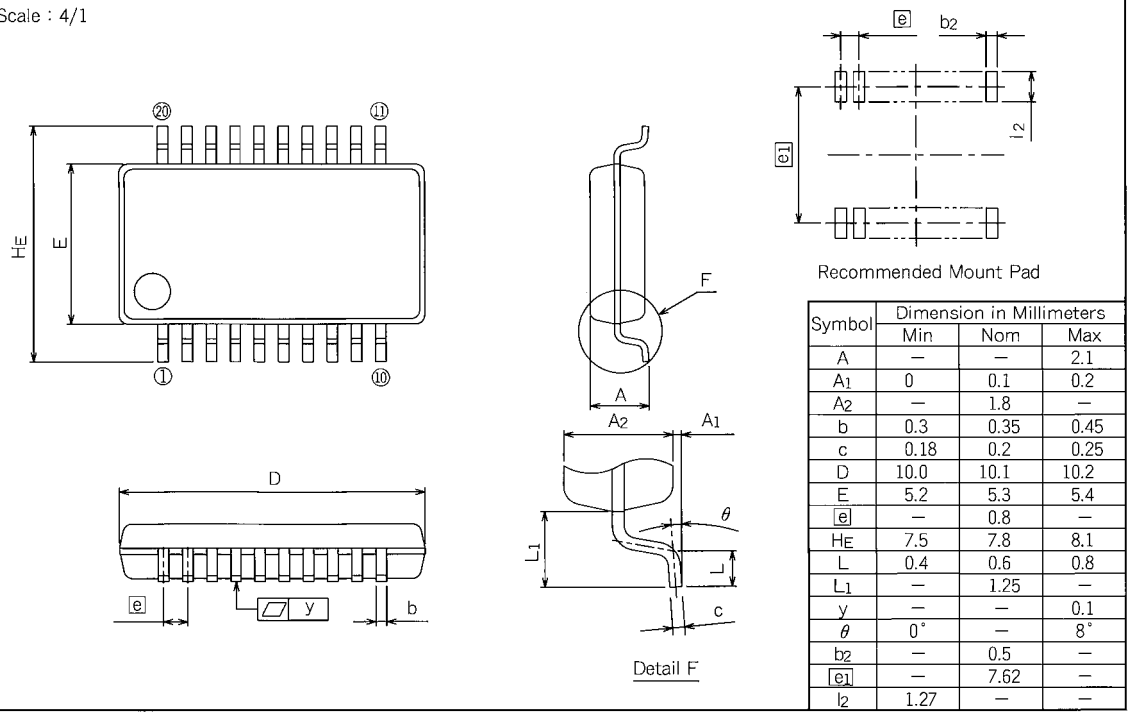
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b	0.38	0.48	0.58
b_1	0.9	1.0	1.3
c	0.22	0.27	0.34
D	18.8	19.0	19.2
E	6.15	6.3	6.45
e	—	1.778	—
e1	—	7.62	—
L	3.0	—	—
θ	0°	—	15°

20P2Q–A

Plastic 20pin 300mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP020-P-0300	—	0.2	Cu Alloy

Scale : 4/1



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.1
A_1	0	0.1	0.2
A_2	—	1.8	—
b	0.3	0.35	0.45
c	0.18	0.2	0.25
D	10.0	10.1	10.2
E	5.2	5.3	5.4
e	—	0.8	—
H_E	7.5	7.8	8.1
L	0.4	0.6	0.8
L_1	—	1.25	—
y	—	—	0.1
θ	0°	—	8°
b_2	—	0.5	—
e1	—	7.62	—
l_2	1.27	—	—

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REVISION DESCRIPTION LIST	M35053-XXXSP/FP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	971130