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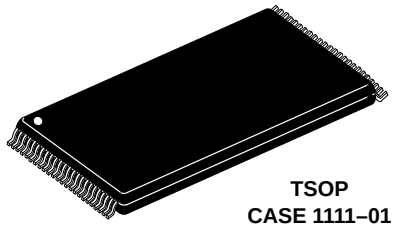
M29F016

Advance Information

16M CMOS Sector Erase Flash Memory



TSOP
CASE 1111–01

TSOP REVERSE
CASE 1111A–01

The M29F016 is a 16M, 5 V–only, sector erase flash memory organized as 2M bytes of 8 bits each. The M29F016 is offered in JEDEC–standard 48–pin packages.

- 5.0 V ± 10% Read, Write and Erase Minimizes System Level Power Requirements
- JEDEC Industry Standard Pin–Out and Architecture
- Compatible with JEDEC–Standard (E^2PROM) Commands
- Minimum 100,000 Write/Erase Cycles
- Sector Erase Architecture:
  32 Equal Size Sectors of 64K Bytes Each
  Any Combination of Sectors can be Concurrently Erased
  Supports Full Chip Erase
- Embedded Erase™ Algorithms Allow Automatic Preprogram and Erase at any Sector
- Embedded Program™ Algorithms Allow Automatic Write and Verify of Data at a Specified Address
- Data Polling and Toggle Bit Feature for Detection of Program or Erase Cycle Completion
- Sector Protection Allows Hardware Disable of Sectors from Write or Erase Operations
- Low V_{CC} Write Inhibit ≤ 3.2 V
- Fast Access Time: M29F016–90 = 90 ns (Max)
  M29F016–12 = 120 ns (Max)
- Low Active Power Dissipation: M29F016–90 = 275 mW
  M29F016–12 = 275 mW
- Low Standby Power Dissipation:
  TTL Levels: M29F016–90 = 5.5 mW
  M29F016–12 = 5.5 mW
  CMOS Levels: M29F016–90 = 0.55 mW
  M29F016–12 = 0.55 mW

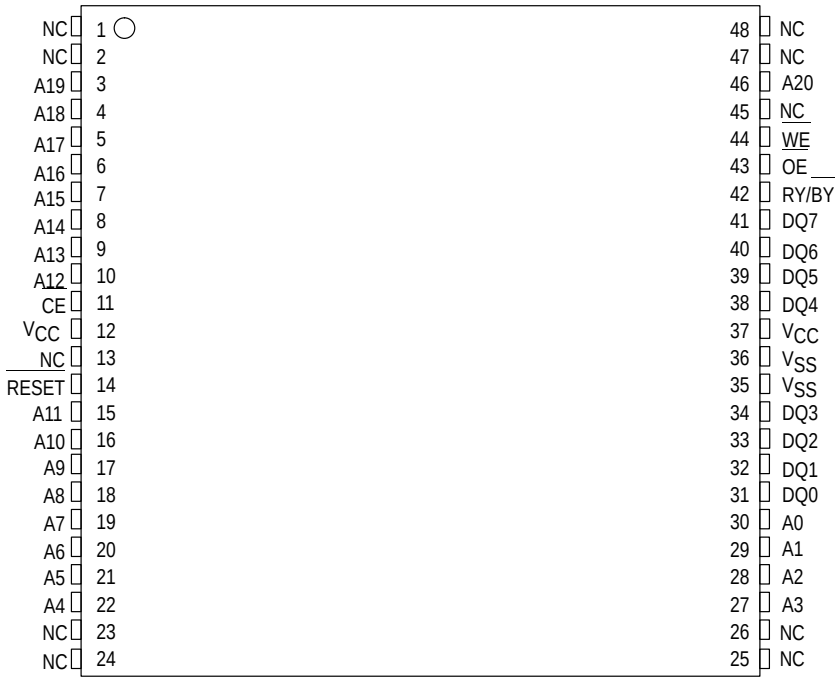
PIN NAMES	
A0 – A20	Address Input
CE	Chip Enable
WE	Write Enable
OE	Output Enable
DQ0 – DQ7	Data Input/Output
RESET	Hardware Reset Pin, Active Low
RY/BY	Ready/BUSY Output
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

Embedded Erase and Embedded Program are trademarks of Advanced Micro Devices, Inc.

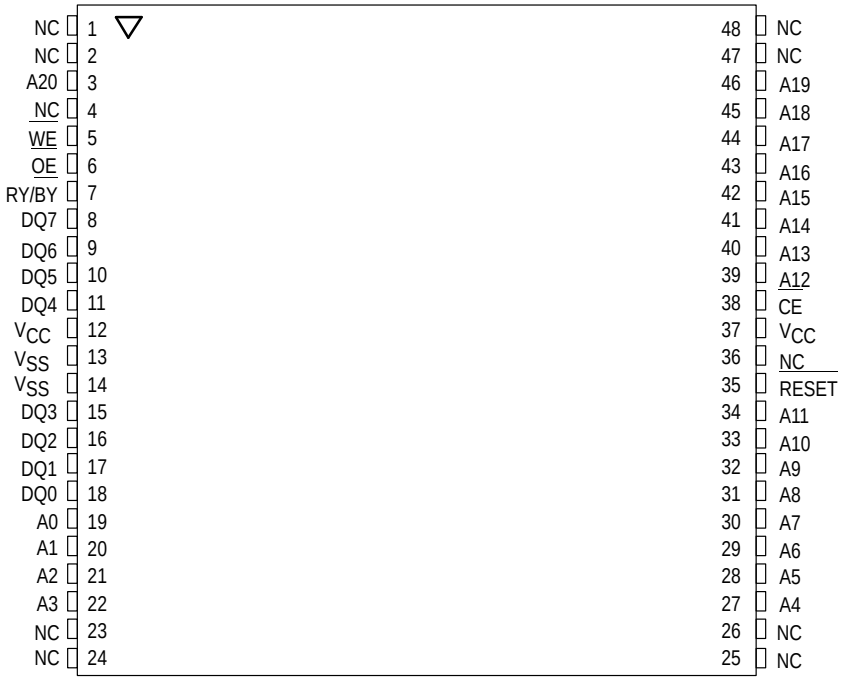
This document contains information on a new product. Specifications and information herein are subject to change without notice.

PIN ASSIGNMENTS

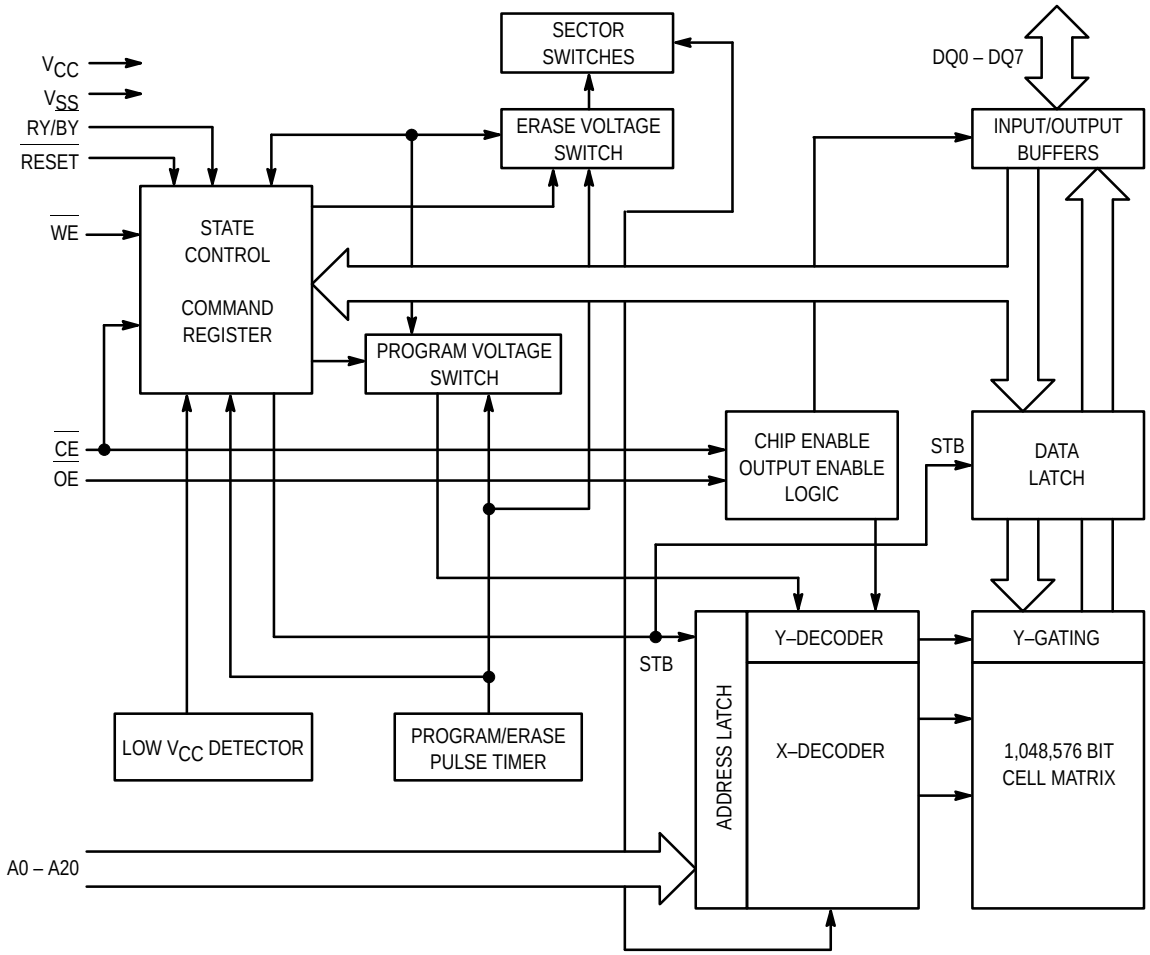
TSOP
STANDARD PINOUT



TSOP
REVERSE PINOUT



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Notes 1 through 4)

Rating	Symbol	Value	Unit
Power Supply Voltage (Note 1)	V_{CC}	– 2.0 to + 7	V
Voltage Relative to V_{SS}: All Pins Except A9, CE, and OE (Note 1) A9, CE, and OE	V_{in}, V_{out}	 – 2.0 to + 7 – 2.0 to + 14	V
Output Short Circuit Current (Note 3)	I_{out}	200	mA
Power Dissipation	P_D	350	mW
Ambient Temperature with Power Applied	T_A	– 55 to + 125	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 – 65 to + 150 – 65 to + 125	°C

NOTES:
1. Minimum dc voltage on input or I/O pins is – 0.5 V. During voltage transitions, inputs may undershoot V_{SS} to – 2.0 V for periods of up to 20 ns. Maximum dc voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.
2. Minimum dc voltage on pin A9, CE, and OE is – 0.5 V. During voltage transitions, A9, CE, and OE may undershoot V to – 2.0 V for periods of up to 20 ns. Maximum dc input voltage on A9, CE, and OE is + 13.5 V which may overshoot to 14.0 V_{SS} for periods up to 20 ns.
3. No more than one output shorted at a time. Duration of the short circuit should not be longer than one second.
4. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

OPERATING RANGES (See Note)

Rating	Symbol	Value	Unit
Supply Voltages M29F016–90 = 90 ns, M29F016–12 = 120 ns	V_{CC}	 + 4.50 to + 5.50	V
Operating Temperature Range Commercial Industrial	T_C	 0 to + 70 – 40 to + 85	°C

NOTE: Operating ranges define those limits between which the functionality of the device is guaranteed.

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A9)	– 1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all I/O pins	– 1.0 V	V_{CC} + 1.0 V
Current	– 100 mA	+ 100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DC OPERATING CONDITIONS AND CHARACTERISTICS

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Active Current (CE = V_{IL}, OE = V_{IH})	I_{CC1}	—	40	mA	1
V_{CC} Active Current (CE = V_{IL}, OE = V_{IH})	I_{CC2}	—	60	mA	2, 3
V_{CC} Standby Current TTL/NMOS Levels (V_{CC} = V_{CC} max, $\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}) CMOS Levels (V_{CC} = V_{CC} max, CE = V_{CC} ± 0.3 V, Reset = V_{CC} ± 0.3 V)	I_{CC3}	 — —	 1.0 5	 mA µA	
Input Load Current (V_{in} = V_{SS} to V_{CC}, V_{CC} = V_{CC} max)	I_{LI}	—	± 1.0	µA	
A9, CE, and OE Input Load Current (V_{CC} = V_{CC} max, A9, CE, and OE = 12.5 V)	I_{LIT}	—	50	µA	
Output Leakage Current (V_{out} = V_{SS} to V_{CC}, V_{CC} = V_{CC} max)	I_{LO}	—	± 1.0	µA	
Input Low Level	V_{IL}	– 0.5	0.8	V	
Input High Voltage TTL/NMOS Levels CMOS Levels	V_{IH}	 2 0.7 x V_{CC}	 V_{CC} + 0.5 V_{CC} + 0.3	V	
Voltage for Autoselect and Sector Protect (V_{CC} = 5.0 V)	V_{ID}	11.5	12.5	V	
Output High Level TTL/NMOS Levels (I_{OH} = – 2.5 mA, V_{CC} = V_{CC} min)	V_{OH}	 2.4	 —	V	
Output High Voltage CMOS Levels (I_{OH} = – 2.5 mA, V_{CC} = V_{CC} min) CMOS Levels (I_{OH} = – 100 µA, V_{CC} = V_{CC} min)	 V_{OH1} V_{OH2}	 0.85 V_{CC} V_{CC} – 0.4	 — —	V	
Low V_{CC} Lock–Out Voltage	V_{LKO}	3.2	4.2	V	

NOTES:
1. The I_{CC} current listed includes both the dc operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with OE at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. Not 100% tested.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

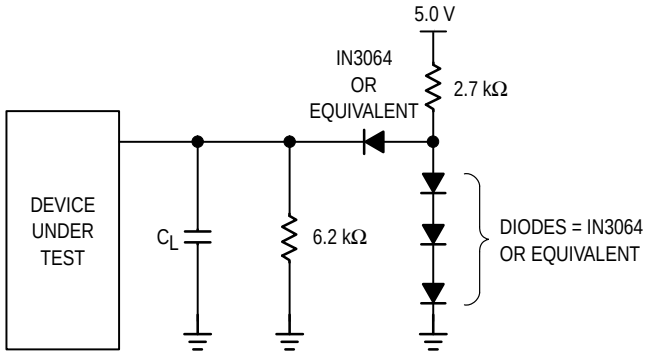
Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0)	C_{in}	6	7.5	pF
Control Pin Capacitance (V_{in} = 0)	C_{in2}	7.5	9	pF
Output Capacitance (V_{out} = 0)	C_{out}	8.5	12	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

READ ONLY OPERATIONS CYCLE (See Note 1)

Parameter	Symbol		M29F016–90 (Note 2)		M29F016–12 (Note 2)		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	90	—	120	—	ns	4
Address to Output Delay, CE = V_{IL}, OE = V_{IL}	t_{AVQV}	t_{ACC}	—	90	—	120	ns	
Chip Enable to Output Delay, OE = V_{IL}	t_{ELQV}	t_{CE}	—	90	—	120	ns	
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	40	—	50	ns	
Chip Enable to Output High–Z	t_{EHQZ}	t_{DF}	—	20	—	30	ns	3, 4
Output Enable to Output High–Z	t_{GHQZ}	t_{DF}	—	20	—	30	ns	3, 4
Output Hold from Addresses, CE, or OE, Whichever Occurs First	t_{AXQX}	t_{OH}	0	—	0	—	ns	
RESET Pin Low to Read Mode		t_{READY}	—	20	—	20	µs	4

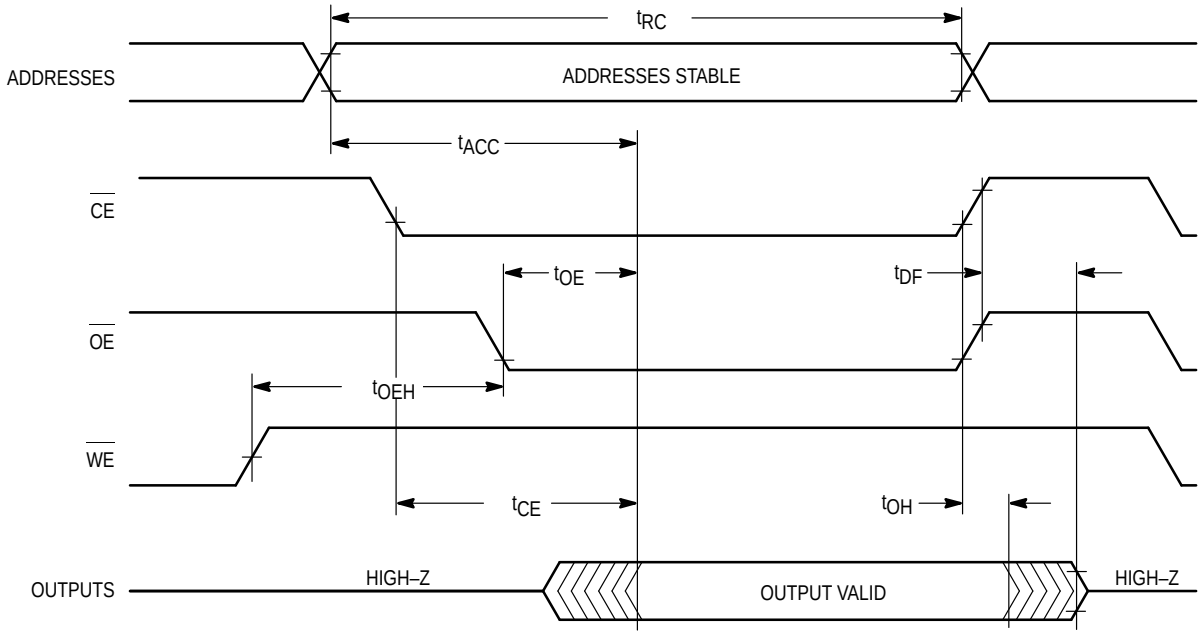
NOTES:
1. Test conditions — output load: one TTL gate and 30 pF; input rise and fall times: 5 ns; input pulse levels: 0 to 3 V; timing measurement reference level: input, 1.5 V; output, 1.5 V.
2. Test conditions — output load: one TTL gate and 100 pF; input rise and fall times: 20 ns; input pulse levels: 0.45 to 2.4 V; timing measurement reference level: input, 0.8 and 2.0 V; output, 0.8 and 2.0 V.
3. Output driver disable time.
4. Not 100% tested.



NOTE: C_L = 100 pF including jig capacitance.

Figure 1. Test Conditions

READ CYCLE


tRC
ADDRESSES
ADDRESSES STABLE
tACC
CE
tOE
tDF
OE
tOEH
WE
tCE
tOH
OUTPUTS
HIGH–Z
OUTPUT VALID
HIGH–Z

WRITE/ERASE/PROGRAM OPERATIONS

Parameter	Symbol		M29F016–90		M29F016–12		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	90	—	120	—	ns	1
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Hold Time	t_{WLAX}	t_{AH}	45	—	50	—	ns	
Data Setup Time	t_{DVWH}	t_{DS}	45		50		ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	ns	
Output Enable Hold Time Read Toggle and Data Polling		t_{OEH}	0 10	— —	0 10	— —	ns	1
Read Recovery Time Before Write (OE high to WE low)	t_{GHWL}		0	—	0	—	ns	
CE Setup Time	t_{ELWL}	t_{CS}	0	—	0	—	ns	
CE Hold Time	t_{WHEH}	t_{CH}	0	—	0	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	45	—	50	—	ns	
Write Pulse Width High	t_{WHWL}	t_{WPH}	20	—	20	—	ns	
Byte Programming Operation	t_{WHWH1}		14	—	14	—	µs	
Erase Operation	t_{WHWH2}		—	15	—	15	s	2
V_{CC} Setup Time		t_{VCS}	50	—	50	—	µs	1
Voltage Transition Time		t_{VLHT}	4	—	4	—	µs	1, 3
OE Setup Time to WE Active		t_{OESP}	4	—	4	—	µs	1, 3
RESET Pulse Width		t_{RP}	500	—	500	—	ns	
Program/Erase Valid to RY/BY Delay		t_{BUSY}	40	—	50	—	ns	

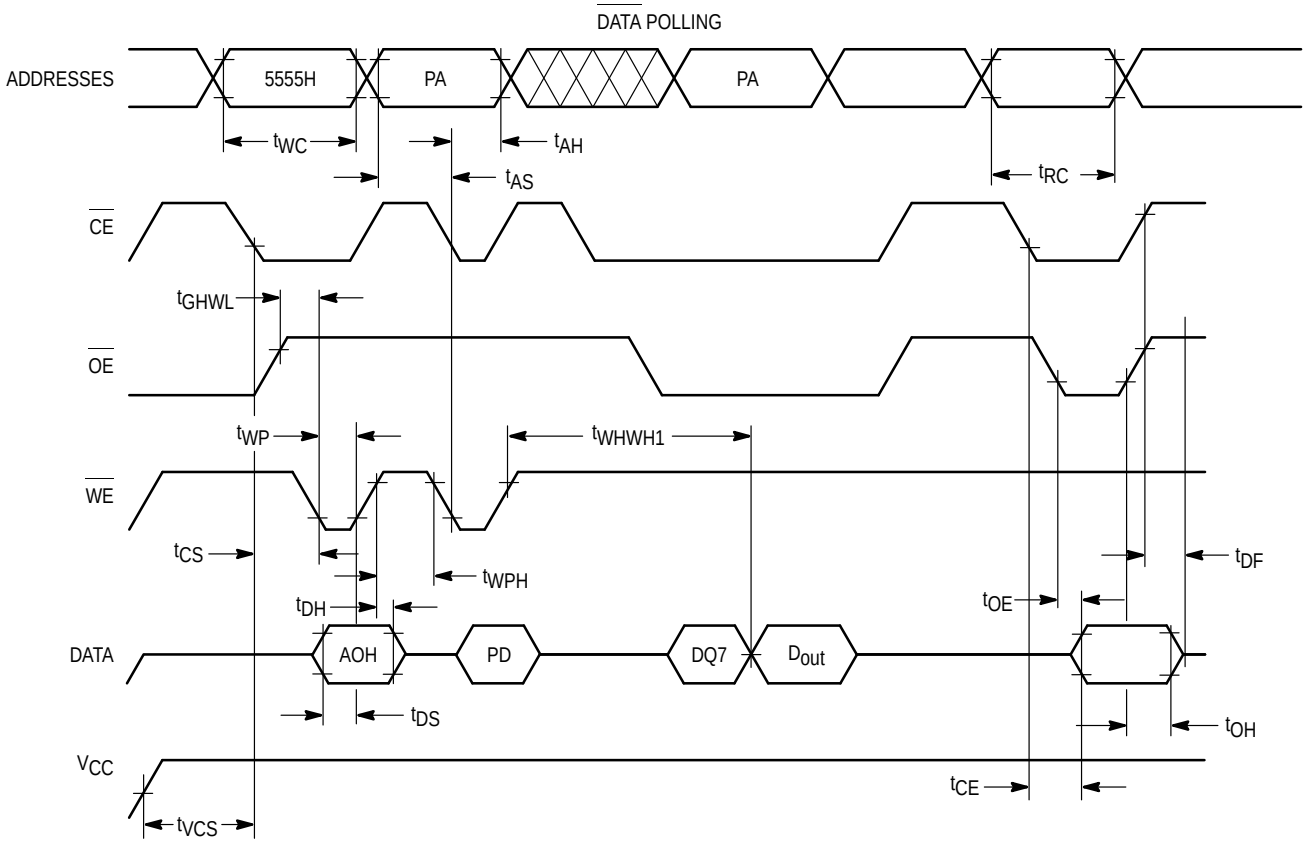
NOTES:
1. Not 100% tested.
2. This does not include the pre–programming time.
3. These timings are for Sector Protect/Unprotect operations.
4. This timing is only for Sector Unprotect.

ERASE AND PROGRAMMING PERFORMANCE (See Note 2)

Parameter	Limits			Unit	Comments	Notes
	Min	Typ	Max			
Chip/Sector Erase Time		1	15	sec	Excludes 00H programming prior to erasure	1
Byte Programming Time		8	2000	µs	Excludes system–level overhead	3
Chip Programming Time		16	50	sec	Excludes system–level overhead	1, 2, 3
Erase/Program Cycles	100,000	1,000,000		Cycles		

NOTES:
1. 25°C, 5.0 V V_{CC}, 100,000 cycles.
2. Although Embedded Algorithms allow for a longer chip program and erase time, the actual time will be considerably less since bytes program or erase significantly faster than the worst case byte.
3. Under worst case condition of 90°C, 4.5 V V_{CC}, 100,000 cycles.

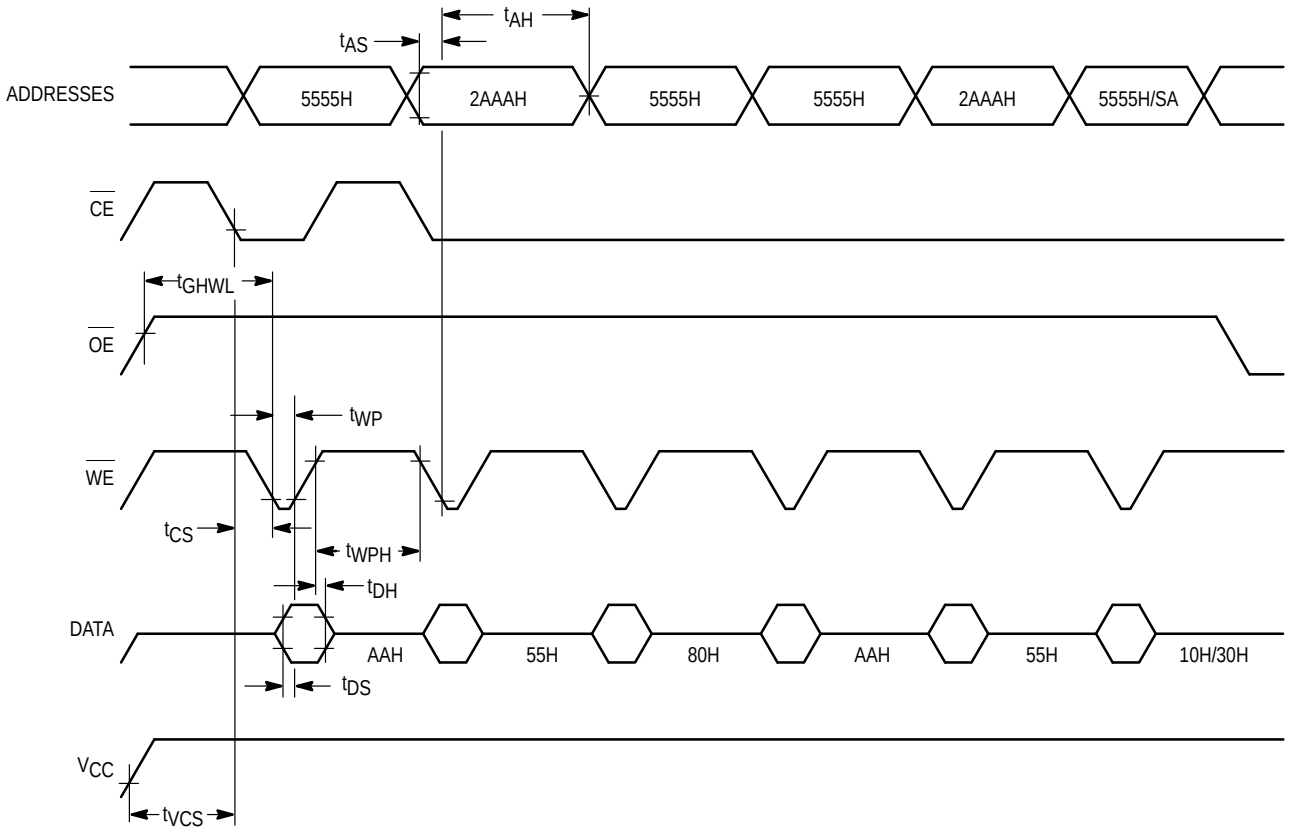
PROGRAM OPERATIONS



NOTES:

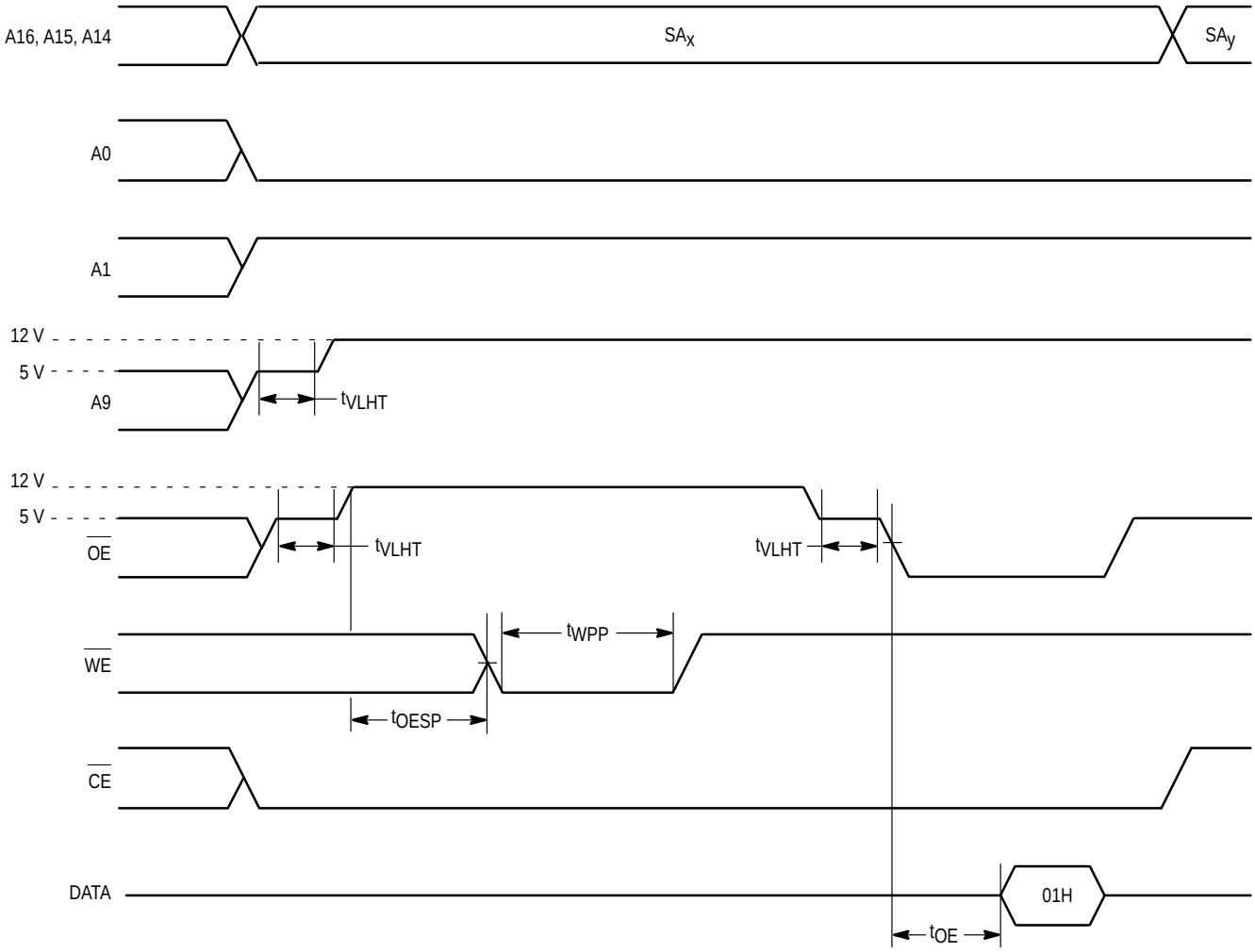
1. Figure indicates last two bus cycles of four bus cycle sequence.
2. PA is address of the memory location to be programmed.
3. PD is data to be programmed at byte address.
4. DQ7 is the output of the complement of the data written to the device.
5. D_{out} is the output of the data written to the device.

CHIP/SECTOR ERASE OPERATIONS



NOTE: SA is the sector address for Sector Erase.

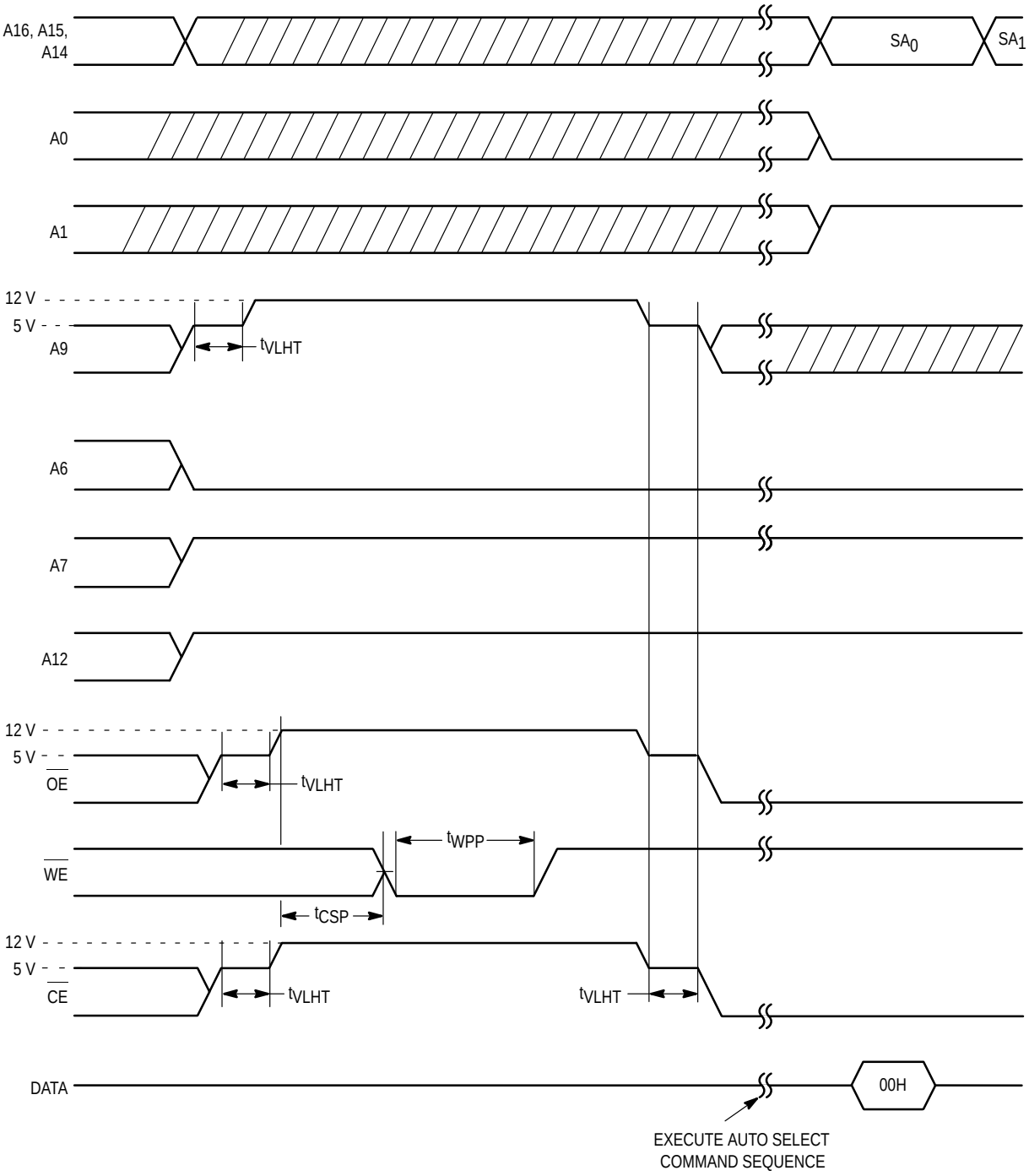
SECTOR PROTECT CYCLE



SA_X = Sector Address for initial sector

SA_Y = Sector Address for next sector

SECTOR UNPROTECT CYCLE

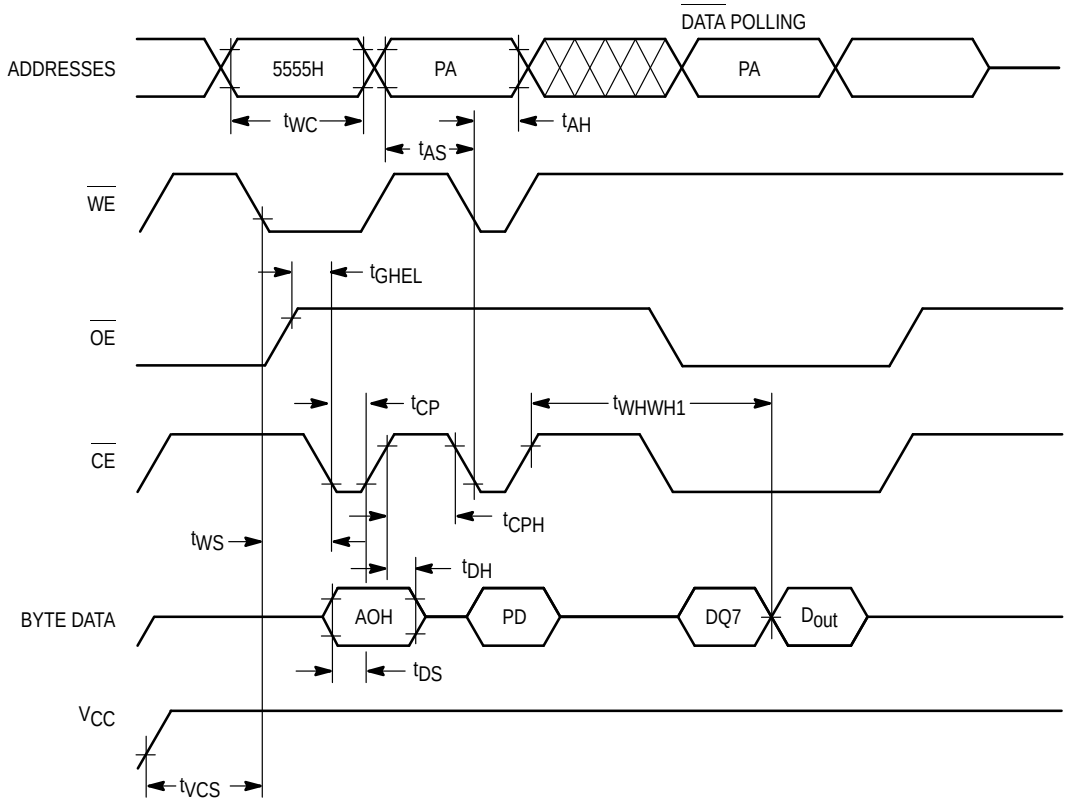


ALTERNATE $\overline{CE}$ CONTROLLED WRITE CYCLES

Parameter	Symbol		M29F016–90			M29F016–12			Unit	Notes
	Std	Alt	Min	Max	Typ	Min	Max	Typ		
Write Cycle Time	t_{AVAV}	t_{WC}	90	—	—	120	—	—	ns	1
Address Setup Time	t_{AVEL}	t_{AS}	0	—	—	0	—	—	ns	
Address Hold Time	t_{ELAX}	t_{AH}	45	—	—	50	—	—	ns	
Data Setup Time	t_{DVEH}	t_{DS}	45			50			ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	—	0	—	—	ns	
Output Enable Setup Time		t_{OES}	0	—	—	0	—	—	ns	
Output Enable Hold Time ____ Read Toggle and Data Polling		t_{OEH}	0 10	— —	— —	0 10	— —	— —	ns	1
Read Recover Time before Write		t_{GHEL}	0	—	—	0	—	—	ns	
WE Setup Time	t_{WLEL}	t_{WS}	0	—	—	0	—	—	ns	
WE Hold Time	t_{EHWH}	t_{WH}	0			0			ns	
CE Pulse Width	t_{ELEH}	t_{CP}	45	—	—	50	—	—	ns	
CE Pulse Width High	t_{EHEL}	t_{CPH}	20	—	—	20	—	—	ns	
Byte Programming Operation	t_{WHWH1}	t_{WHWH1}	—	—	8	—	—	8	µs	
Erase Operation	t_{WHWH2}	t_{WHWH2}	—	—	1	—	—	1	s	2
V_{CC} Setup Time		t_{VCS}	2	—	—	2	—	—	µs	1

NOTES:
1. Not 100% tested.
2. This also includes the pre–programming time.

ALTERNATE $\overline{CE}$ CONTROLLED WRITE CYCLE



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2. PA is address of the memory location to be programmed.
3. PD is data to be programmed at byte address.
4. DQ7 is the output of the complement of the data written to the device.
5. D_{out} is the output of the data written to the device.

GENERAL DESCRIPTION

The M29F016 is a 16M, 5 V only Flash Memory device organized a s two megabytes of eight bits each. The two megabytes of data are divided into 32 sectors of 64 Kbytes for flexible erase capability. The eight bits of data will appear on DQ0–DQ7. The M29F016 is offered in a 48 pin TSOP package. This device is designed to be programmed in–system with the standard system 5.0 volt V_{CC} supply. 12.0 volt V_{pp} is not required for program or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The standard M29F016 offers access times between 90 and 120 nanoseconds, allowing operation of high–speed microprocessors without wait states. To eliminate bus contention, the device has separate chip enable (CE), write enable (WE), and output enable (OE) controls.

This device is entirely command set compatible with the JEDEC single–power supply Flash standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state–machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

The M29F016 is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

This device also features a sector erase architecture. This allows sectors of memory to be erased and reprogrammed without affecting the data contents of other sectors. A sector is typically erased and verified within one second. the M29F016 is erased when shipped form the factory.

The device also features hardware sector group protection. This feature will disable both program and erase operations in any combination of eight sector groups of memory. A sector group consists of four adjacent sectors grouped in the following pattern: sectors 0–3, 4–7, 8–11, 12–15, 16–19, 20–23, 24–27, and 28–31.

The Erase Suspend feature enables the user to put erase on hold for any period of time to read data from, or program data to, a sector that was not being erased. Thus, true background erase can be achieved.

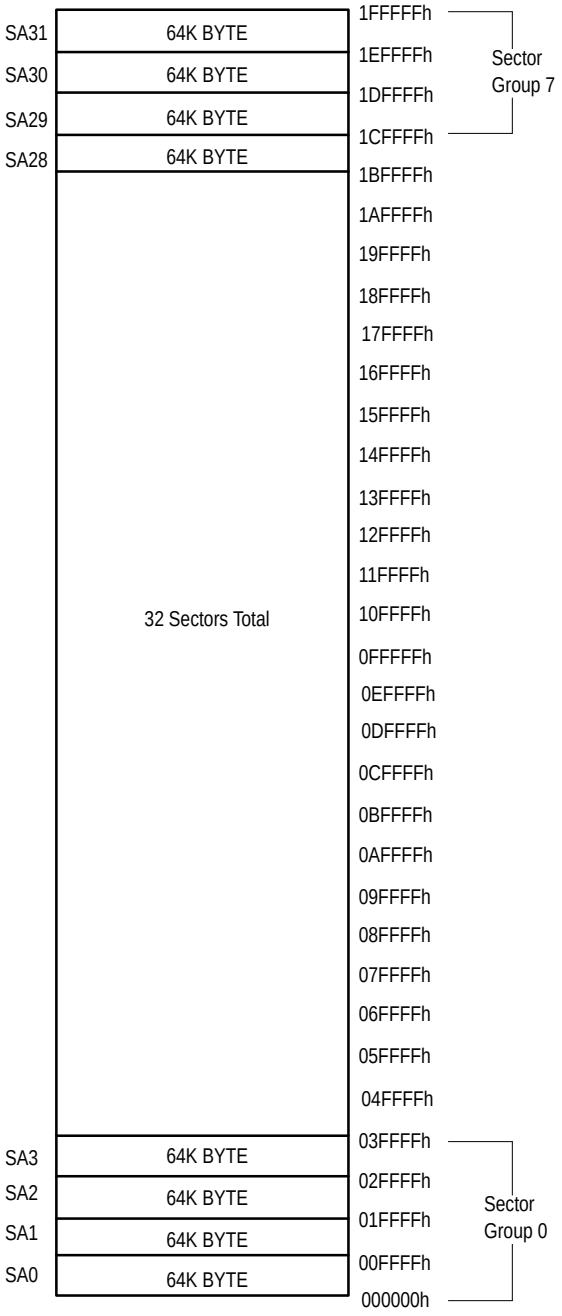
The device features single 5.0 volt power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations during power transitions. The end of program or erase is detected by the RY/BY pin, Data Polling of DQ7, or by the Toggle Bit I (DQ6). Once the end of a program of erase cycle has been completed, the device automatically resets to the read mode.

The M29F016 also has a hardware $\overline{\text{RESET}}$ pin, When this pin is driven low, execution of any Embedded Program Algorithm of Embedded Erase Algorithm will be terminated. The internal state machine will then be reset into the read mode. The RESET pin may be tied to the system reset circuitry. Therefore, if a system reset occurs during the Embedded Program Algorithm or Embedded Erase Algorithm, the device will be automatically reset to the read mode. This will enable the system's microprocessor to read the boot–up firmware from the Flash memory.

The M29F016 memory electrically erases all bits when sector simultaneously via Fowler–Nordheim tunneling. The bits are programmed one byte at a time using the EPROM programming mechanism of hot electric injection.

FLEXIBLE SECTOR–ERASE ARCHITECTURE

- Thirty–two 64K byte sectors
- 8 sector groups each of which consists of 4 adjacent sectors in the following pattern: sectors 0–3, 4–7, 8–11, 12–15, 16–19, 20–23, 24–27, and 28–31.
- Individual–sector or multiple–sector erase capability
- Sector group protection is user–definable



READ MODE

The M29F016 has two control functions which must be satisfied in order to obtain data at the outputs. CE is the power control and should be used for device selection. OE is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable CE to valid data at the output pins. The output enable access time is the delay from the falling edge of OE to valid data at the output pins (assuming the addresses have been stable for at least $t_{ACC} - t_{OE}$ time).

STANDBY MODE

The device has two standby modes, a CMOS standby mode (CE input held at $V_{CC} \pm 0.5$ V), when the current consumed is 100 µA; and a TTL standby mode (CE is held at V_{IH}) when the current required is reduced to approximately 200 µA. In the standby mode the outputs are in a high impedance state, independent of the OE input.

If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

OUTPUT DISABLE

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

AUTOSELECT

The autoselect mode allows the reading out of a binary code from the device and will identify the Flash component manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All addresses are don't cares except A0, A1, and A6.

The manufacturer and device codes may also be read via the command register, when the device is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 4 (refer to Autoselect Command section).

Byte 0 (A0 = V_{IL}) represents the manufacturer's code (for example, AMD = 01H) and byte 1 (A0 = V_{IH}) the device identifier code (for example, M29F016 = ADH). These two bytes are given in the table below. All identifiers for manufacturers and device will exhibit odd parity with the MSB (DQ7) defined as the parity bit. In order to read the proper device codes when executing the autoselect, A1 must be V_{IL} (see Table 2).

The autoselect mode also facilitates the determination of sector group protection in the system. By performing a read operation at the address location XX02H with the higher order address bits A18, A19, and A20 set to the desired sector group address, the device will return 01H for a protected sector group and 00H for a non–protected sector group.

Table 1. User Bus Operations (see Note 1)

Operation	CE	OE	WE	A0	A1	A6	A9	I/O	RESET	Notes
Auto–Select Manufacturer Code	L	L	H	L	L	L	V_{ID}	Code	H	2
Auto–Select Device Code	L	L	H	H	L	L	V_{ID}	Code	H	2
Read	L	L	H	A0	A1	A6	A9	D_{out}	H	
Standby	H	X	X	X	X	X	X	High Z	H	
Output Disable	L	H	H	X	X	X	X	High Z	H	
Write	L	H	L	A0	A1	A6	A9	D_{in}	H	3
Enable Sector Protect	L	V_{ID}	L	X	X	X	V_{ID}	X	H	
Verify Sector Protect	L	L	H	L	H	L	V_{ID}	Code	H	4
Temporary Sector Group Unprotect	X	X	X	X	X	X	X	X	V_{ID}	
Hardware Reset/Standby	X	X	X	X	X	X	X	High–Z	L	

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care. See DC Characteristics for voltage levels.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Tables 2 and 3.
3. Refer to Table 4 for valid D_{in} during a write operation.
4. Refer to Sector Protection section.

Table 2. Autoselect and Sector Protection Verify Codes

Type	A18	A19	A20	A6	A1	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer Code	X	X	X	V_{IL}	V_{IL}	V_{IL}	01H	0	0	0	0	0	0	0	1
Device Code	X	X	X	V_{IL}	V_{IL}	V_{IH}	ADH	1	0	1	0	1	1	0	1
Sector Protection Verify	Sector Addresses			V_{IL}	V_{IH}	V_{IL}	01H*	0	0	0	0	0	0	0	1

*Outputs 01H at protected sector addresses.

WRITE

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing WE to V_{IL}, while CE is at V_{IL} and OE is at V_{IH}. Addresses are latched on the falling edge of WE or CE, whichever happens later; while data is latched on the rising edge of WE or CE, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

SECTOR GROUP PROTECTION

The M29F016 features hardware sector group protection. This feature will disable both program and erase operations in any combination of eight sector groups of memory. Each sector group consists of four adjacent sectors grouped in the following pattern: sectors 0–3, 4–7, 8–11, 12–15, 16–19, 20–23, 24–27, and 28–31 (see Table 4). The sector group protect feature is enabled using programming equipment at the user's site. The device is shipped with all sector groups unprotected. Alternatively, Motorola may program and protect sector groups in the factory prior to shipping the device.

TEMPORARY SECTOR GROUP UNPROTECT

This feature allow temporary unprotection of previously protected sector groups of the M29F016 device in order to change data in–system. The sector group unprotect mode is activated by setting the RESET pin to high voltage (12 V). During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once the 12 V is taken away from The RESET pin, all the previously protected sector groups will be protected again. Refer to Figures 10 and 11.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Table 3 defines the valid register command sequences. Note that the erase suspend (B0H) and erase resume (30H) commands are valid only while the Sector Erase operation is in progress. Moreover, both Reset/Read commands are functionally equivalent, resetting the device to the read mode.

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory.

The device remains enabled for reads until the command register contents are altered.

The device will automatically power–up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Sector Address Tables

	A20	A19	A18	A17	A16	Address Range
SA0	0	0	0	0	0	000000h–00FFFFh
SA1	0	0	0	0	1	010000h–01FFFFh
SA2	0	0	0	1	0	020000h–02FFFFh
SA3	0	0	0	1	1	030000h–03FFFFh
SA4	0	0	1	0	0	040000h–04FFFFh
SA5	0	0	1	0	1	050000h–05FFFFh
SA6	0	0	1	1	0	060000h–06FFFFh
SA7	0	0	1	1	1	070000h–07FFFFh
SA8	0	1	0	0	0	080000h–08FFFFh
SA9	0	1	0	0	1	090000h–09FFFFh
SA10	0	1	0	1	0	0A0000h–0AFFFFh
SA11	0	1	0	1	1	0B0000h–0BFFFFh
SA12	0	1	1	0	0	0C0000h–0CFFFFh
SA13	0	1	1	0	1	0D0000h–0DFFFFh
SA14	0	1	1	1	0	0E0000h–0EFFFFh
SA15	0	1	1	1	1	0F0000h–0FFFFFh
SA16	1	0	0	0	0	100000h–10FFFFh
SA17	1	0	0	0	1	110000h–11FFFFh
SA18	1	0	0	1	0	120000h–12FFFFh
SA19	1	0	0	1	1	130000h–13FFFFh
SA20	1	0	1	0	0	140000h–14FFFFh
SA21	1	0	1	0	1	150000h–15FFFFh
SA22	1	0	1	1	0	160000h–16FFFFh
SA23	1	0	1	1	1	170000h–17FFFFh
SA24	1	1	0	0	0	180000h–18FFFFh
SA25	1	1	0	0	1	190000h–19FFFFh
SA26	1	1	0	1	0	1A0000h–1AFFFFh
SA27	1	1	0	1	1	1B0000h–1BFFFFh
SA28	1	1	1	0	0	1C0000h–1CFFFFh
SA29	1	1	1	0	1	1D0000h–1DFFFFh
SA30	1	1	1	1	0	1E0000h–1EFFFFh
SA31	1	1	1	1	1	1F0000h–1FFFFFh

AUTOSELECT COMMAND

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

Table 4. Sector Group Addresses

	A20	A19	A18	Address Range
SGA0	0	0	0	SA0–SA3
SGA1	0	0	1	SA4–SA7
SGA2	0	1	0	SA8–SA11
SGA3	0	1	1	SA12–SA15
SGA4	1	0	0	SA16–SA19
SGA5	1	0	1	SA20–SA23
SGA6	1	1	1	SA24–SA27
SGA7	1	1	1	SA28–SA31

The device contains an autoselect operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacturer code of 01H. A read cycle from address XX01H returns the device code ADH (see Table 2). All manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit. Furthermore, the write protect status of sectors can be read in this mode. Scanning the sector group addresses (A18, A19, and A20) while (A6, A1, A0) = (0, 1, 0) will produce a logical “1” at the device output DQ0 for a protected sector group.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

BYTE PROGRAMMING

The Flash chip is programmed on a byte–by–byte basis. Programming is a four bus cycle operation. There are two “unlock” write cycles. These are followed by the program set–up command and data write cycles. Addresses are latched on the falling edge of CE or WE, whichever happens later and the data is latched on the rising edge of CE or WE, whichever happens first. The rising edge of CE or WE (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence the system is *not* required to provide further controls or timings. The Flash chip will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to the read mode and addresses are no longer latched. Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time. Hence, data polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored.

Programming is allowed in any sequence and across sector boundaries. Beware that a data 0 cannot be programmed back to a 1. Attempting to do so will probably hang up the device (exceed timing limits), or perhaps result in an apparent success according to the data polling algorithm but a read from reset/read mode will show that the data is still 0. Only erase operations can convert 0s to 1s.

Figure 2 illustrates the Embedded Programming Algorithm using typical command strings and bus operations.

Table 5. Command Definitions

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset/Read	1	XXXXH	F0H										
Reset/Read	3	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	3	5555H	AAH	2AAAH	55H	5555H	90H						
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	Data				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Erase Suspend	1	XXXXH	B0H										
Erase Resume	1	XXXXH	30H										

NOTES:
1. Bus operations are defined in Table 1.
2. RA = Address of the memory location to be read.
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A20, A19, A18, A17, and A16 will uniquely select any sector.
3. RD = Data read from location RA during read operation.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$.
4. Read and Byte program functions to non–erasing sectors are allowed in the erase suspend mode.
5. Address bits A15, A14, A13, A12, and A11 = X = don't care.

CHIP ERASE

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set–up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does *not* require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last WE pulse in the command sequence and terminates when the data on DQ7 of each byte is 1 (see Write Operation Status section) at which time the device returns to read the mode.

Figure 3 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

SECTOR ERASE

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set–up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of WE, while the command (data) is latched on the rising edge of WE. A time–out of 50 µs from the rising edge of the last sector erase command will initiate the sector erase command(s).

CAUTION

Do not attempt to write an invalid command sequence during the sector erase timeout. Otherwise, it will terminate the sector erase operation and the device will reset back into the read mode.

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the sector erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 50 µs, otherwise that command will not be accepted. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re–enabled after the last sector erase command is written. A time–out of 50 µs from the rising edge of the last WE will initiate the execution of the sector erase command(s). If another falling edge of the WE occurs within the 50 µs time–out window the timer is reset. (Monitor DQ3 to determine if the sector erase window is still open, see section DQ3, Sector Erase Timer). Any command other than sector erase or erase suspend during this period will reset the device to read mode, ignoring the previous command string. Resetting the device after it has begun execution will result in the data of the operated sectors being undefined. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (1 to 8).

Sector erase does *not* require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations. A reset command will terminate the sector erase but the data in the sector will be undefined. In that case, perform the sector erase operation again and allow it to complete

The automatic sector erase begins after the 50 µs time out from the rising edge of the WE pulse for the last sector erase command pulse and terminates when the data on DQ7 of each byte is 1 (see Write Operation Status section) at which time the device returns to read mode. Data polling must be performed at an address within any of the sectors being erased.

Figure 3 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

ERASE SUSPEND

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads or programs to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time–out period for sector erase. The Erase Suspend command will be ignored if written during the Chip Erase operation or Embedded Program Algorithm. Writing the Erase Suspend command during the Sector Erase time–out results in immediate termination of the time–out period and suspension of the erase operation.

Any other command written during the Erase Suspend mode will be ignored except the Erase Resume command. Writing the Erase Resume command resumes the erase operation. The addresses are “don’t–cares” when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of 15 µs to suspend the erase operation. When the device has entered the erase–suspended mode, the RY/BY output pin and the DQ7 bit will be at logic 1, and DQ6 will stop toggling. The user must use the address of the erasing sector for reading DQ6 and DQ7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the device defaults to the erase–suspend–read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase–suspended. Successively reading from the erase–suspended sector while the device is in the erase–suspend–read mode will cause DQ2 to toggle. (See the section on DQ2).

After entering the erase–suspend–read mode, the user can program the device by writing the appropriate command sequence for Byte Program. This program mode is known as the erase–suspend–program mode. Again, programming in this mode is the same as programming in the regular Byte Program mode except that the data must be programmed to sectors that are not erase–suspended. Successively reading from the erase–suspended sector while the device is in the erase–suspend–program mode will cause DQ2 to toggle. The end of the erase–suspended program operation is detected by the RY/BY output pin, Data Polling of DQ7, or by the Toggle Bit I (DQ6) which is the same as the regular Byte Program operation. Note the DQ7 must be read from the byte program address while DQ6 can be read from any address.

To resume the operation of Sector Erase, the Resume command (30H) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

WRITE OPERATION STATUS

DQ7
Data Polling

The device features data polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed.

During the Embedded Program Algorithm an attempt to read the device will produce the complement data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7. Data polling is valid after the rising edge of the fourth WE pulse in the four write pulse sequence.

During the Embedded Erase Algorithm, an attempt to read the device will produce a 0 at the DQ7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a 1 at the DQ7 output.

Data polling will also flag the entry into erase suspend. DQ7 will switch “0” to “1” at the start of the erase suspend mode. Please note that the address of an erasing sector must be applied in order to observe DQ7 in the erase suspend mode.

During program in erase suspend, data polling will perform the same as in regular program execution outside of the suspend mode.

For chip erase, the data polling is valid after the rising edge of the sixth WE pulse in the six write pulse sequence. For sector erase, the data polling is valid after the last rising edge of the sector erase WE pulse. data polling must be performed at sector address within any of the sectors being erased and **not** a protected sector. Otherwise, the status may not be valid. Once the Embedded Algorithm operation is close to being completed, the data pins (DQ7) may change asynchronously while the output enable (OE) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then that byte’s valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and DQ7 has a valid data, the data outputs on DQ0 – DQ6 of each byte may be still invalid. The valid data on DQ0 – DQ7 will be read on the successive read attempts.

The data polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time–out (see Table 5).

See Figure 5 for the data polling timing specifications and diagrams.

DQ6
Toggle Bit

The device also features the “Toggle Bit” as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read (OE toggling) data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on *the next* successive attempt. During programming, the

toggle bit is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. For chip erase, the toggle bit is valid after the rising edge of the sixth WE pulse in the six write pulse sequence. For sector erase, the toggle bit is valid after the last rising edge of the sector erase WE pulse. The toggle bit is active during the sector time out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 2 µs and then stop toggling without the data having changed. In erase, the device will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 100 µs and then drop back into read mode, having changed none of the data.

Either CE or OE toggling will cause the DQ6 to toggle.

See Figure 6 for the toggle bit timing specifications and diagrams.

DQ5
Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ5 will produce a 1. This is a failure condition which indicates that the program or erase cycle was not successfully completed. data polling is the only operating function of the device under this condition. The CE circuit will partially power down the device under these conditions. The OE and WE pins will control the output disable functions as described in Table 1.

If this failure condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused, however, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this failure condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this failure condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused). The device must be reset to use the other sectors.

The DQ5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ7 bit and DQ6 never stops toggling. Once the device has exceeded timing limits, the DQ5 bit will indicate a 1. Please note that this is not a device failure condition since the device was incorrectly used. The device must be reset to continue using the device.

DQ3
Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time–out will begin. DQ3 will remain low until the time–out is complete. data polling and toggle bit are valid after the initial sector erase command sequence.

If data polling or the toggle bit indicates the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is high (1) the internally controlled erase cycle has begun; attempts to write subsequent sector erase commands to the device will be ignored until the erase operation is completed as indicated by data polling or toggle bit. If DQ3 is low (0), the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted.

Refer to Table 6: Write Operation Status.

Table 6. Write Operation Status

	Status		DQ7	DQ6	DQ5	DQ3	DQ2
In Progress	Byte Program in Embedded Program Algorithm		DQ7	Toggle	0	0	1
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	1	Toggle (Note 1)
		Erase Suspend Read (Non–Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non–Erase Suspended Sector)	DQ7	Toggle (Note 2)	0	1	1 (Note 3)
Exceeded Time Limits	Byte Program in Embedded Erase Algorithm		DQ7	Toggle	1	0	1
	Program/Erase in Embedded Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non–Erase Suspended Sector)	DQ7	Toggle	1	1	N/A

NOTES:
1. Performing successive read operations from the erase–suspended sector will cause DQ2 to toggle.
2. Performing successive read operations from any address will cause DQ6 to toggle.
3. Reading the byte address being programmed while in the erase–suspend program mode will indicate logic “1” at the DQ2 bit. However, successive reads from the erase–suspended sector will cause DQ2 to toggle.

DQ2
Toggle Bit II

This toggle bit, along with DQ6, can be used to determine whether the device is in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ2 to toggle during the Embedded Erase Algorithm. If the device is in the erase–suspended–read mode, successive reads from the erase–suspend sector will cause DQ2 to toggle. When the device is in the erase–suspended program mode, successive reads from the byte address of the non–erase suspended sector will indicate the logic '1' at the DQ2 bit.

DQ6 is different from DQ2 in that DQ6 toggles only when the standard program or erase, or erase suspend program operation is in progress. The behavior of these two status bits, along with that of DQ7, is summarized as follows:

Mode	DQ7	DQ6	DQ2
Program	DQ7	toggles	1
Erase	0	toggles	toggles
Erase Suspend Read (1) (Erase Suspended Sector)	1	1	toggles
Erase Suspend Program	DQ7 (2)	toggles	1 (2)

NOTES:
1. These status flags apply when outputs are read from a sector that has been erase–suspended.
2. These status flags apply when outputs are read from the byte address of the non–erase suspended sector.

For example, DQ2 and DQ6 can be used together to determine the erase–suspend–read mode (DQ2 toggles while DQ6 does not). See also Table 6 and Figure 12.

Furthermore, DQ2 can also be used to determine which sector is being erased. When the device is in the erase mode, DQ2 toggles if this bit is read from the erasing sector.

RY/$\overline{BY}$
Ready/Busy

The device provides a RY/$\overline{BY}$ open–drain output pin as a way to indicate to the host system that the Embedded Algorithms are either in progress or has been completed. If the output is low, the device is busy with either a program or erase operation. If the output is high, the device is ready to accept any read/write or erase operation. When the RY/BY pin is low, the device will not accept any additional program or erase commands with the exception of the erase suspend command. If the device is placed in an erase suspend mode, the RY/BY output will be high.

During programming, the RY/BY pin is driven low after the rising edge of the fourth WE pulse. During an erase operation, the RY/BY pin is driven low after the rising edge of the sixth WE pulse. The RY/BY pin will indicate a busy condition during the RESET pulse. Refer to Figure 13 for a detailed timing diagram. The RY/BY pin is pulled high in standby mode.

Since this is an open–drain output, several RY/$\overline{BY}$ pins can be tied together in parallel with a pull–up resistor to V_{CC}.

$\overline{RESET}$
Hardware Reset

The device may be reset by driving the $\overline{RESET}$ pin to V_{IL}. The RESET pin must be kept low (V_{IL}) for at least 500 ns. Any operation in progress will be terminated and the internal state machine will be reset to the read mode 20 µs after the RESET pin is driven low. If a hardware reset occurs during a program operation, the data at that particular location will be indeterminate.

When the RESET pin is low and the internal reset is complete, the device goes to standby mode and cannot be accessed. Also, note that all the data output pins are three–stated for the duration of the RESET pulse. Once the RESET pin is taken high, the device requires 500 ns of wake up time until outputs are valid for read access.

The RESET pin may be tied to the system reset input. Therefore, if a system reset occurs during the Embedded Program or Erase Algorithm, the device will be automatically reset to read mode and this will enable the system's microprocessor to read the boot–up firmware from the flash memory.

DATA PROTECTION

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up, the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi–bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power–up and power–down transitions or system noise.

LOW V_{CC} WRITE INHIBIT

To avoid initiation of a write cycle during V_{CC} power–up and power–down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}.

WRITE PULSE "GLITCH" PROTECTION

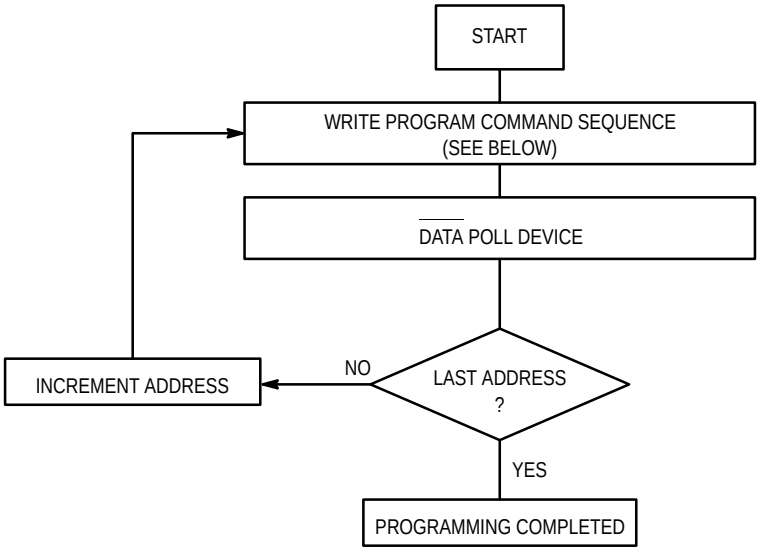
Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

POWER–UP WRITE INHIBIT

Power–up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of WE. The internal state machine is automatically reset to the read mode on power–up.



Program Command Sequence (Address/Command):

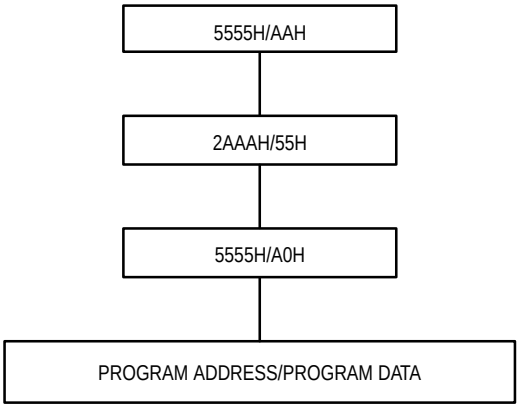


Figure 2. Embedded Programming Algorithm

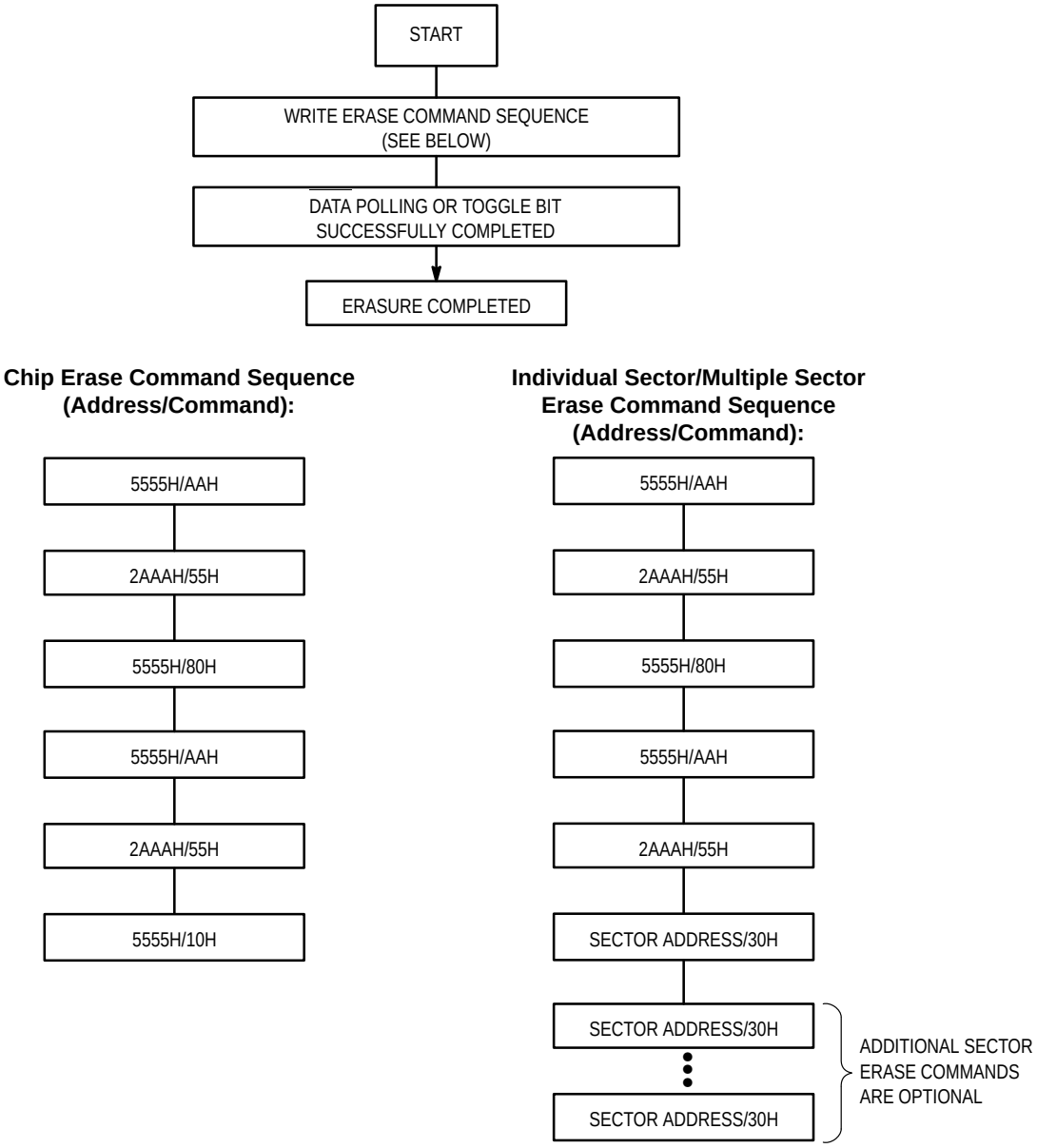
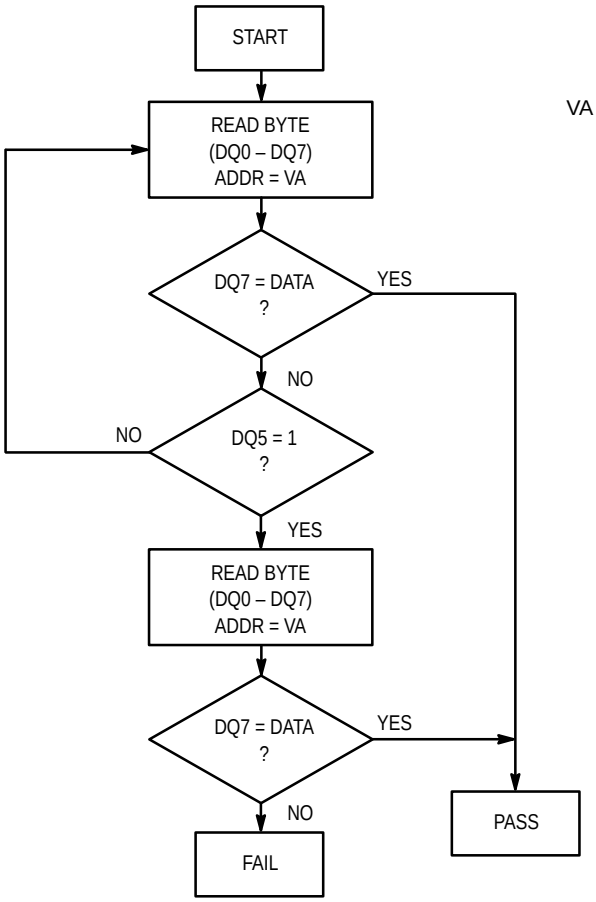


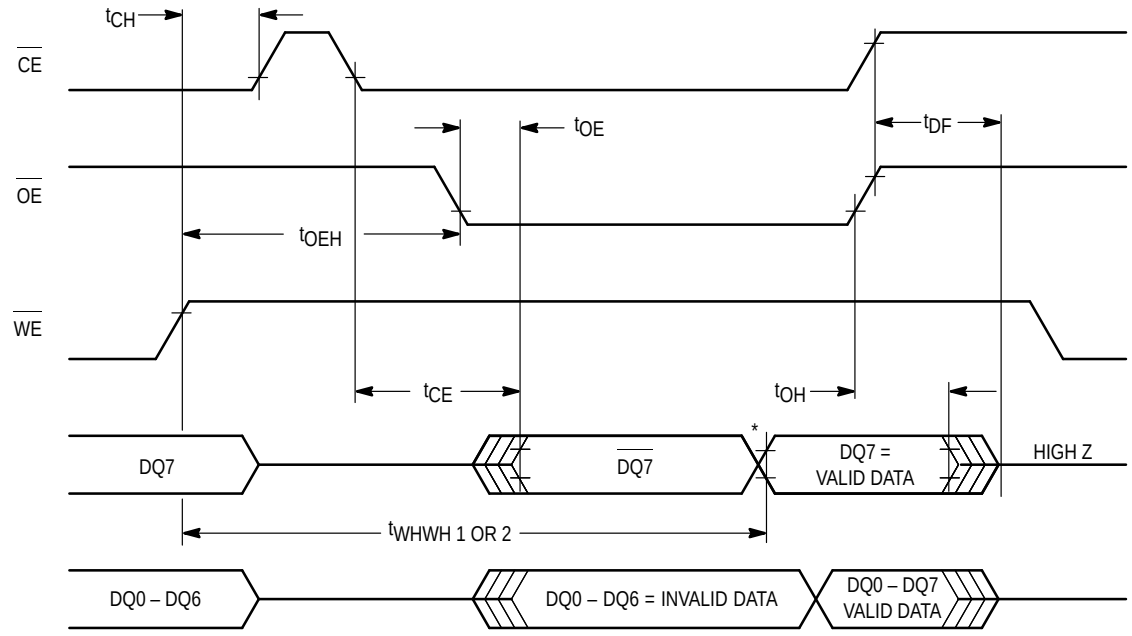
Figure 3. Embedded Erase Algorithm



VA = Byte address for programming
= Any of the sector addresses within the sector being erased during sector erase operation
= XXXXH during chip erase

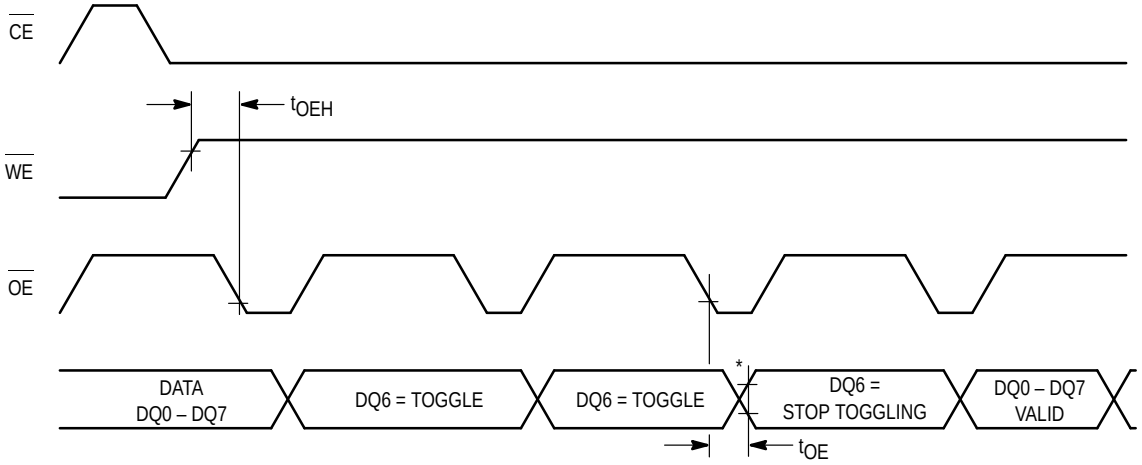
NOTE: DQ7 is rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.

Figure 4. Data Polling Algorithm



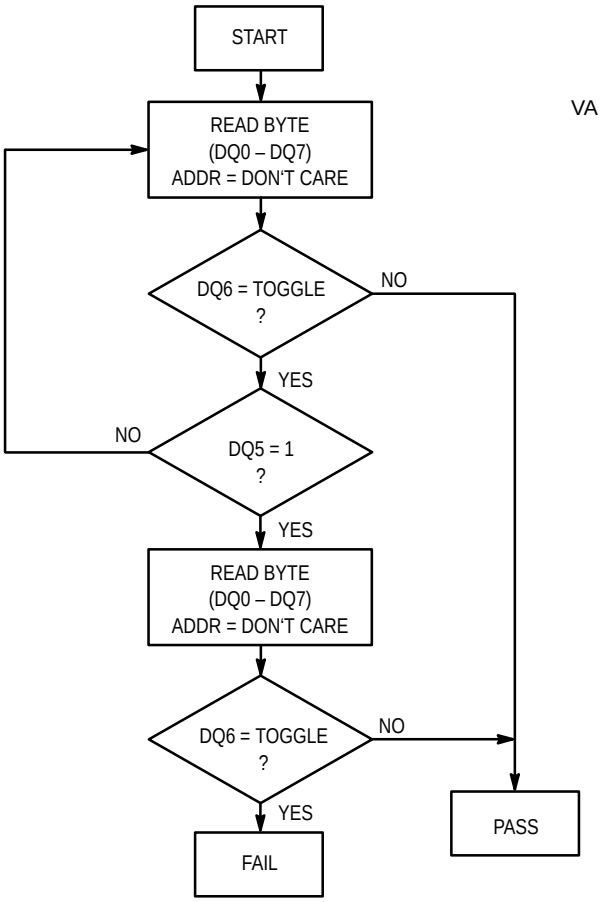
*DQ7 = Valid Data (the device has completed the embedded operation).

Figure 5. AC Waveforms for Data Polling During Embedded Algorithm Operations



*DQ6 Stops Toggling (the device has completed the embedded operation).

Figure 6. AC Waveforms for Toggle Bit During Embedded Algorithm Operations



NOTE: DQ6 is rechecked even if DQ5 = 1 because DQ6 may stop toggling at the same time as DQ5 changing to 1.

Figure 7. Toggle Bit Algorithm

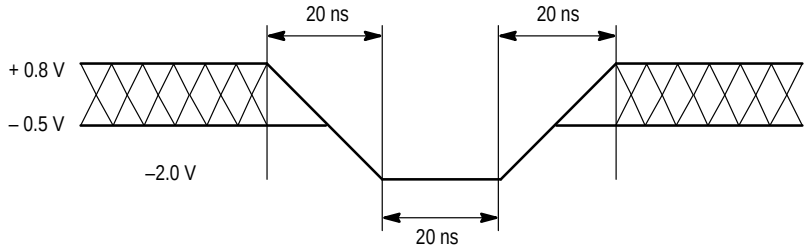


Figure 8. Maximum Undershoot Waveform

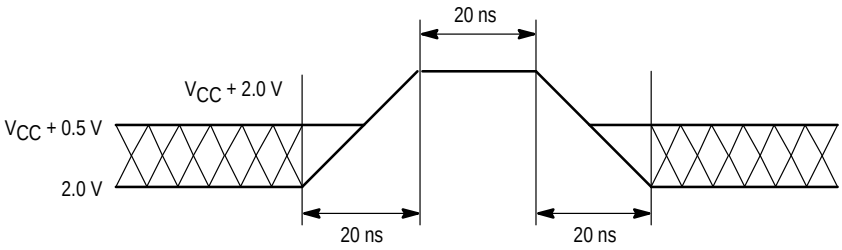
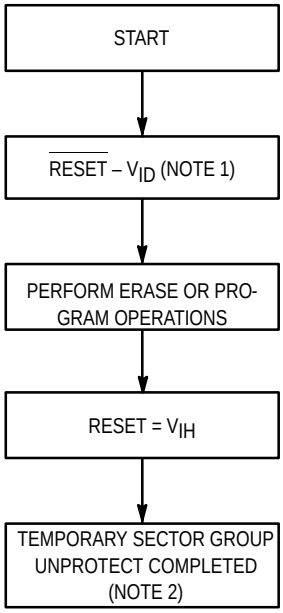


Figure 9. Maximum Overshoot Waveform



NOTE: 1. All protected sector groups unprotected.
2. All previously protected sector groups are protected once again.

Figure 10. Temporary Sector Group Unprotect Algorithm

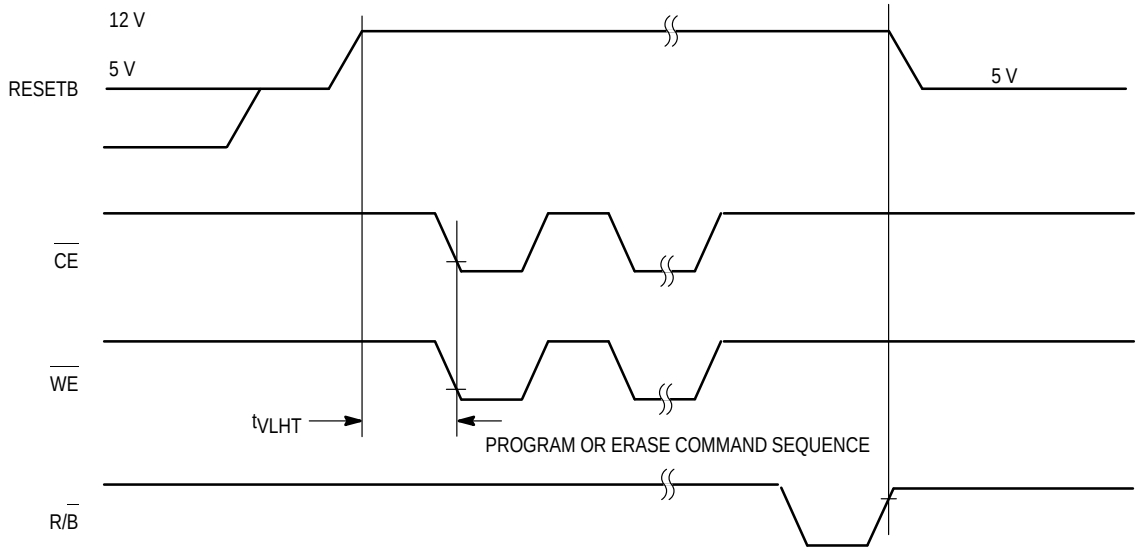
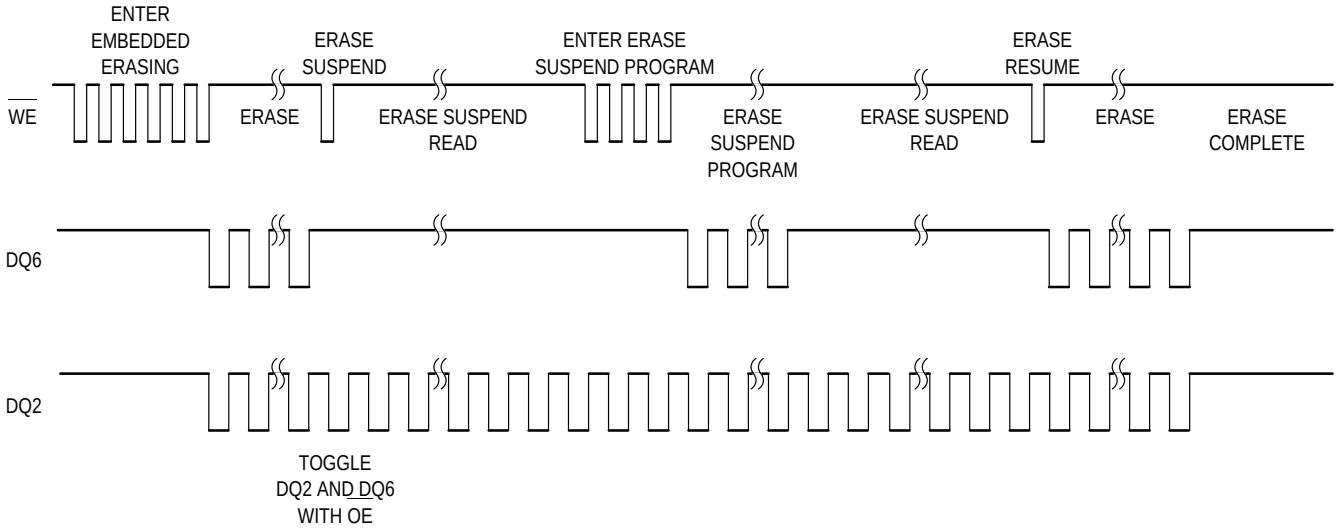


Figure 11. Temporary Sector Group Unprotect



NOTE: DQ2 is read from the erase–suspended sector.

Figure 12. DQ2 vs. DQ6

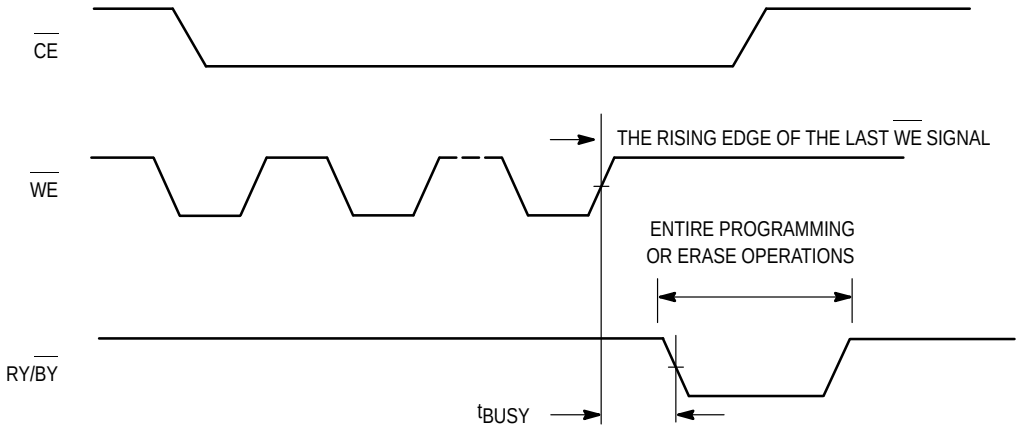


Figure 13. RY/BY Timing Diagram During Program/Erase Operations

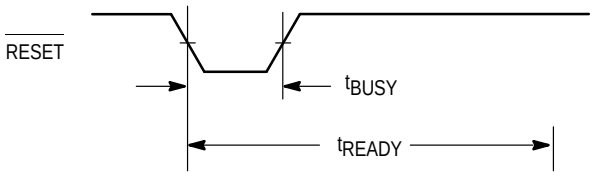
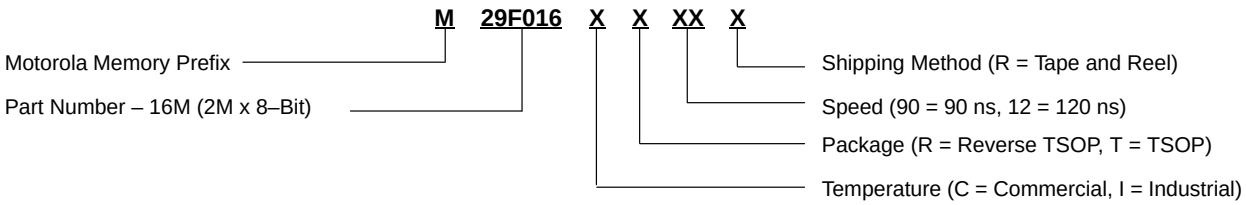


Figure 14. RESET Timing Diagram

ORDERING INFORMATION
(Order by Full Part Number)

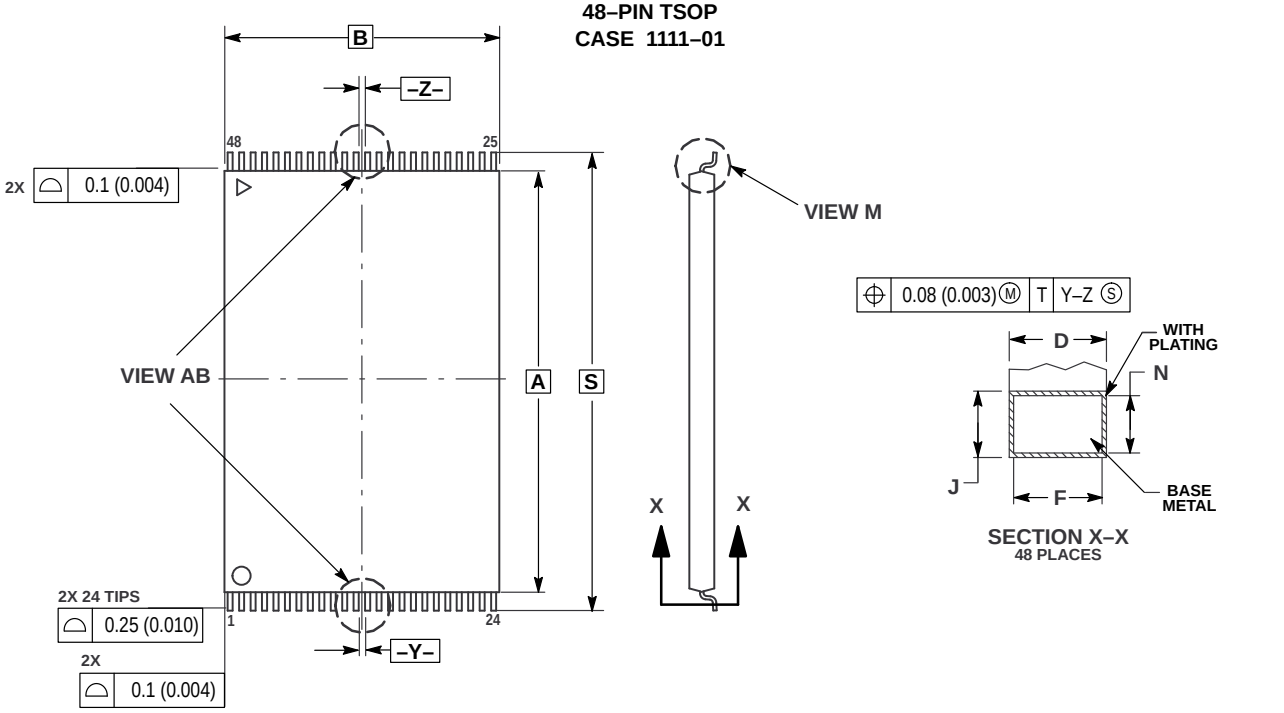


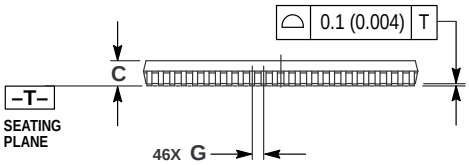
Full Part Numbers —

M29F016CT90	M29F016CT12
M29F016CR90	M29F016CR12
M29F016CT90R	M29F016CT12R
M29F016CR90R	M29F016CR12R
M29F016IT90	M29F016IT12
M29F016IR90	M29F016IR12
M29F016IT90R	M29F016IT12R
M29F016IR90R	M29F016IR12R

PACKAGE DIMENSIONS

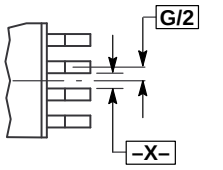
T PACKAGE
48–PIN TSOP
CASE 1111–01



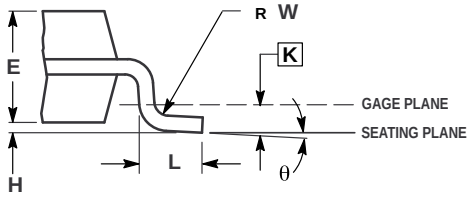


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.40 BSC		0.724 BSC	
B	12.00 BSC		0.472 BSC	
C	—	1.20	—	0.047
D	0.17	0.27	0.007	0.011
E	0.95	1.05	0.037	0.041
F	0.17	0.23	0.007	0.009
G	0.50 BSC		0.020 BSC	
H	0.05	0.15	0.002	0.006
J	0.10	0.21	0.004	0.008
K	0.25 BSC		0.010 BSC	
L	0.50	0.70	0.020	0.028
N	0.10	0.16	0.004	0.006
S	20.00 BSC		0.787 BSC	
W	0.08	0.20	0.003	0.008
θ	0°	5°	0°	5°

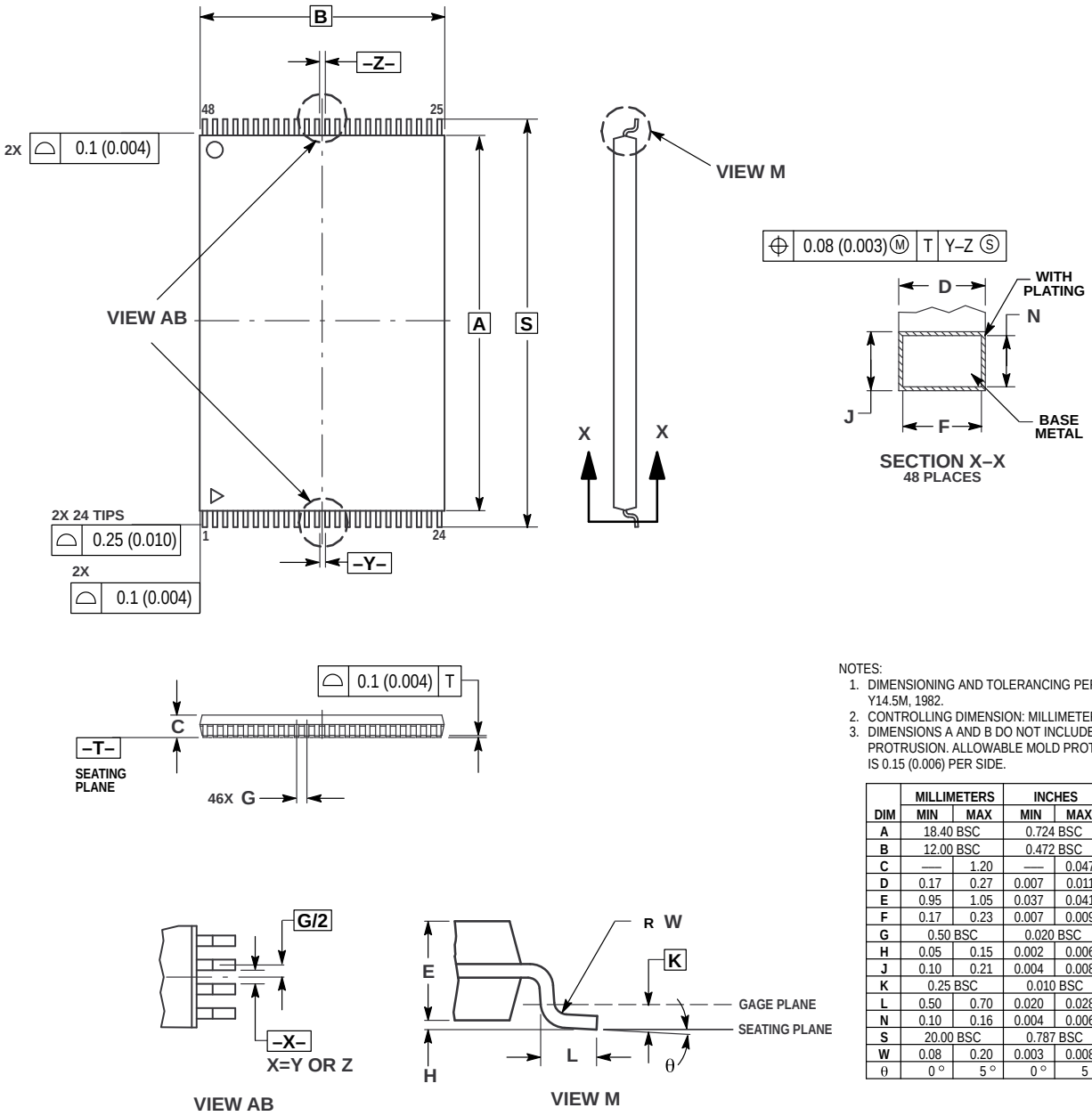


VIEW AB



VIEW M

R PACKAGE
48–PIN REVERSE TSOP
CASE 1111A–01



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S	20.00 BSC		0.787 BSC	
W	0.08	0.20	0.003	0.008
θ	0 °	5 °	0 °	5 °

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