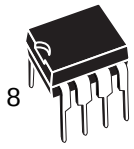
SGS-THOMSON MICROELECTRONICS

M24164

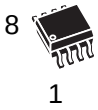
16K SERIAL I²C BUS EEPROM

PRELIMINARY DATA

- TWO WIRE I²C SERIAL INTERFACE SUPPORTS 400kHz PROTOCOL
- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- 2ms TYPICAL PROGRAMMING TIME
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for M24164
  - 2.5V to 5.5V for M24164-W
  - 1.8V to 5.5V for M24164-R
- HARDWARE WRITE CONTROL
- BYTE and PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH-UP PERFORMANCES



PSDIP8 (BN)
0.25mm Frame



SO8 (MN)
150mil Width

DESCRIPTION

The M24164 is a 16K bit EEPROM. The memory is an electrically erasable programmable memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology which guarantees an endurance typically well above one million erase/write cycles with a data retention of 40 years. The "-W" version operate with a power supply value as low as 2.5V and the "-R" version operate down to 1.8V.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Table 1. Signal Names

E0-E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

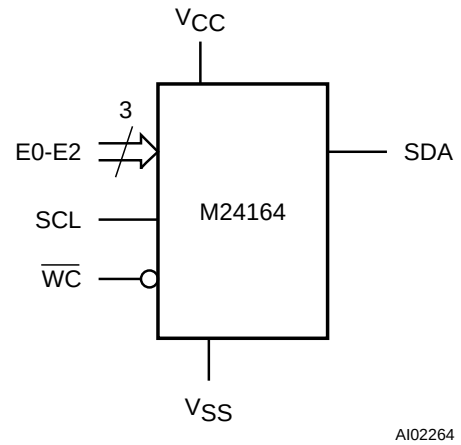


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient OperatingTemperature(2)			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(PSDIP8 package) (SO8 package)	10 sec 40 sec	260 215	°C
V_{IO}	Input or Output Voltages			–0.6 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (3)			4000	V
	Electrostatic Discharge Voltage (Machine model) (4)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Depends on range.
3. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
4. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

Figure 2A. DIP Pin Connections

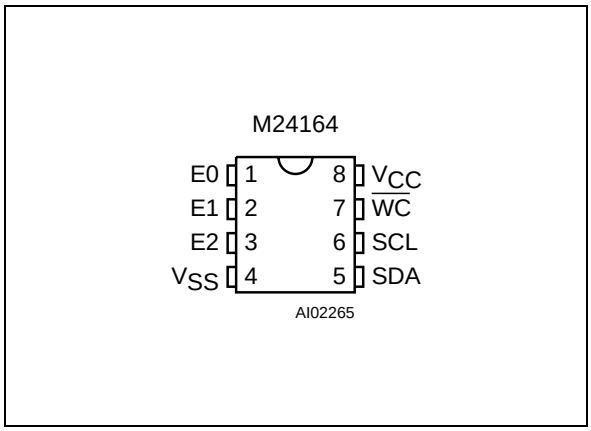
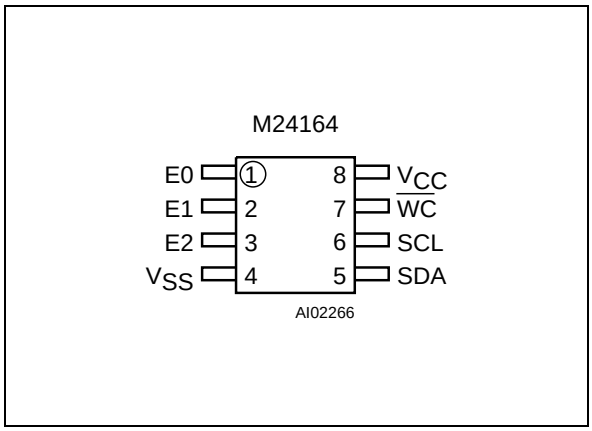


Figure 2B. SO Pin Connections



DESCRIPTION (cont'd)

The memory is compatible with the two wire serial interface which uses a bi-directional data bus and serial clock. The memory offers 3 chip enable inputs (E2, E1, E0) so that up to 8 x 16K devices may be attached to the bus and selected individually. The memory behaves as a slave device with all memory operations synchronized by the serial clock.

Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits, plus one read/write bit and terminated by an acknowledge bit (see Table 3). When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent any possible data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

Table 3. Device Select Code

		Chip Enable			MSB Address			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	E2	$\overline{E1}$	E0	A10	A9	A8	R$\overline{W}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	RW bit	WP	Data Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, R$\overline{W}$ = '1'
Random Address Read	'0'	X	1	START, Device Select, R$\overline{W}$ = '0', Address,
	'1'	X		reSTART, Device Select, R$\overline{W}$ = '1'
Sequential Read	'1'	X	≥ 1	As CURRENT or RANDOM Mode
Byte Write	'0'	V_{IL}	1	START, Device Select, R$\overline{W}$ = '0'
Page Write	'0'	V_{IL}	≤ 16	START, Device Select, R$\overline{W}$ = '0'

Note: 1. X = V_{IH} or V_{IL}.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E2 - E0). These chip enable inputs are used to set 3 bits (b6, b5, b4) of the 7 bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Write Control ($\overline{WC}$). A hardware Write Control pin ($\overline{WC}$) is provided on pin 7 of the memory. This feature is useful to protect the entire contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$=V_{IL}) or disable ($\overline{WC}$=V_{IH}) write instructions to the entire memory area. When unconnected, the $\overline{WC}$ input is internally read as V_{IL} and write operations are allowed. When $\overline{WC}$=1, Device Select and Address bytes are acknowledged, Data bytes are not acknowledged.

Refer to Application Note AN404 for more detailed information about Write Control feature.

DEVICE OPERATION

I^2C Bus Background

The memory supports the I^2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The memory is always a slave device in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the memory continuously monitors the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the memory and the bus master. A STOP condition at the end of a Read sequence, after and only after a No-Acknowledge, forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the memory samples the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation, the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave memory, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the Device Select code (7 bits) and a READ or WRITE bit.

Three out of the four most significant bits of the Device Select code are the Device Select bits (b6, b5, b4). They are matched to the chip enable signals applied on pins E2, $\overline{E1}$, E0. Thus up to 8 x 16K memories can be connected on the same bus giving a memory capacity total of 128K bits.

After a START condition any memory on the bus will identify the device code and compare the 3 bits to its chip enable inputs E2, $\overline{E1}$, E0. The 8th bit sent is the read or write bit ($\overline{RW}$).

This bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time. If the memory does not match the Device Select code, it will self-deselect from the bus and go into standby mode.

Write Operations

Following a START condition the master sends a Device Select code with the $\overline{RW}$ bit set to '0'. The memory acknowledges it and waits for a byte address, which provides access to the memory area. After receipt of the byte address, the memory again responds with an acknowledge and waits for the data byte. Writing in the Memory may be inhibited if input pin $\overline{WC}$ is taken high.

Any write command with $\overline{WC}$=1 (during a period of time from the START condition until the Acknowledge of the last Data byte) will not modify the memory content and will NOT be acknowledged on data bytes, as shown in Figure 9.

Byte Write. In the Byte Write mode, after the Device Select code and the address, the master sends one data byte. If the addressed location is write protected by the $\overline{WC}$ pin, the memory send a NoACK and the location is not modified. If the $\overline{WC}$ pin is tied to 0, after the data byte the memory sends an ACK. The master terminates the transfer by generating a STOP condition.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

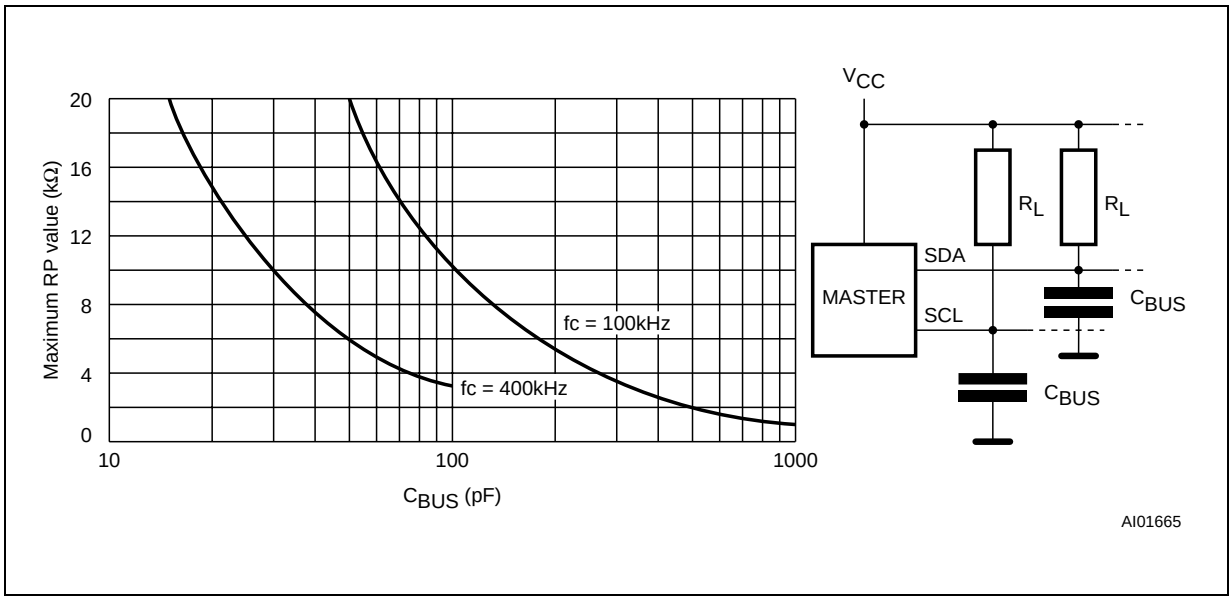


Table 5. Input Parameters (1) (T_A = 25°C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)		200	500	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V, 2.5V to 5.5V or 1.8V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 400kHz (Rise/Fall time < 30ns)		2	mA
	Supply Current (-W series)	V_{CC} = 2.5V, f_C = 400kHz (Rise/Fall time < 30ns)		1	mA
	Supply Current (-R series)	V_{CC} = 1.8V, f_C = 100kHz (Rise/Fall time < 30ns)		0.8	mA
I_{CC1}	Supply Current, Standby	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		20	µA
I_{CC2}	Supply Current, Standby (-W series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		1	µA
I_{CC3}	Supply Current, Standby (-R series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8V		0.1	µA
V_{IL}	Input Low Voltage (SCL, SDA, E2, E1, E0)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA, E2, E1, E0)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage ($\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage ($\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (-W series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V
	Output Low Voltage (-R series)	I_{OL} = 0.15mA, V_{CC} = 1.8V		0.2	V

Table 7. AC Characteristics

Symbol	Alt	Parameter	M24164						Unit
			V_{CC} = 4.5V to 5.5V T_A = 0 to 70°C T_A = –40 to 85°C		V_{CC} = 2.5V to 5.5V T_A = 0 to 70°C T_A = –40 to 85°C		V_{CC} = 1.8V to 5.5V T_A = 0 to 70°C T_A = –40 to 85°C		
			Min	Max	Min	Max	Min	Max	
t_{CH1CH2}	t_R	Clock Rise Time		300		300		1000	ns
t_{CL1CL2}	t_F	Clock Fall Time		300		300		300	ns
t_{DH1DH2} (1)	t_R	SDA Rise Time	20	300	20	300	20	1000	ns
t_{DL1DL2} (1)	t_F	SDA Fall Time	20	300	20	300	20	300	ns
t_{CHDX} (2)	$t_{SU:STA}$	Clock High to Input Transition	600		600		4700		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		600		4000		ns
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	600		600		4000		ns
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		0		0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		1.3		4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	100		100		250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	600		600		4000		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		1.3		4.7		µs
t_{CLQV} (3)	t_{AA}	Clock Low to Next Data Out Valid	200	900	200	900	200	3500	ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		200		200		ns
f_C	f_{SCL}	Clock Frequency		400		400		100	kHz
t_W	t_{WR}	Write Time		5		10		10	ms

Notes: 1. Sampled only, not 100% tested.
2. For a reSTART condition, or following a write cycle.
3. The minimum value delays the falling/rising edge of SDA away form SCL = 1 in order to avoid unwanted START and/or STOP condition.

Table 8. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms

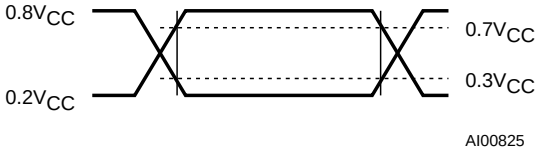
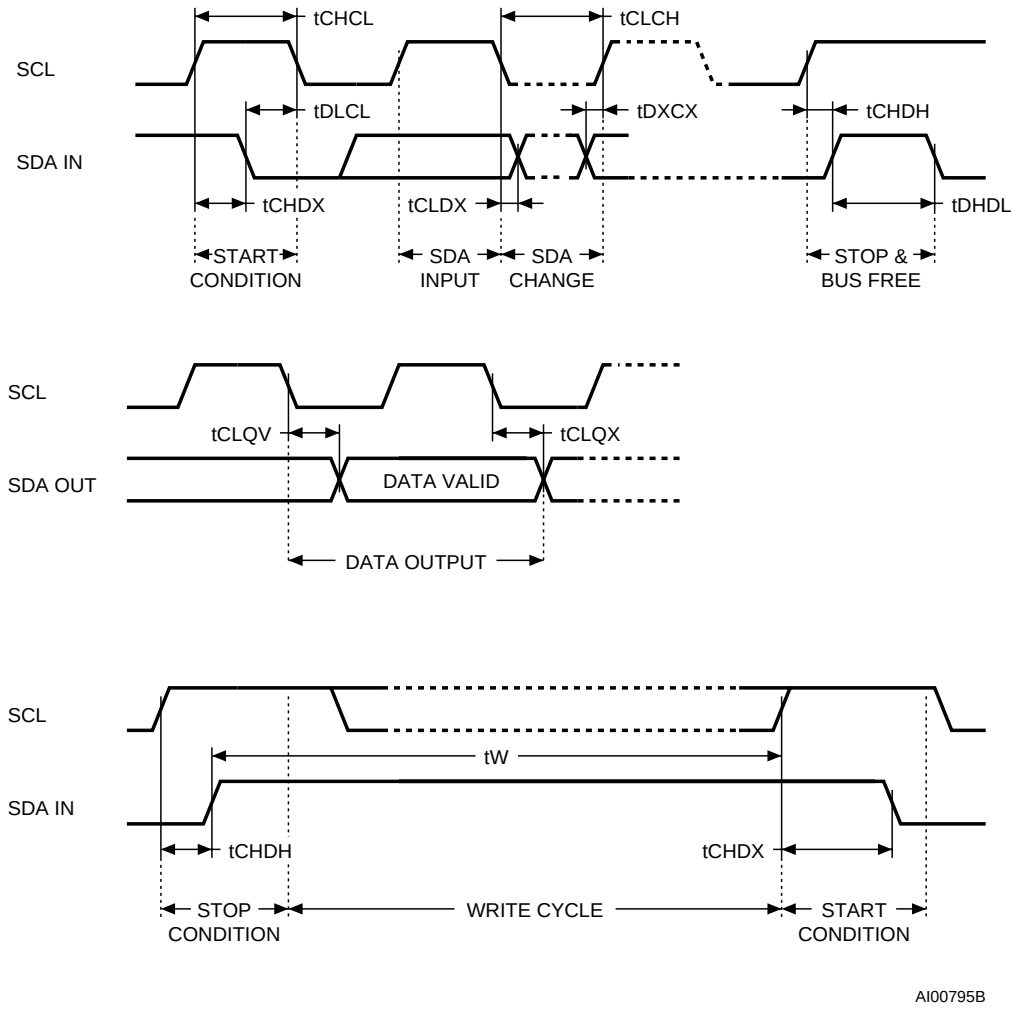
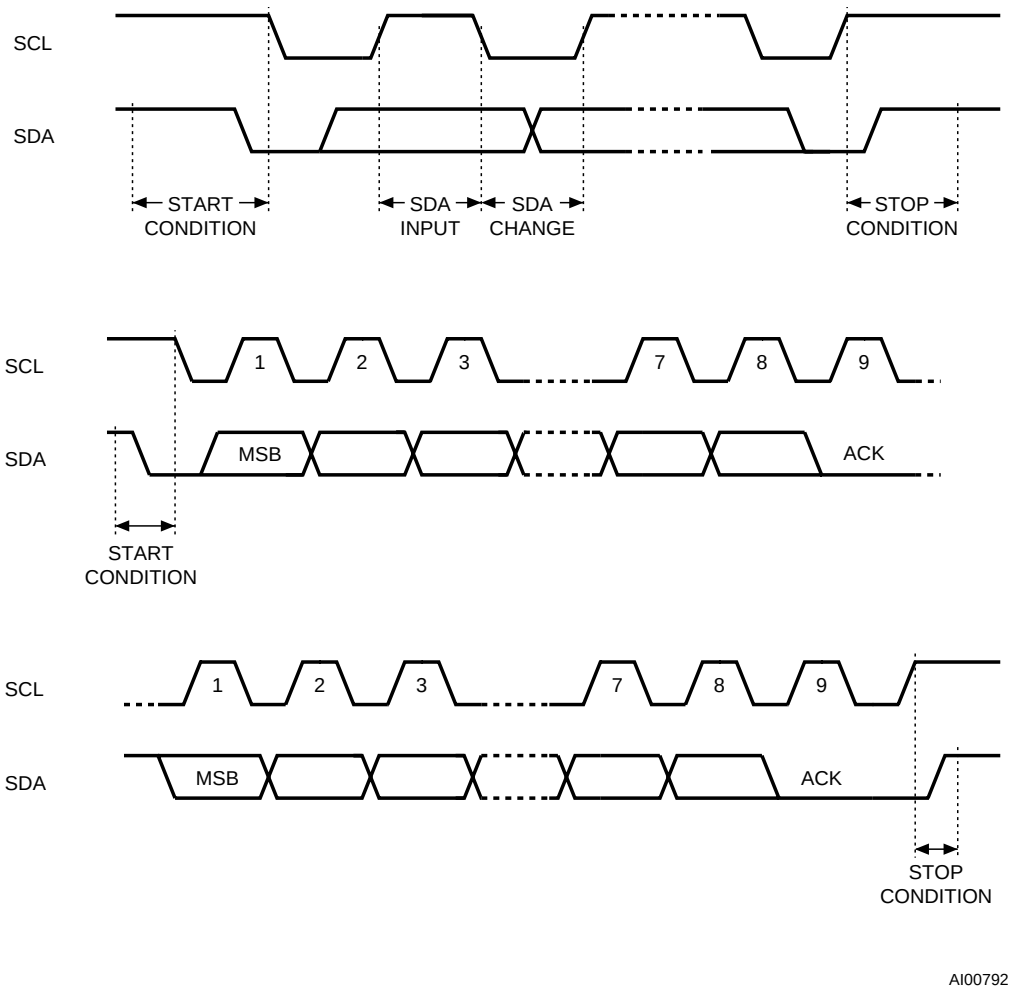


Figure 5. AC Waveforms



Page Write. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the most significant memory address bits are the same. The master sends from one up to 16 bytes of data, each of which is acknowledged by the memory if the $\overline{WC}$ pin is low. If the $\overline{WC}$ pin is high, each data byte is followed by a NoACK and the location will not be modified. After each byte is transferred, the internal byte address counter (4 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any byte or page write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Figure 6. I²C Bus Protocol



Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master. The sequence is:

– Initial condition: a Write is in progress (see Figure 7).
– Step 1: the master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
– Step 2: if the memory is busy with the internal write cycle, NoACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the incoming instruction (the first byte of this instruction was already sent during Step 1).

Figure 7. Write Cycle Polling using ACK

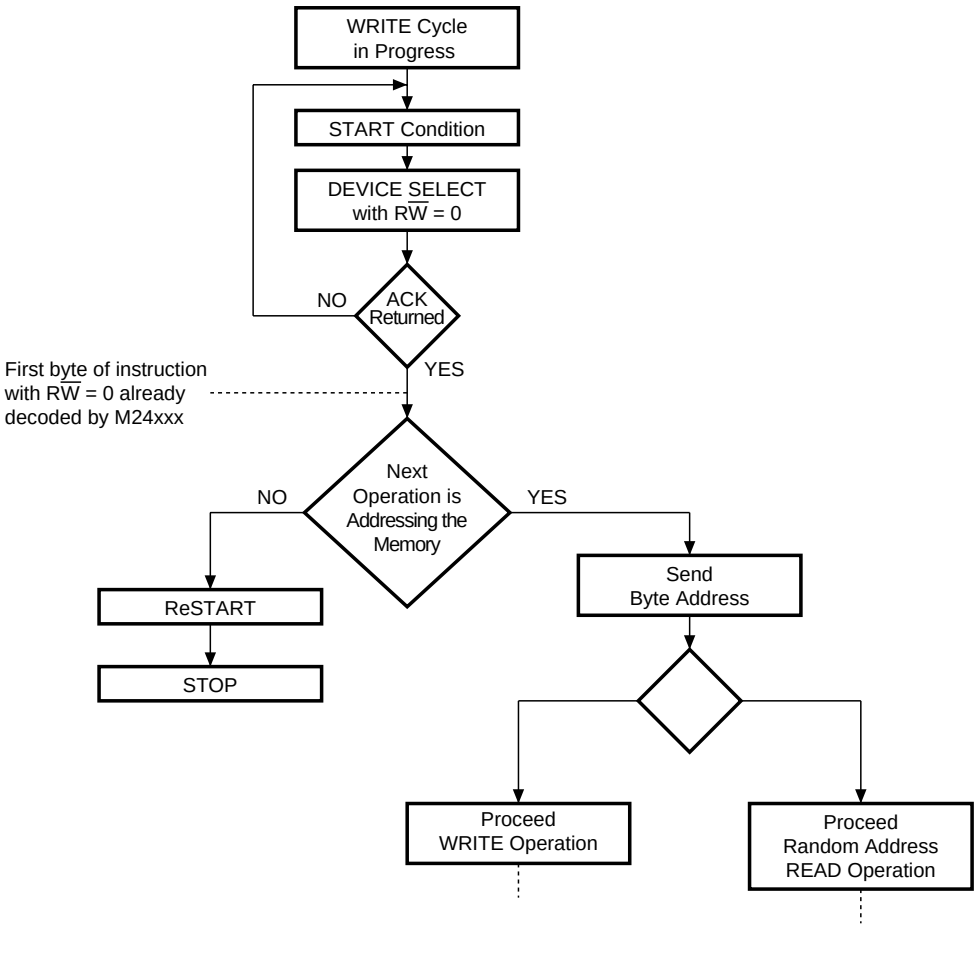
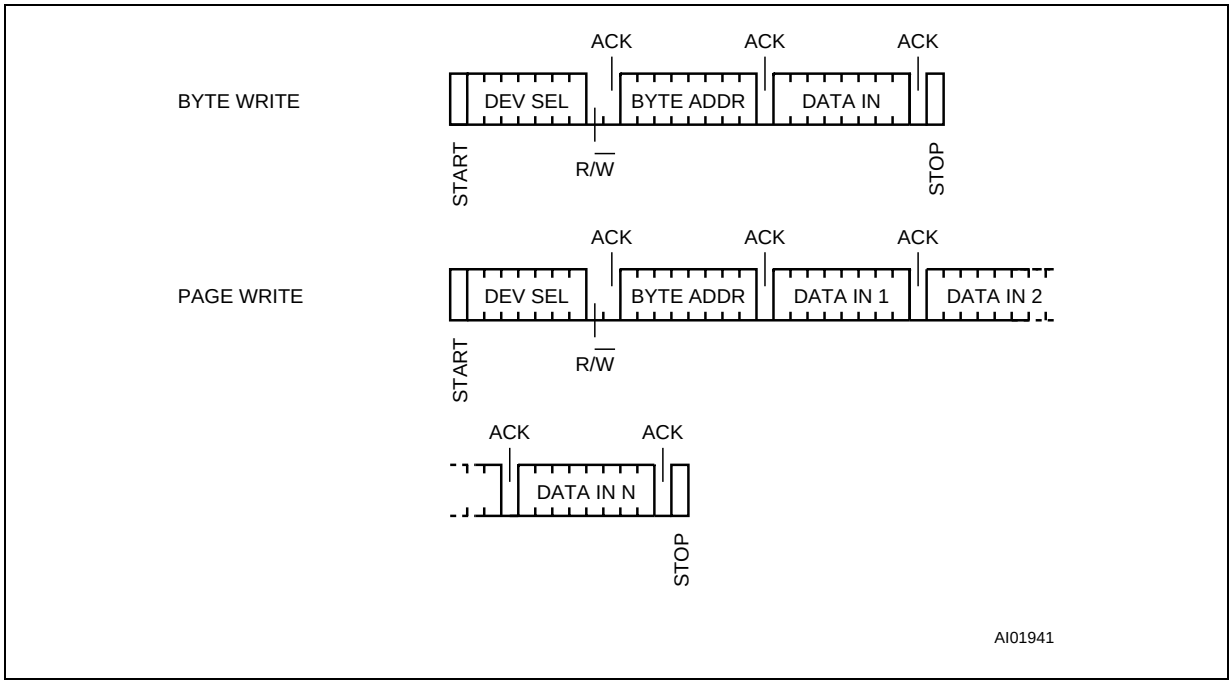


Figure 8. Write Modes Sequence



Read Operations

Read operations are independent from the state of the $\overline{WC}$ input pin. On delivery, the memory contents is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a Device Select code with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master have to NOT acknowledge the byte output and terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the memory address into the address counter, see Figure 10. This is followed by another START condition from the master and the Device Select code is repeated with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master have to NOT acknowledge the byte output and terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output and MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the memory wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the memory terminate the data transfer and switches to a standby state.

Figure 9. Write Modes Sequence with Write Control = 1

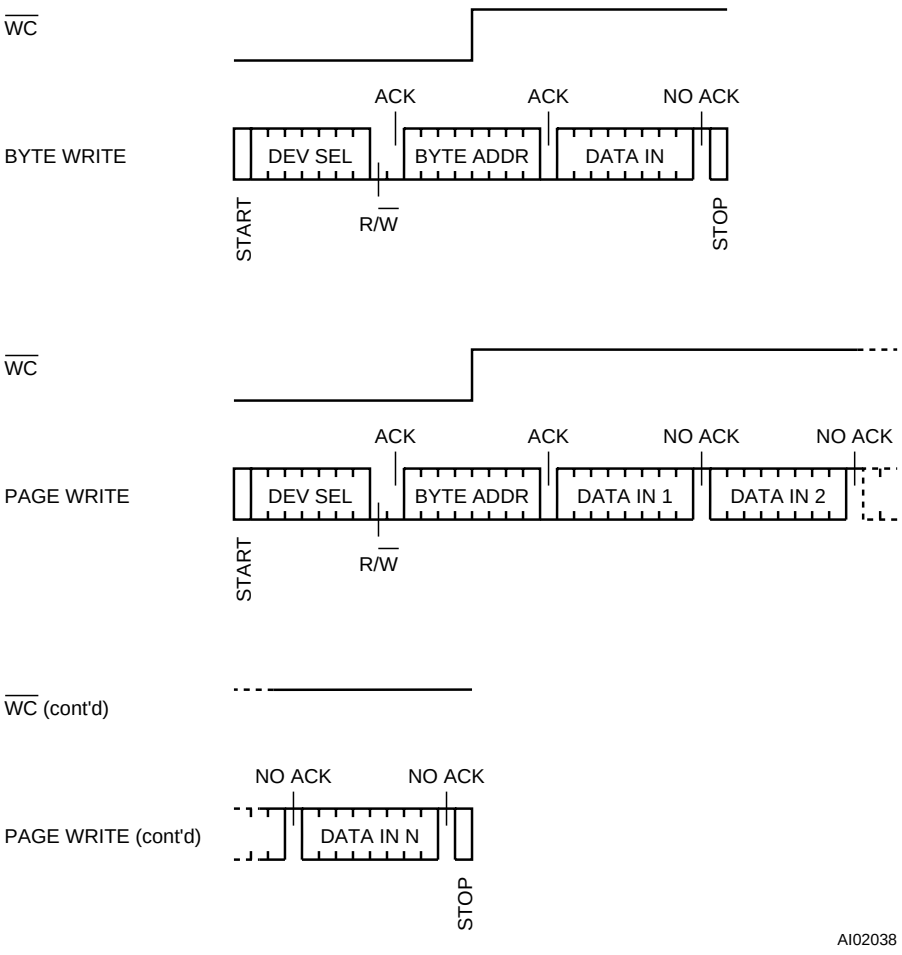
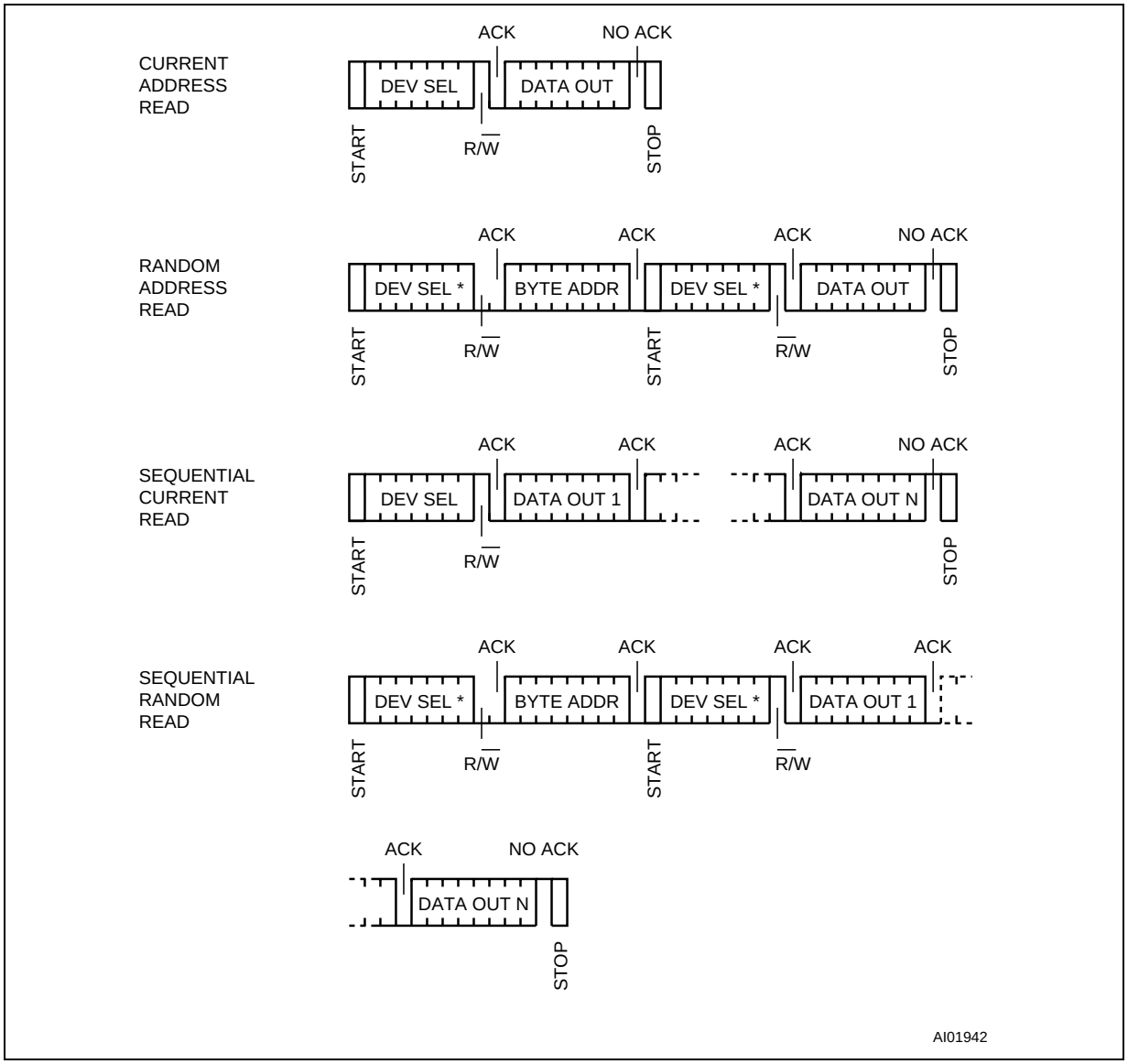


Figure 10. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

ORDERING INFORMATION SCHEME

Example: M24164 – R MN 1 T

Density		Operating Voltage		Package		Temperature Range		Option	
164	16K bit	blank	4.5V to 5.5V	BN	PSDIP8 0.25mm Frame	1 (1)	0 to 70 °C	T	Tape & Reel Packing
		W	2.5V to 5.5V			6	–40 to 85 °C		
		R	1.8V to 5.5V	MN	SO8 150mil Width	3 (2)	–40 to 125 °C		

Notes: 1. Temperature range on request only.
2. Produced with High Reliability Certified Flow (HRCF), in V_{CC} range 4.5V to 5.5V at 100kHz only.

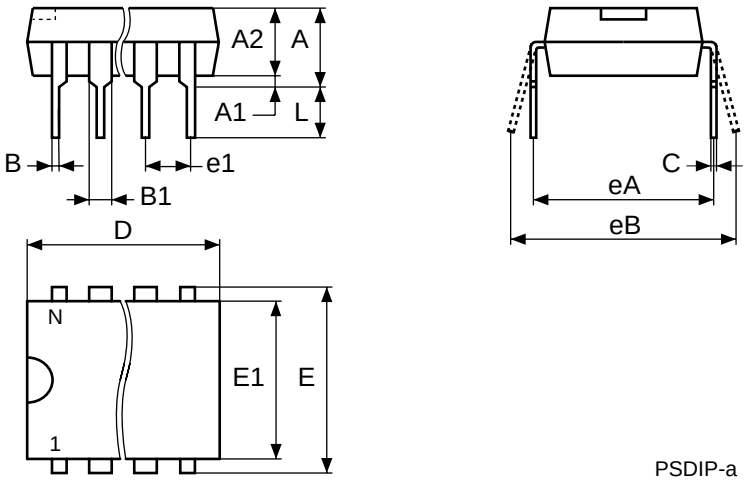
Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



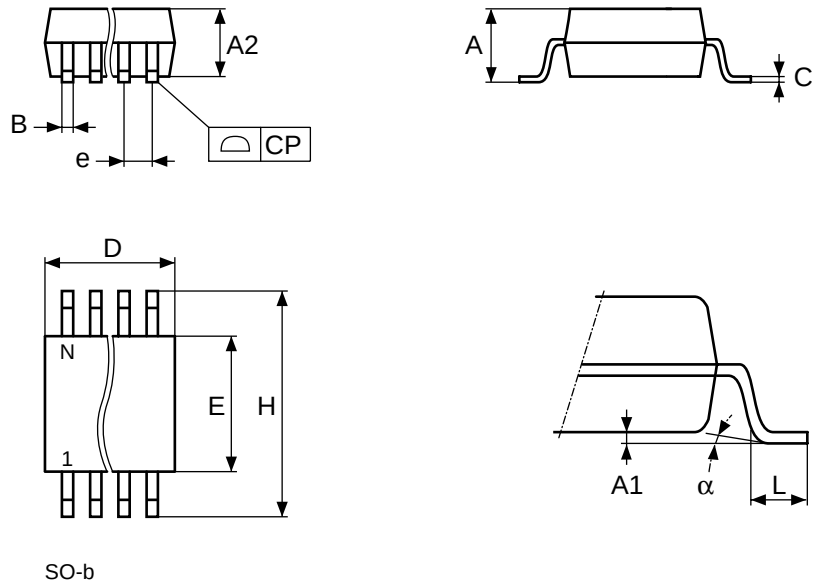
PSDIP-a

Drawing is not to scale.

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8a



SO-b

Drawing is not to scale.