SIEMENS

The Influence of Parasitic Network Parameters on the Switching Behavior of Power MOSFETs when Switching Ohmic/Inductive Loads

1 Introduction

The most important of the effects, which occur when power MOSFETs are switched in electrical networks, are described. The article starts with a discussion of the current and voltage waveforms, disregarding parasitic network and device parameters. After this, the influence of the latter parameters on the switch-on and switch-off processes is considered.

The high switching rate of power FETs, which can be achieved with low drive power and with no device wiring, and their insensitivity to overload makes them appropriate for use in any situation where pulsed operation at a high level of efficiency is required (including switched mode power supplies, UPSs, pulse-width modulation inverters up to about 10 kVA).

By contrast with earlier investigations, which have considered the power semiconductor device as an isolated, ideal driven element, the switching behavior of a power FET is here investigated in conjunction with its typical application environment and shown in parametric form. In this investigation special emphasis has been put on those factors which have a particularly strong effect for short switching times.

The advantage of a parametric representation of the current and voltage waveforms when a power FET is operated in switched mode, taking into account variable parasitic network and device parameters, is that the results have a direct relationship to the network variables and are thus a great help to the application engineer in optimizing the input and output circuits.

2 Switching Behavior of a Power MOSFET under the Assumption of Ideal Network Conditions

2.1 Current and Voltage Waveforms during the Switch-on Process, disregarding Parasitic Network Parameters

To turn a enchancement power FET into the conductive state, the driver circuit must supply the energy $W = C_{in} \times v_{GS}^2/2$. It should be noted that it is difficult to determine the input capacitance C_{in}, because it is non-linear, i.e. is voltage-dependent. To avoid the need for application engineers using this semiconductor device to use voltage-dependent capacitances in the dimensioning calculations for the driver circuit, the “gate charge curve” $v_{GS} = f(Q_G)$ for I_D = const. and V_D = const. is very often given. This curve (see **Figure 2**) gives the change in charge level for a change from the OFF to the ON state. From this it is very easy to calculate the gate current required to switch the FET within any required time.

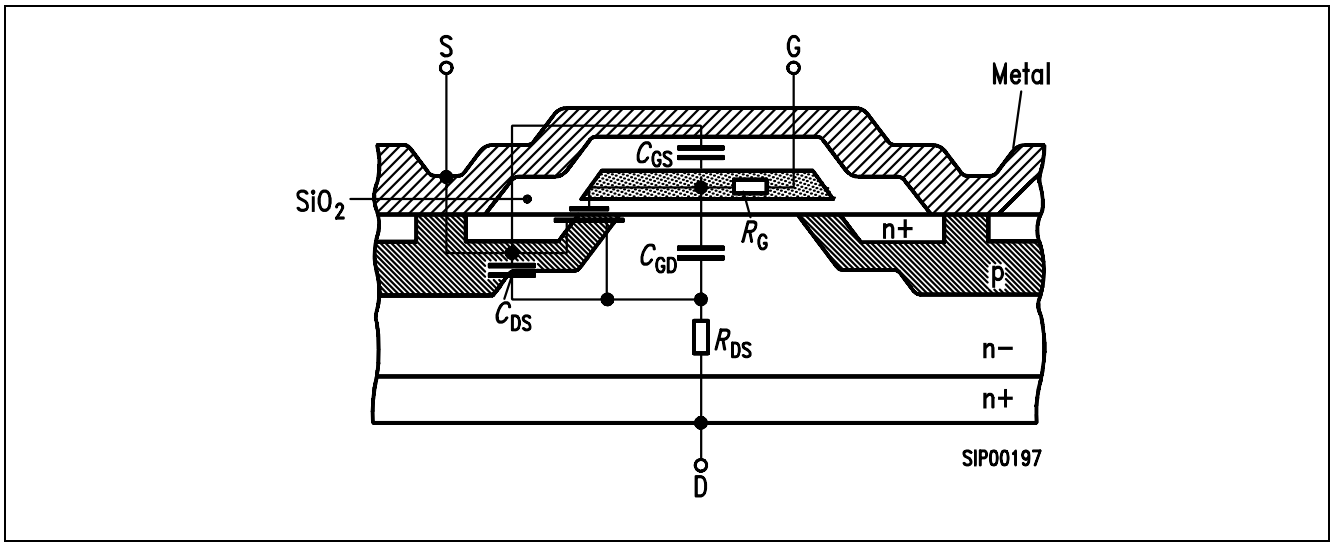

Figure 1
Semiconductor Structogram for a FET Cell Showing the Main Equivalent Electrical Components

Figure 1 shows the semiconductor structogram for a power MOSFET cell, together with the main equivalent circuit components. **Figure 2** shows the circuit diagram of the measuring circuit, and the corresponding current and voltage time waveforms during a switch-on process.

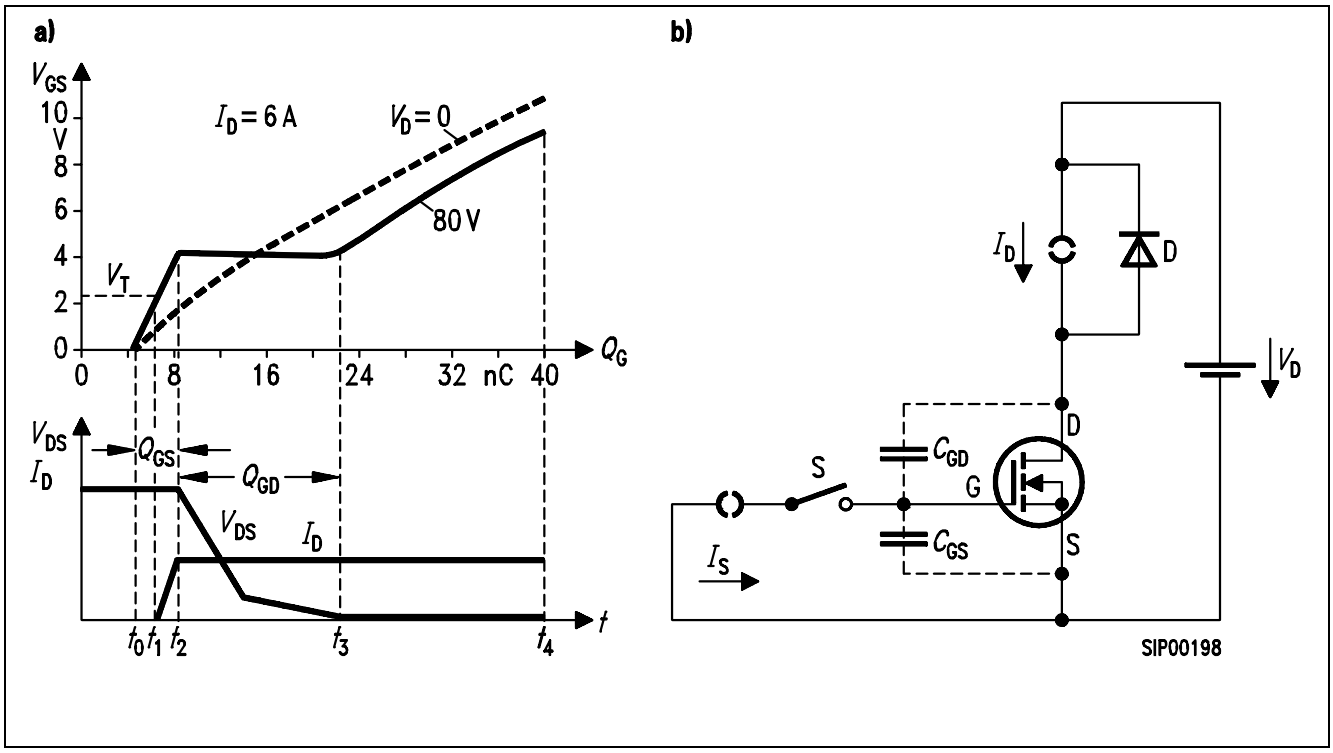

Figure 2
The Gate Charge Curve During the Switch-on Process;
a) $Q_G = f(v_{GS})$ and the Associated Current and Voltage Waveforms
b) The Measuring Circuit

Over the time interval t_0-t_2, $C_{in} \approx C_{GS} + C_{GD}(V_D) \approx$ const. The gate-drain capacitance over this time interval is still relatively small, because almost the entire supply voltage drop V_D occurs across the transistor, which means that the capacitance of the epitaxial layer dominates relative to the gate-drain oxide capacitance. During the time interval t_1-t_2, the p-channel is inverted, so that an n-conducting channel develops from the drain to the source contact, and the load current commutates from the freewheeling diode into the FET. At time t_2, the freewheeling diode D is in a position to accept a voltage (assuming an ideal diode). Account must be taken here of the fact that the input capacitance is increased due to the voltage amplification factor.

The following applies:

$$C_{in} = C_{GS} + C_{GD}\,(1 + |\partial v_{DS}/\partial v_{GS}|) \qquad \textbf{equation 1}$$

The steepness of the fall in the drain-source voltage is determined by the driver current. The kink in the drain-source voltage waveform shows clearly the substantial increase in the capacitance C_{GD} at $v_{GS} \approx v_{DS}$ (see **Figure 4**). This arises because of the fact that at $v_{GS} > V_{DS}$ the epitaxial layer is enriched with charge carriers and thus no longer represents a dielectric. At $v_{DS} = i_D \times R_{DSon}$ only the C_{GD} oxide capacitance, which is significantly larger than the depletion layer capacitance of the epitaxial layer, still has any effect.

At time t_3, the switch-on process is complete. The drain residual voltage is $v_{DS} = I_D \times R_{DS}$. From time t_3 on, the input capacitance charges up, with a waveform which is approximately linear due to the constant current feed. The slope of the changing curve over the time interval t_3-t_4 is less than over the interval t_0-t_2, because the transistor is gated and acts as an input capacitance $C_{in} = C_{GS} + C_{GD}$ (C_{GD} is the capacitance at $v_{DS} << v_{GS}$).

The gate charging curve can be recorded under approximately ideal network conditions ($Q_{rr} \rightarrow 0$, $R_i \rightarrow 0$, $L_\sigma = L_S \rightarrow 0$) if, for example, the gate charging current I_S is small enough for the switching process to be very slow. However, as the switching times get shorter, the parasitic elements have a particularly strong effect, so that this method must be used only with care in obtaining a complete specification of the switching process.

2.2 Switch-off Behavior, Disregarding Parasitic Network Parameters

Careful investigation of the switch-off behavior shows that, in addition to a displacement of the charging curve, they exhibit a different waveform from that during power-on, and this depends on the circuitry. For this reason the curve $v_{GS} = f(Q_G)$ for the switch-on behavior may not be used as the basis for calculating the capacities in the individual time intervals, or the corresponding times, even by running along it in the negative direction (from $t_4 \rightarrow t_0$). Furthermore, it is found that the rise time for the drain-source voltage is longer for the switch-on process than for the switch-off, because the output capacitance is charged via the load resistance. By contrast, during switch-on there is a low-impedance discharge of this capacitance via the conducting-state FET.

3 Taking Account of the Important Devices and Network Parameters in the Switching Process

The parametric representation has the advantage that it is immediately apparent what the effect is of the individual network parameters (L_σ, L_S, V_D, Q^*_{rr}[1]) t^*_{rr}, R_S, V_0, R_L, I_D) and device parameters (C_{GS}, $C_{GD}(v_{GS}, v_{DS})$, $C_{DS}(v_{DS})$, R_{DS}, R_G, g_{fs}, V_T, bond inductances) on the switching behavior. Whereas the network parameters can be critically affected by the application engineer, by suitable network layout, the device parameters are essentially determined by the choice of semiconductor devices. The influence of temperature, which mainly affects V_T, g_{fs} and R_{DS}, is ignored in the analytical considerations.

3.1 The Electrical Network Considered and Analytical Description of the Switching Behavior

The circuit variant chosen for the network is one which is common in power electronics – see **Figure 3** – and which is particularly suitable for showing the most important effects which occur during switching.

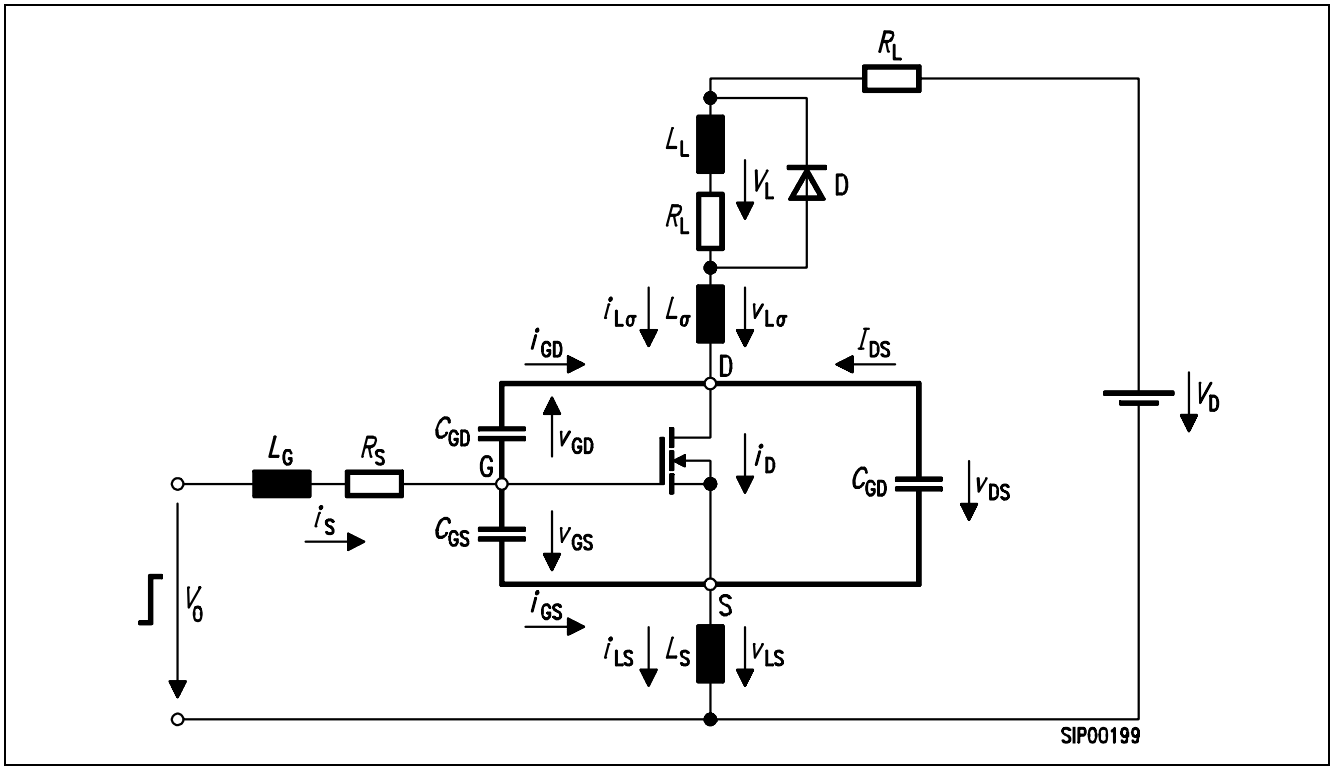

Figure 3
Network Representation of the Power FET With Input and Output Current Circuit

[1] Q^*_{rr} and t^*_{rr} are characteristic values for the freewheeling diode, where Q^*_{rr} is the reverse recovery charge and t^*_{rr} is the reverse recovery time.

The power FET is replaced by the equivalent electrical network drawn in **Figure 1**. The point capacitances (C_{GD}, C_{GS}, C_{DS}) assumed in this diagram replace the function of the capacitances in every FET cell, which have a differential effect. To complete the analytical specification of the network, including the power FET, the transient response of the FET must be specified. The control characteristic curve g_{fs} of the power FET is described by the following equation:

$$g_{fs} = \frac{\mu \varepsilon_{ox} W}{T_{ox} \times L} \times (v_{GS} - V_T) \qquad \textbf{equation 2}$$

(where μ_n = mobility of the electrons, W = channel width, L = channel length, ε_{ox} = dielectric constant of the oxide, T_{ox} = thickness of the oxide). This equation shows that the control characteristic for the power FET is a linearly increasing function of the applied voltage v_{GS}, and is displaced relative to the origin by the threshold voltage V_T. Using this control characteristic function, the switching region can be described mathematically as follows:

– Blocked region: $i_D = 0$

– Active region: $i_D = g_{fs} \times (v_{GS} - V_T)$

Gated (on) region: $i_D = v_{DS} / R_{DS}$

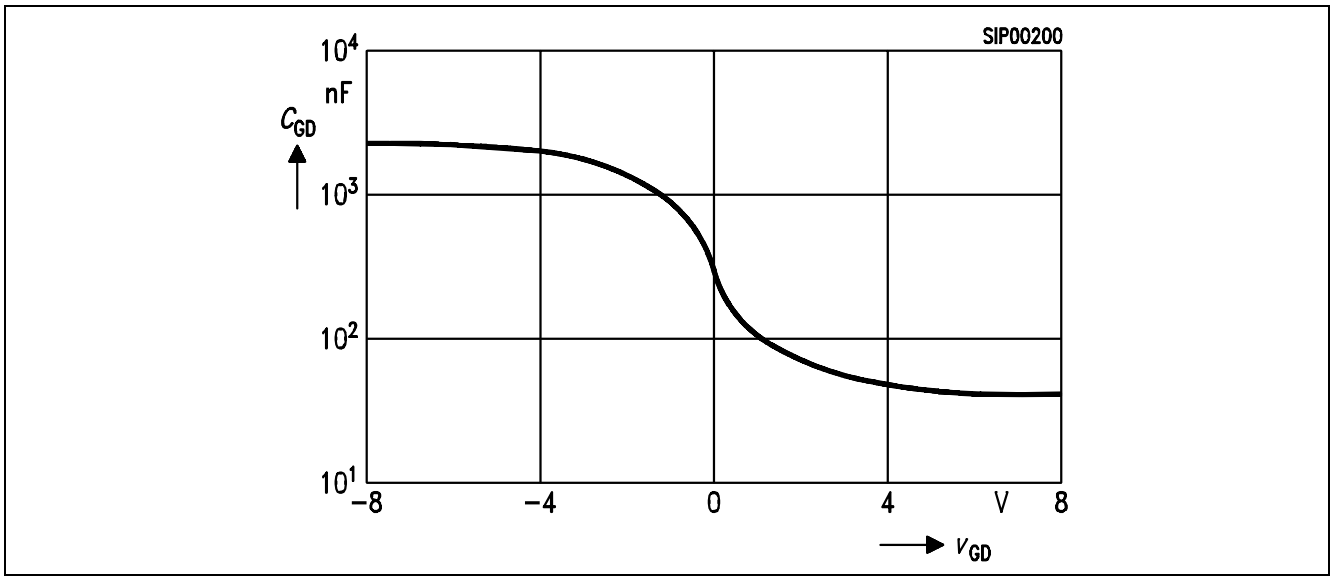

Figure 4
The Gate-Drain Capacitance as a Function of the Voltage v_{GD}

To specify the power FET, data sheet details are sufficient. However, account must be taken of the fact that the capacitances C_{GD} and C_{DS} are voltage-dependent. The feedback capacitance C_{GD} is a capacitance which depends on the amplification and on v_{GD}, and characterizes switching in the active region. The graph of this capacitance in the lower voltage region, $-8\ V \le v_{GD} \le +8\ V$ is shown in **Figure 4**.

The power FET is driven from a signal source generator which provides an input voltage v_i in the form

$$v_i = \begin{cases} 0\ \text{V for}\ t \le 0 \\ V_0\ \text{for}\ t > 0 \end{cases}$$

and has an internal resistance of R_S.

An analysis of the current and voltage waveforms during switching has shown that switch-on and switch-off each proceed through 4 stages. This subdivision of the switching process into 4 time intervals forms the basis for the analytical calculation. **Figure 5** shows an example of this subdivision of the switch-on and switch-off processes.

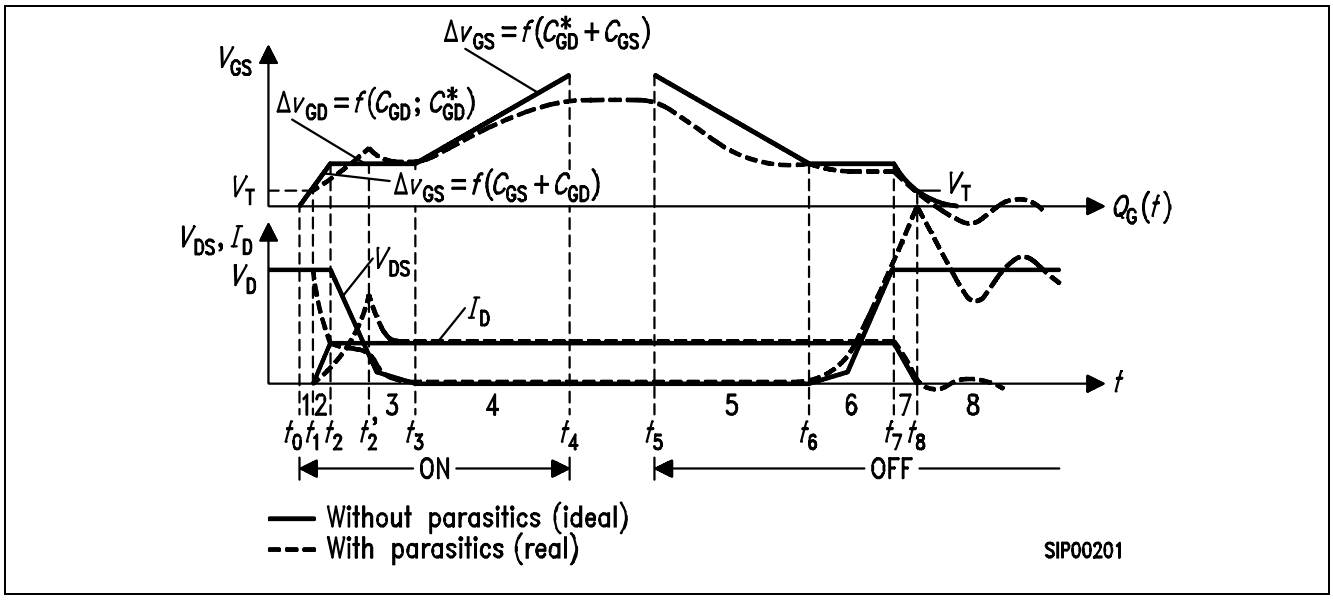

Figure 5
Current and Voltage Waveforms During Switch-on and Switch-off (Computed Result);
L_σ = 0.35 µH, L_S = 50 nH, R_S = 50 Ω

The calculation of the current and voltage waveforms for the input and output circuits is made on the assumption that it is possible to neglect certain factors in the network and in the semiconductor device. The detailed requirements which the input and output networks (excluding the power FET) must meet are as follows:

– L_σ is the total stray inductance of the output circuit.

– The effect of the inductance L_S is considered separately.

– The effect of the stray inductance in the gate circuit is ignored. This assumption is permissible provided that the driver circuit is connected via short conductive paths.

– The load inductance L_L is so large that the load current remains constant during the switching and commutative phases.

In producing a mathematical specification of the power FET, it is assumed that the following can be neglected:

– The internal gate resistance R_G is ignored. It follows from this that the signal applied to the gate connection initiates inversion of the channel with no delay.

– The drain current rises linearly with v_{GS}, as soon as $v_{GS} > V_T$.

– The stray inductances due to the chip bonding are included in L_σ or L_S, as appropriate.

In the following analytical treatment, the current and voltage waveforms in each time interval are described by differential equations (DEs). These DEs are, as far as possible, solved explicitly for the state variables ($v_{GS}(t)$, $v_{DS}(t)$ and $i_D(t)$), which are relevant in analyzing the switching process, and evaluated using a digital computer.

$$\begin{bmatrix} -R_S(C_{GD}+C_{GS})+L_S g_{fs}\left(1+\frac{C_{GS}}{C_{GD}}\right) & R_S C_{GD} & -L_S\frac{C_{GS}}{C_{GD}} & -L_S\left(1+\frac{C_{GS}}{C_{GD}}-\frac{C_{GS}}{C_{DS}}\right) \\ C_{GD} & C_{DS}-C_{GD} & 0 & 0 \\ L_S g_{fs}\left(1+\frac{C_{GS}}{C_{GD}}\right) & 0 & L_\sigma - L_S\frac{C_{GS}}{C_{GD}} & -L\left(1+\frac{C_{GS}}{C_{GD}}-\frac{C_{GS}}{C_{DS}}\right) \\ 0 & C_{DS} & 0 & 0 \end{bmatrix} \begin{bmatrix} \frac{d}{dt}v_{GS} \\ \frac{d}{dt}v_{DS} \\ \frac{d}{dt}i_{L\sigma} \\ \frac{d}{dt}i_{DS} \end{bmatrix}$$

$$= \begin{bmatrix} 1 & 0 & 0 & 0 \\ g_{fs} & 0 & -1 & 0 \\ 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{GS} \\ v_{DS} \\ i_{L\sigma} \\ i_{DS} \end{bmatrix} + \begin{bmatrix} -V_0 \\ -g_{fs}V_T \\ V_D \\ 0 \end{bmatrix}$$

equation 3

The starting point for the calculation is determined by the steady state with $i_D = 0$, $v_{DS} = V_D$ and $V_0 = 0$ V. In addition, it should be true that the voltage drop across the load is negligible. Subject to this convention, the network shown in **Figure 3** can be completely described by a 4×4 matrix. When solving the DEs, account must be taken of the fact that $C_{DS} = f(v_{DS})$ and $C_{GD} = f(v_{DS}, V_{GD})$ are non-linear capacitances.

We discuss first the switching behavior with the parasitic components $Q_{rr} \neq 0$, $L_\sigma \neq 0$ and $R_S \neq 0$. The effect of the stray inductance L_S will be considered separately. Under this assumption, the system of equations in (3) reduces to a 3×3 matrix. The first step in solving this system of DEs, is to calculate the value λ of the system matrix. In the case that the FET is switched off, the network is described by matrix (3) if g_{fs} is set = 0 and L_σ is replaced by $L_\sigma + L_L$. If the power FET is saturated it will be in the region of the characteristic curve which is ohmic, so that in this switching state the network must be described by the system of equations (4).

$$\begin{bmatrix} \frac{d}{dt}v_{GS} \\ \frac{d}{dt}v_{DS} \\ \frac{d}{dt}i_{L_\sigma} \end{bmatrix} = \frac{1}{A}\begin{bmatrix} (C_{DS}-C_{GD})L_\sigma & -\frac{R_S C_{GD} L_\sigma}{R_{DSon}} & -R_S C_{GD} L_\sigma \\ -C_{GD} L_\sigma & \frac{-R_S L_\sigma (C_{GD}+C_{GS})}{R_{DSon}} & -R_S L_\sigma (C_{GD}+C_{GS}) \\ 0 & R_S (C_{GD}+C_{GS}) \times (C_{DS}-C_{GD}) - C_{GD}^2 & 0 \end{bmatrix} \begin{bmatrix} v_{GS} \\ v_{DS} \\ i_{L_\sigma} \end{bmatrix}$$

$$+\frac{1}{A}\begin{bmatrix} -V_0 L_\sigma (C_{DS}-C_{GD}) \\ V_0 L_\sigma C_{GD} \\ -V_D R_S \left[(C_{GD}+C_{GS})(C_{DS}-C_{GD}) + C_{GD}^2 \right] \end{bmatrix}$$

equation 4

$$A = -R_S L_\sigma \left[(C_{GD}+C_{GS})(C_{DS}-C_{GD}) + C_{GD}^2 \right]$$

The explicit solutions for the state variables ($v_{GS}(t)$, $v_{DS}(t)$ and $i_D(t)$) of the switch-on and switch-off processes are in some cases very extensive, so they will be omitted here.

The summary below shows the simplifications which can reasonably and validly be made in each of the time intervals to avoid the computing effort being impracticably great, while at the same time giving sufficient accuracy in the description of the switching processes.

Time interval 1

$i_{L\sigma}$ = 0
$i_{GD} = i_{DS} << i_{GS}$
$v_{DS} = V_D (v_{LL} = 0)$

Time interval 2 + 3

$i_{GD} << i_{L\sigma}$
$i_{DS} << i_{L\sigma}$

Time interval 4

i_{GD} = 0
i_{DS} = 0
$v_{DS} = i_{DS} \times R_{DSon}$
$i_D = i_L$

Time interval 5

$v_{DS} = i_{DS} \times V_{DSon}$
$i_D = I_L$
i_{GD} = 0
i_{DS} = 0

Time interval 6 + 7

$i_{GD} << i_{L\sigma}$
$i_{DS} << i_{L\sigma}$

Time interval 8

i_D = 0

3.2 Parametric Representation of the Switching Process

The computational program calculates the switching process for a period, using the chosen parameters. One computational pass calculates the main values, such as di_D/dt, dv_{DS}/dt, $\hat{I}_D$, $\hat{V}_{DS}$, t_{on}, t_{off}, P_{dyn}, P_{stat} and $\hat{I}_{GS}$. Two examples will be used to compare the calculated current and voltage waveforms with the results obtained experimentally.

The special features of the computational program produced for this work can be summarized as follows:

– non-linear graph of the capacitances (C_{GD}, C_{DS})

– changeable switching speed ($v_0(t)$; R_S)

– takes into account the stray inductances L_S and L_σ

– realistic freewheeling diode (Q_{rr}, t_{rr})

– manufacturer's data suffices to describe the power FET

– actual transient behavior (including with drain-source connection)

– calculation of dynamic and static power loss

– parametric representation of the switching process

– calculates the magnitude of the required absolute maximum ratings for component dimensioning.

A meaningful parametric representation of the switching process is only provided if a single (network or component) parameter is varied at once.

Switching Behavior for Different Stray Inductances, L_σ

The effect of the stray inductance L_σ is particularly dangerous during switch-off, due to the overvoltage ($L_\sigma \times di_D/dt$). On the other hand, the switch-on process benefits in that, during time intervals 2 and 3, the voltage across the FET is reduced as a result of the positive current commutation from the freewheeling diode into the transistor (see **Figure 5**).

The amplitude of the drain-source voltage overshoot will increase, all other parameters being unchanged, as the stray inductance L_σ increases. After the maximum value has been reached, the power FET has left the active region, but the FET's output capacitor is charged up to the maximum value of the drain-source voltage, and discharges via the damped resonant circuit which comprises L_σ, FET capacitances and the output circuit conductor resistance. The influence of $C_{GD} = f(v_{GD})$ can clearly be seen in the rise of the drain-source voltage. As will be seen from **Figure 6**, this oscillation is transmitted to the input via the feedback capacitance C_{GD}. The waveform of the gate-source voltage $v_{GS}(t)$ in time interval 8 is made up of two functions (an exponential function and a damped trigonometric function). The amplitude of the resonant circuit's effect in the input signal can reach dangerously high levels if the stray inductance L_σ (for constant di_D/dt) is large and the input circuit is not of sufficiently low impedance.

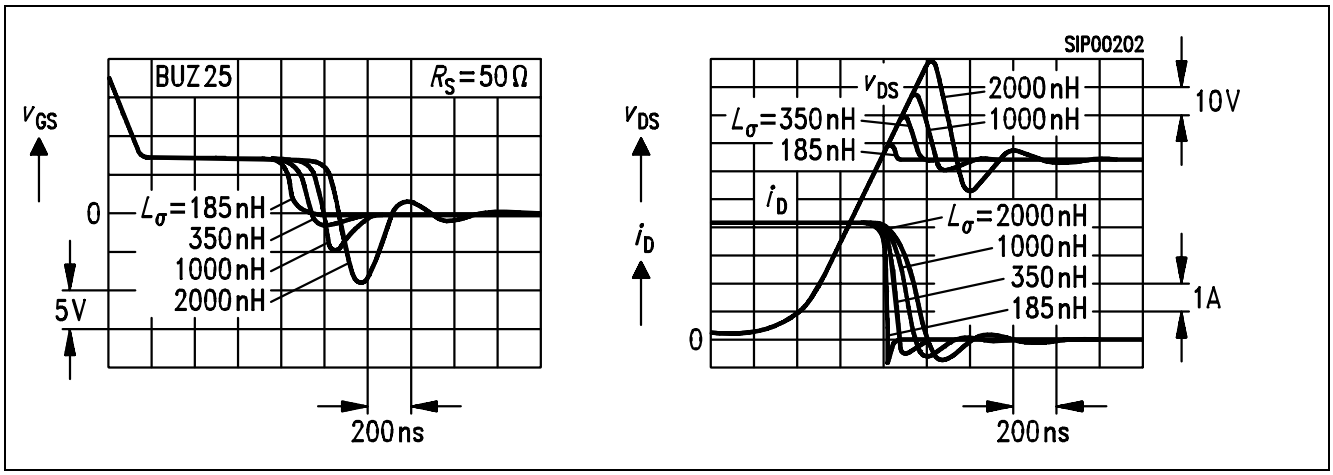

Figure 6
Waveform of the Gate-Source Voltage $v_{GS}(t)$ when the FET is Switched-off (Measured Results); V_D, I_L, V_0, R_S all Constant; BUZ 25

Variation in the Switching Time

The switching speed of the power FET can be very easily controlled, either by varying the resistance R_S while holding the signal source voltage V_0 constant or – as shown in **Figure 7** – with the resistance R_S held constant by varying the amplitude of V_0.

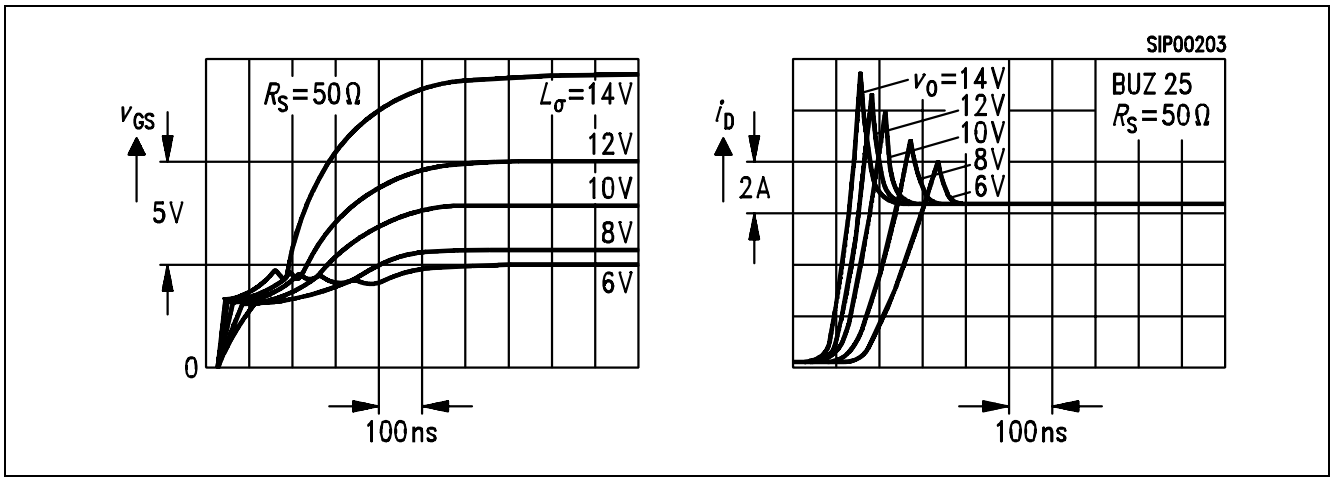

Figure 7
Waveforms of the Voltages $v_{GS}(t)$ and $v_{DS}(t)$ Across a Switching Cycle, as a Function of the Signal Source Voltage V_0 (measured results); V_D, I_L, R_S all Constant

As the input resistance R_S increases (for a constant signal source voltage V_0), the drive current drops, and hence the switching times lengthen. This is linked with an increasing reduction in the overvoltage amplitudes during switch-off. A critical disadvantage of longer switching times is the increasing switching power loss.

The figure shows the waveform of $v_{GS}(t)$ during switch-on, where V_0 is varied from 6 V - 14 V. The associated waveform of $i_D(t)$ shows very clearly that the peak reverse current for the diode decreases as the switching speed is reduced.

The control characteristic curve $i_D = gf_s\ (v_{GS} - V_T)$ defines how the amplitude of the diode return oscillation is transferred to the gate-source signal. After the threshold voltage has been reached, drain current begins to flow, and this induces in the stray inductance L_σ a voltage which depresses the drain potential, and forces a current through the C_{GD} capacitance. This leads to a weaker charging of the gate-source capacitance, and slows the switching process.

Switching Behavior with Variable Drain Current

As the load current increases, the FET channel must be increasingly driven higher (see also figure 8). A higher drain current requires a higher gate source voltage. At a constant resistance R_s, this means a higher gate current which in term permits a higher drain source voltage change. With the same stray inductance L_σ, the increasing gradient in the drain current waveform results in higher overvoltage amplitudes in the drain source voltage waveform.

Switching Behavior for Different Types of FET

Figure 9 shows the switch-off process for different types of FET, i.e. very different input capacitances. The FET with the lowest input capacitance (BUZ 72A) switches fastest.

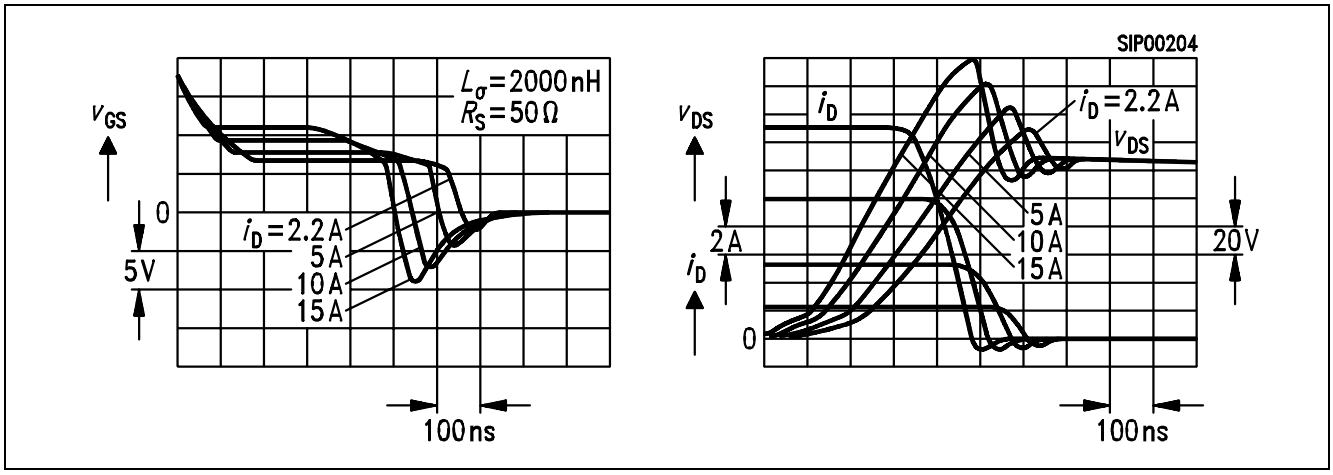

Figure 8
Current and Voltage Waveforms During Switch-off of a Power FET with I_D as the Parameter (computed results); V_D, V_0, L_σ, R_S all Constant

The FET's self-capacitances (C^*_{GD}, C_{DS}, C_{GS}), the stray inductances in the drain current circuit and the ohmic impedances are responsible for the transient behavior after the peak value $\hat{v}_{DS}$. The peak value of the drain-source voltage $\hat{v}_{DS}$ depends on the rate of load current commutation, di_D/dt, and on the values of L_σ and L_S. In particular, where there are high load current commutation rates, as achieved with the FET type BUZ 72A because of its low input capacitance (assuming constant driver current for all types of FET), small changes in L_σ and L_S have a considerable effect on the amplitude of the drain-source overvoltage. There is a difference between the values of the drain-source voltage amplitudes in **Figure 9a** and

Figure 9b. The reason for this is that the bond inductances have an effect at this point, and the structure-dependent stray inductances cannot be exactly determined.

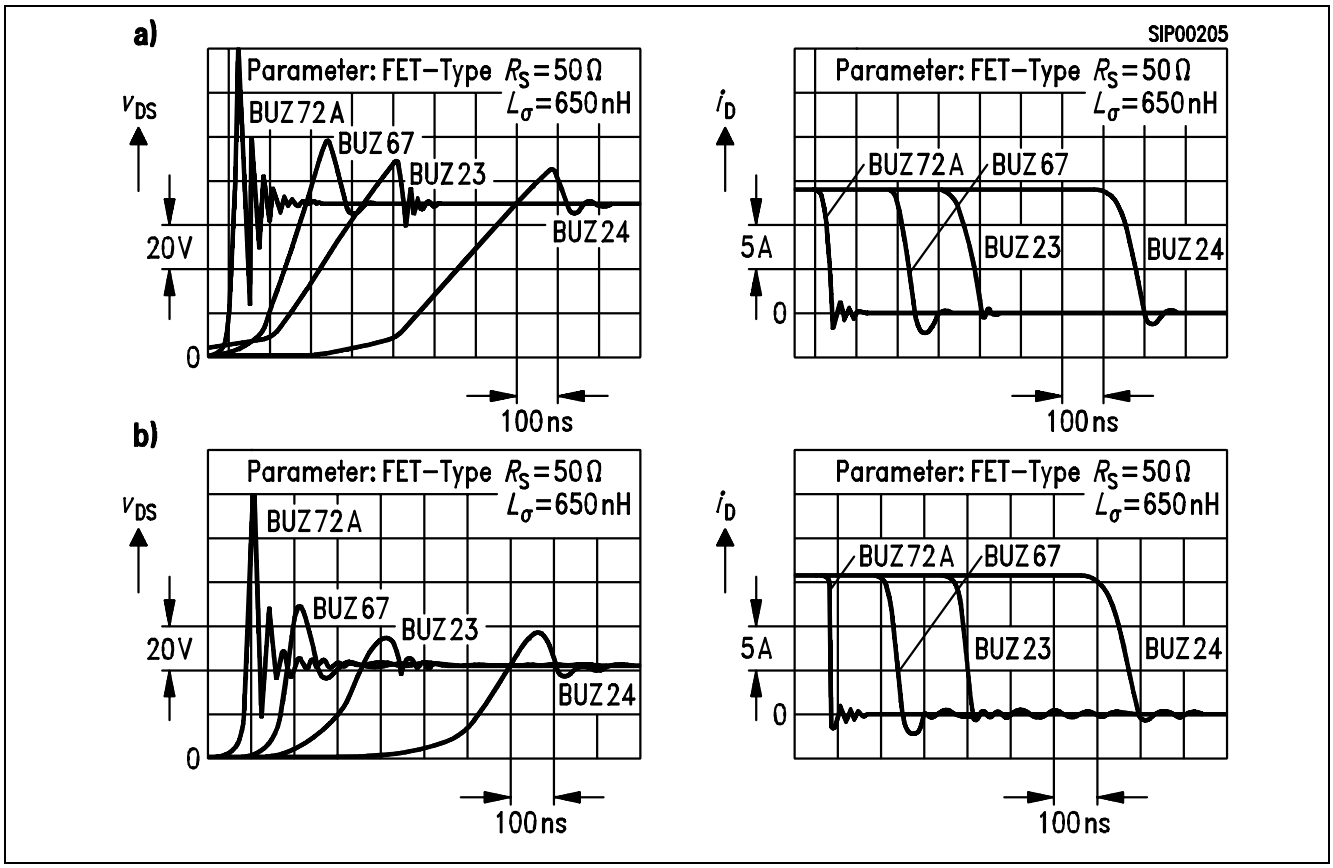

Figure 9
Current and Voltage Waveforms During Switch-off, for Different Types of FET; V_0, V_D, I_D, L_σ, R_S all Constant
a) Computed Results,
b) Oscillogram

Effect of the Stray Inductance L_s on Switching Behavior

So far, the stray inductance L_S (see **Figure 3**), which is common to the input and output circuits, has been ignored. This stray inductance consists of two main components.

One subcomponent L'_S due to the conductor leads from external source connections to the chip surface.

One subcomponent L''_S which is proportional to the length of the external source feed conductors. Any lengthening of this source connection is accompanied by substantial control disadvantages.

The measured effect of the stray inductance L_S on the switching behavior is shown in **Figure 10a**. **Figure 10b** shows the computed waveforms. The figures show that the stray inductance L_S delays the drop in the drain-source voltage, which leads to a significant increase in the dynamic power loss. This effect can be reduced by separating the driver and

output circuits back at the source connection. Two effects are responsible for the switching process proceeding as shown in **Figure 10** for a switch-on.

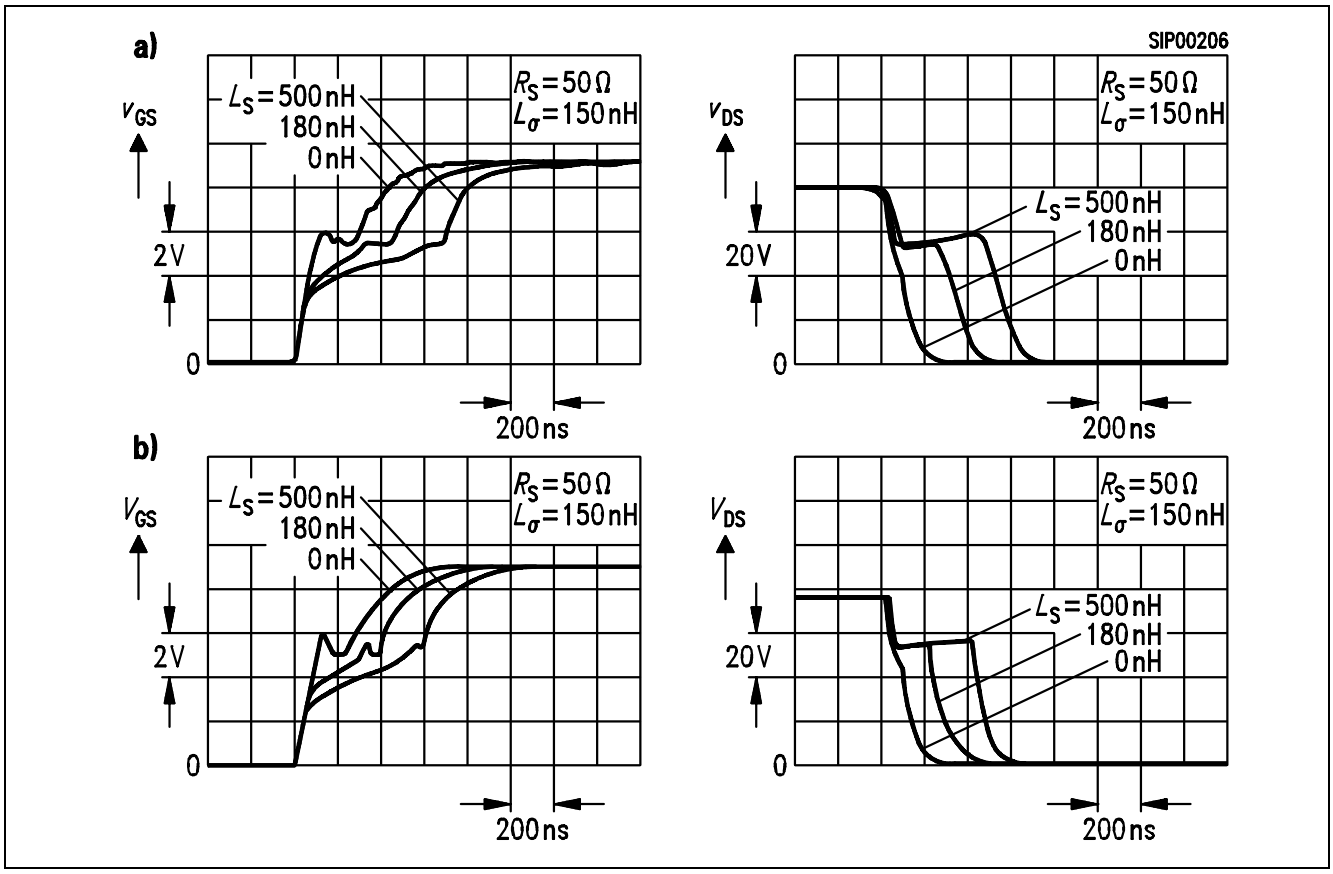

Figure 10
Current and Voltage Waveforms During Switch-on, with L_S as Parameter; V, V_D, I_D, L_σ, R_S all Constant
a) Oscillogram,
b) Computed Results

The voltage induced in L_S, namely

$$v_{LS} = L_S \times \left[\frac{d}{dt} i_D + \frac{d}{dt} i_S \right] \qquad \textbf{equation 5}$$

opposes the applied gate-source voltage v_{GS}, and thus inhibits the “enrichment” of the current channel.

As soon as the threshold voltage V_T is exceeded, the FET load current begins to take over, causing a voltage drop across L_σ and hence changing the drain-source voltage. The effect of the stray inductance L_S on the switching behavior must be considered in conjunction with L_σ, because there is no network with $L_\sigma = 0$.

The difference in the $v_{GS}(t)$ and $v_{DS}(t)$ waveforms compared with good circuit layouts, i.e. $L_S \approx 0$, is considerable. A comparison of **Figure 10a** and **Figure 10b** shows the good agreement between the computed results and those obtained experimentally.

4 Conclusions for the Use of Power FETs as “Fast Switches”

The investigations have shown that a power FET is subject to additional loads, due to the freewheeling diode’s recovery current during switch-on and to the stray inductance L_S during switch-off. Since the amplitude of the freewheeling diode’s reverse current rises exponentially with increasing switching time (assuming constant load current) it is particularly important to select a suitable freewheeling diode (small Q_{rr}). This leads to a problem, particularly for high reverse voltages, because the reverse recovery charge increases with the voltage across the diode. One good option available in this case is a power FET itself which, because of its semiconductor structure (see **Figure 1**) can also be used as a diode. By simultaneously switching the FET channel to conducting, it is possible to reduce considerably the storage charge of the n^--p^+ junction, so that a FET is also well suited as a freewheeling diode for fast current commutation processes. However, when used as a freewheeling diode it must be noted that the n^+-p^+-n^- zone sequence (see **Figure 1**) of the structure-dependent parasitic bipolar transistor, which lies parallel to the FET channel, means that simultaneous excessively high values of dv_D/dt with di_D/dt can cause the FET to switch over to conducting, resulting in it being damaged.

Because of the capacitive feedback to the input circuit via the C_{GD} capacitance, there is an increased danger for rapid switching operations that the FET is switched on again unintentionally. For this reason, for large drain-source voltage changes the impedance of the driver circuit must be low enough to protect the FET input.

The stray inductance L_S delays the drop in the drain-source voltage, which leads to a significant increase in the dynamic power loss. This can be largely avoided by separating the driver and output circuits back at the source connection, so that there is no additional common inductance in the input and output circuits.

The effect of the stray inductance L_σ, on the other hand, is that as the switching times become shorter, firstly the amplitude of the overvoltage which drives the transistor into a voltage breakdown rises, and secondly that the switch-off dynamic power loss is increased.

It is always the case that, all other switching circuit parameters being constant, the dynamic power loss increases as the switching time becomes shorter.