Switching Inductive Loads

When an inductive load is switched off rapidly switch-off overvoltages arise, which drive the power switch into avalanche breakdown. For this situation it should be noted that the semiconductor may only be operated in breakdown mode under the conditions specified in the data book. When this happens, the avalanche energy, permissible power loss and the defined current amplitude must not be exceeded. The values of the avalanche energy which the semiconductor can absorb in such operating situations depend on the area of the semiconductor which is driven into avalanche. However, if the voltage limitation is effected not in the semiconductor but instead in an “active Zener clamp”, it can absorb significantly higher energy values (**Figure 1b)**. When this happens, the power MOSFET switches on in a controlled way when the Zener voltage is exceeded, and converts the energy stored in the inductance into the switching mode. Provided that the pulse frequency of the switch is not too high, the maximum switch-off energy is determined by the silicon area, and not by the form of the package. This situation can be regarded as thermally pulsed operation.

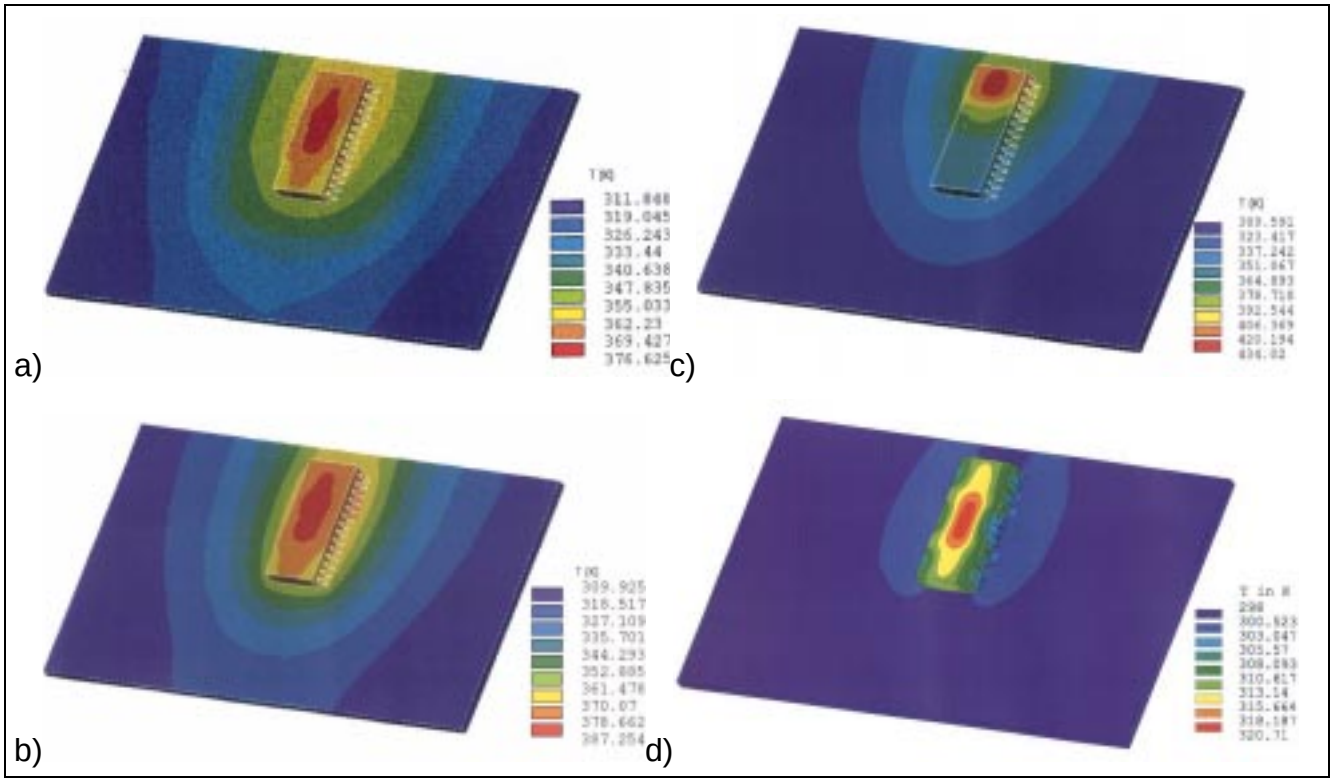

Figure 1
Temperature Profile of the Mounted P-DSO Package
Figures a) and d) refer to a 6 cm² Cu Surface on one Side, while Figures b) and c) are for a 2.2 cm² Cu Surface on two Sides of the P.C.B.

At a maximum power loss of 0.8 W, a power MOSFET with R_{DSon} = 0.2 Ω (warm value) will operate in a steady state. Assume the ambient temperature is 75 °C, the maximum permissible junction temperature 150 °C. When the pulse current is 8 A, the transistor is in avalanche mode for 400 µs.

This gives a maximum junction temperature of (multichannel transistor in the P-DSO package (mounted as in **Figure 1a**):

R_{thJA} (6 cm^2 copper area) = 35 K/W

ΔT = 0.8 W × 35 K/W = 28 °C

Avalanche mode:

P_{tot} = 8^2 × 0.2 = 12.8 W

Δt = 400 µs

R_{th} = 1 K/W

ΔT_{ges} = 28 °C + 12.8 × 1 ≅ 41 °C

T_{jmax} = 116 °C

Because of the short avalanche time of 400 µs, the spreading of the heat pulse is mainly dependent on the dimensions of the chip and on the thermal properties of the silicon. The transient heat resistance can therefore only be affected through the chip size, since neither the island size not the number of pin-island connections nor the size of the cooling surfaces have any significant effect on the transient heat resistance for brief pulses.