SIEMENS

The Ruggedness of Paralleled Power MOSFETs

Abstract

The behavior of power MOSFETs under avalanche conditions has been described in a number of papers. However, only single devices were examined. This paper investigates the avalanche action of power MOSFETs connected in parallel. A disadvantage of this configuration is that its overall ruggedness is at worst case no greater than that of each individual component. The user has to consider certain boundary conditions when connecting avalanche-resistant components in parallel. For example, it must be ensured that current sharing in the avalanche phase is as symmetrical as possible. This paper also takes a look at the thermal settling effects that occur during the avalanche process.

Keywords

Paralleled power MOSFETs, avalanche

Introduction

The demand for high-performance power switches is increasing at a constant rate. The fact that MOSFETs, unlike bipolar transistors, are easy to parallel enhances this development.

The main advantages of paralleled MOS transistors include:

– reduced $R_{DS(ON)}$

– higher load current I_D

– lower (transient) thermal resistance

– lower circuit inductance

– lower cost due to a higher yield

Special care has to be taken to ensure symmetrical current sharing in both the static phase and the dynamic phase. In the static phase, $R_{DS(ON)}$, forward transconductance g_{fs} and thermal coupling between the transistors must be matched as closely as possible. The transistor capacitances, the forward transconductance, the threshold voltage and parasitic elements play a significant role in the dynamic phase. The criteria which are important for parallel connections have been described in several papers.

Generally, poor dynamic current sharing indicates only that different junction temperatures are effective in the transistors but due to the generally high overload capability of MOSFETs, they are normally not at risk. In a worst-case scenario, however, critical operating states may occur, particularly when n transistors are connected in parallel and one transistor has to carry n-times current during turn-on or turn-off and hence moves out of the SOA. The behavior of power MOSFETs connected in parallel during the avalanche transient has not yet been described, however. It is a difficult topic since data sheets only include information about avalanche behavior at nominal current. During turn-off, however, very unsymmetrical current

sharing occurs in the case of paralleled MOSFETs with even slightly different breakdown voltages. The purpose of this paper is to establish rules to be observed in order to avoid endangering the reliability and ruggedness of the entire circuit during the avalanche transient even in the case of MOSFETs connected in parallel. The rules elaborated below are based on empirical investigations.

Breakdown Behavior

In the case of a short-circuited gate-source region, the maximum breakdown voltage in the case of a power MOSFET is determined by the avalanche breakdown of the P-base and the N-drift layer. The breakdown voltage is reached when the carrier avalanche multiplication factor $M = \infty$. With increasing junction temperature, M decreases and hence the breakdown voltage increases. It is assumed in this case that the breakdown of the edge structure only occurs at higher voltage. In addition, when considering the breakdown behavior of power MOSFETs, the existence of the parasitic bipolar structure (p.b.s.) must also be taken into account (**Figure 1**). This n^+-p-n^- transistor which is always present in the vertical n-channel MOSFET can substantially reduce the theoretically possible breakdown voltage in an adverse case. This always applies when the p.b.s turns on, i.e. the voltage drop at R_B is > 0.6 V. In the practical use of power MOSFETs, the following events may initiate activation of the p.b s:

- commutation transient,
- avalanche,
- static and dynamic d*v*/d*t* stress.

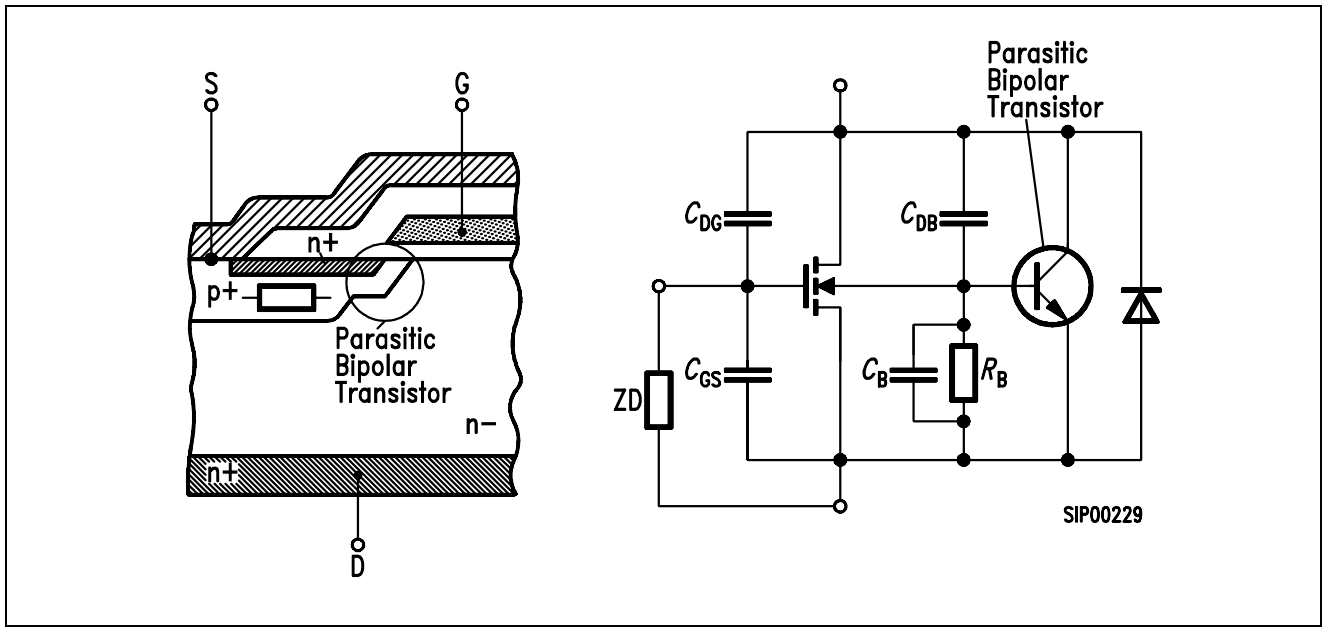

Figure 1
SIPMOS Transistor Cell
a) Semiconductor Structure
b) Electrical Equivalent Circuit

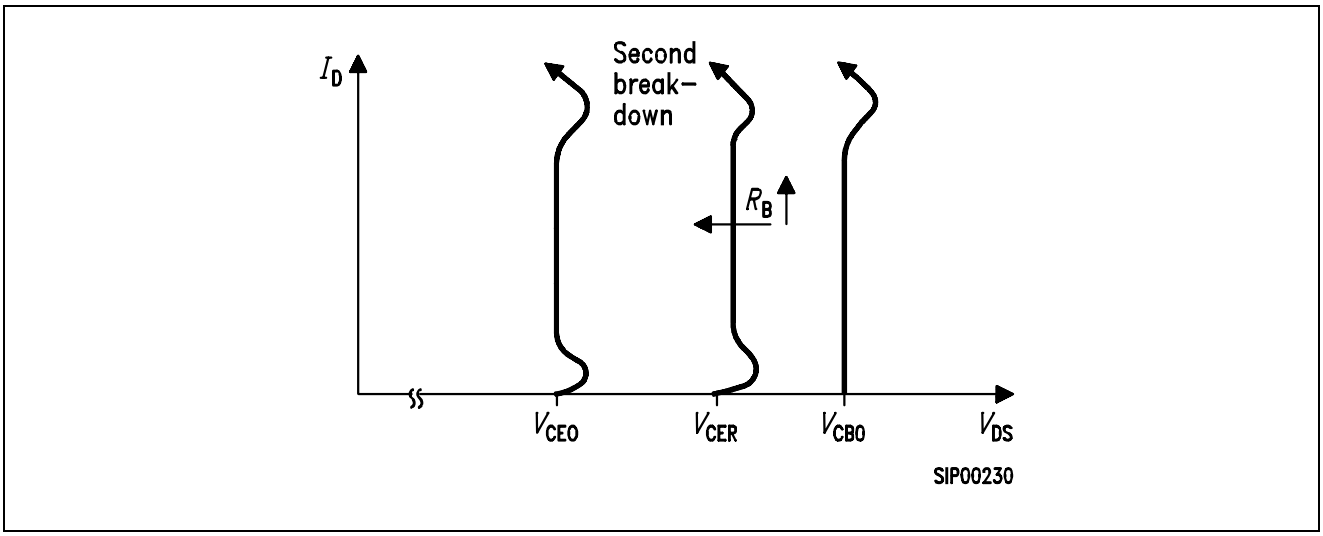

Figure 2
Breakdown Behavior of a Vertical MOSFET (inclusive p.b.s.)

Figure 2 shows the breakdown behavior of power MOSFETs taking account of the p.b.s. When the n^+ emitter of the p.b.s is inactive, the breakdown voltage of the MOSFET is V_{CBO} and attains its maximum value. However, if for one of the above reasons the emitter base barrier layer displays a voltage drop > 0.6 V, the emitter injects electrons into the base. In this way the p.b.s determines the breakdown behavior of the p-base and the n^--drift layer and the breakdown voltage of the MOSFET is reduced to the value V_{CEO}, meaning that it is approximately halved. If a resistor R_B is located between the base and the emitter, the breakdown voltage V_{CER} lies between V_{CB} and V_{CEO}. The greater the value of R_B, the more closely V_{CER} approaches V_{CEO}. If the voltage applied to the MOSFET is greater than V_{CEO}, the component is destroyed by the second breakdown. **Figure 3** shows the turn-on of the parasitic bipolar transistor.

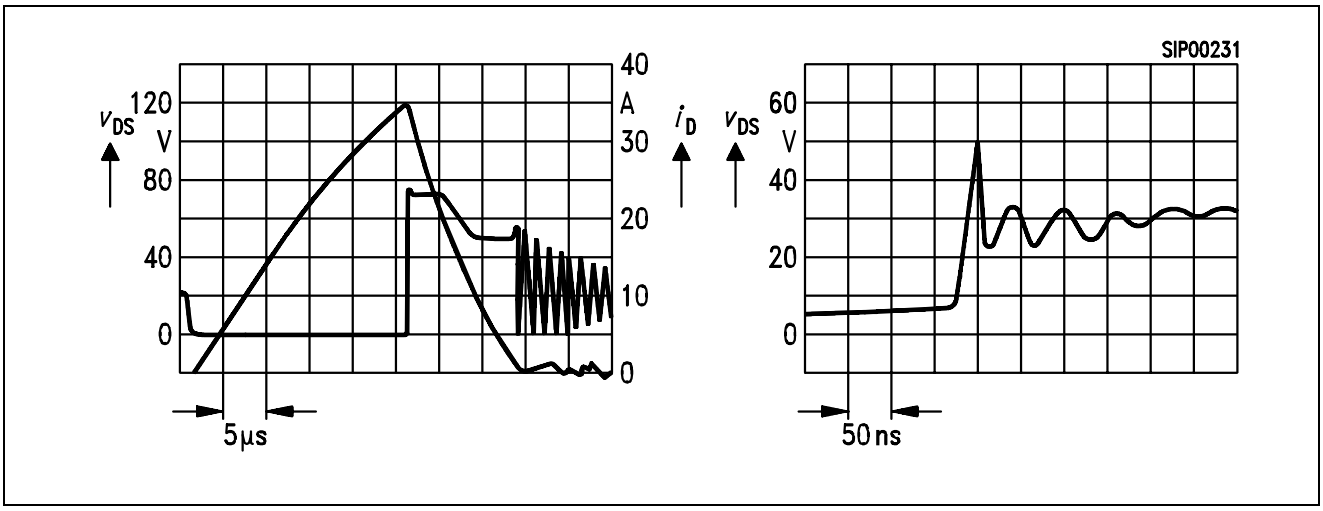

Figure 3
Turn-on of the Parasitic Bipolar Transistor of a MOSFET
a) $V_{DD} < V_{CEO}$
b) $V_{DD} > V_{CEO}$

In order to consider the breakdown behavior of power MOSFETs connected in parallel, it is necessary to know the slope of the I_D-V_{CBO} characteristic. It is the aim of this paper to investigate only the avalanche behavior of parasitic bipolar transistors in the off state. Two basic circuit configurations are suitable for the purposes of investigating the breakdown behavior of MOSFETs. **Figure 4a** shows the “classical” test circuit where the device under test is connected in series with an unclamped inductor. When the test device (DUT) turns off, an overvoltage builds up due to the inductance at the device which forces the MOSFET into breakdown when it exceeds $V_{BR(DSS)}$.

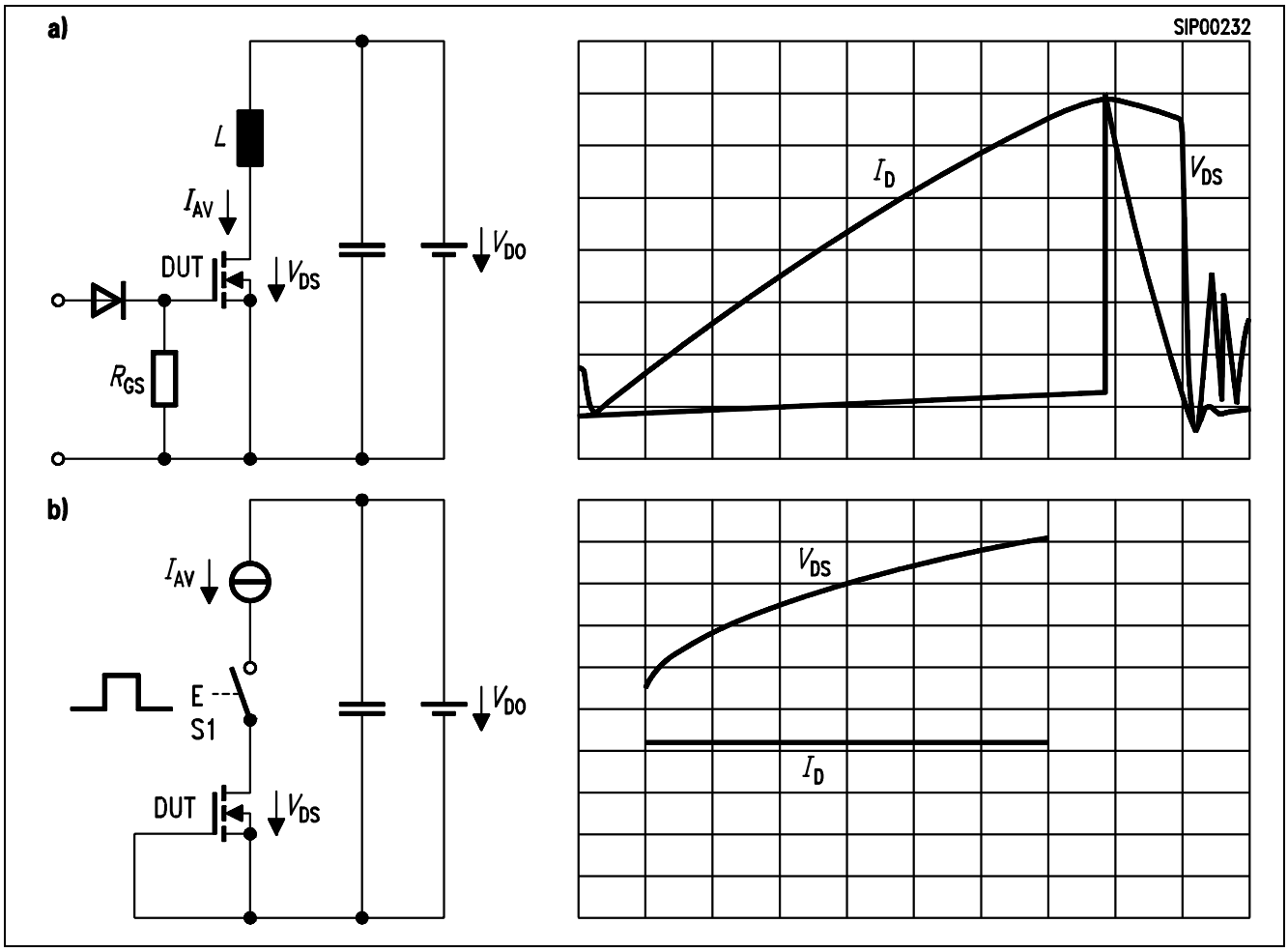

Figure 4
Principle Avalanche Test Configuration
a) Classical Test Circuit with an Inductive Load
b) Test Circuit with a Current Source

The circuit shown in **Figure 4b** applies a constant current to the MOSFET in the off state thereby causing breakdown. The advantage of this method is that the DUT can be subjected very easily to differing avalanche energies without exchanging inductors and the current remains constant. A current source is needed with a dielectric strength approximately 10% greater than $V_{BR(DSS)}$ of the device under test. The rise of I_D versus V_{DS} can be largely assumed to be linear in the relevant section. This does not apply in the mA range, which is not critical for the avalanche case, because the drain current then lies largely below its nominal current I_{DN}. This no longer applies to higher currents or current densities j if the number of charge carriers generated lies within the order of magnitude of the base doping N_D.

$j = e \times N_D \times v_{sat}$ **equation 1**

v_{sat} is the maximum drift velocity of electrons (10^7 cms^{-1}). Due to these additional mobile charge carriers, the gradient of the electrical field E (x) is substantially lessened.

$dE/dx = e/\varepsilon \times (N_D - n + p)$ **equation 2**

ε is the dielectric permittivity of silicon. This means that the component now absorbs more voltage. As current density continues to increase, the MOSFET enters an unstable region with negative I_D-V_{DS} characteristic load, which finally results in second breakdown (**Figure 2**).

Since the base doping of 50 V components is around 5×10^{15} cm^{-3} and that of 1000 V components around 2×10^{14} cm^{-3}, very different critical current strengths result in this case. Since, moreover, breakdown is not homogeneous in the avalanche condition (**Figure 5**), the result is differing area utilization of the active transistor as a function of voltage class, i.e. the relevant cell geometry.

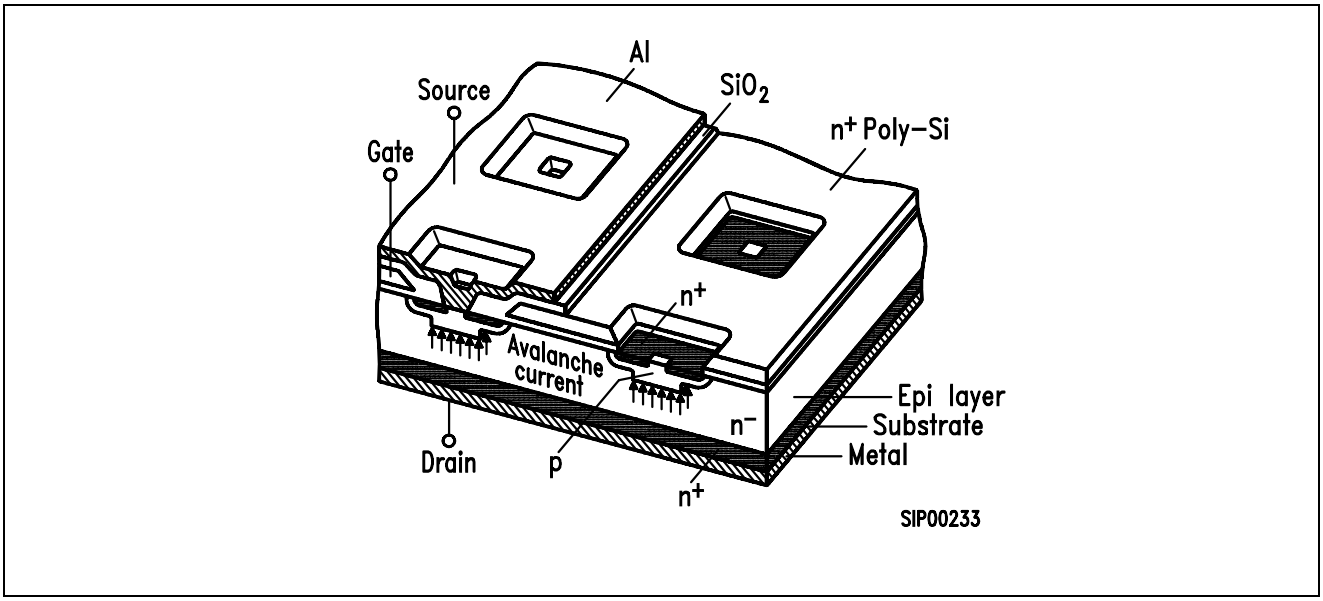

Figure 5
Avalanche Breakdown of a MOSFET

This means that for 50 V components the critical current density lies around 8 times the nominal current and for 1000 V components around 1.8 times the nominal current. When determining the slope of the characteristic, it must be borne in mind that there is no overlapping of thermal effects in this case, as this would give too low a slope. Since it is interesting for the user to know whether n transistors connected in parallel can absorb n times the avalanche energy of the single component, it is now necessary to investigate the current amplitudes up to which the individual component can absorb the avalanche energy E_{AS}. These measurements were carried out for various components of one manufacturer and also for different production codes, and the results were very similar. **Figure 6** shows the failure probability P of MOSFETs at constant energy and increasing current. It can be seen that there is no impairment of the reliability and ruggedness of the transistor up to a level of 2 times nominal current. This means that during the dynamic phase individual transistors can carry twice the nominal current during avalanche with no need to reduce the permissible avalanche energy.

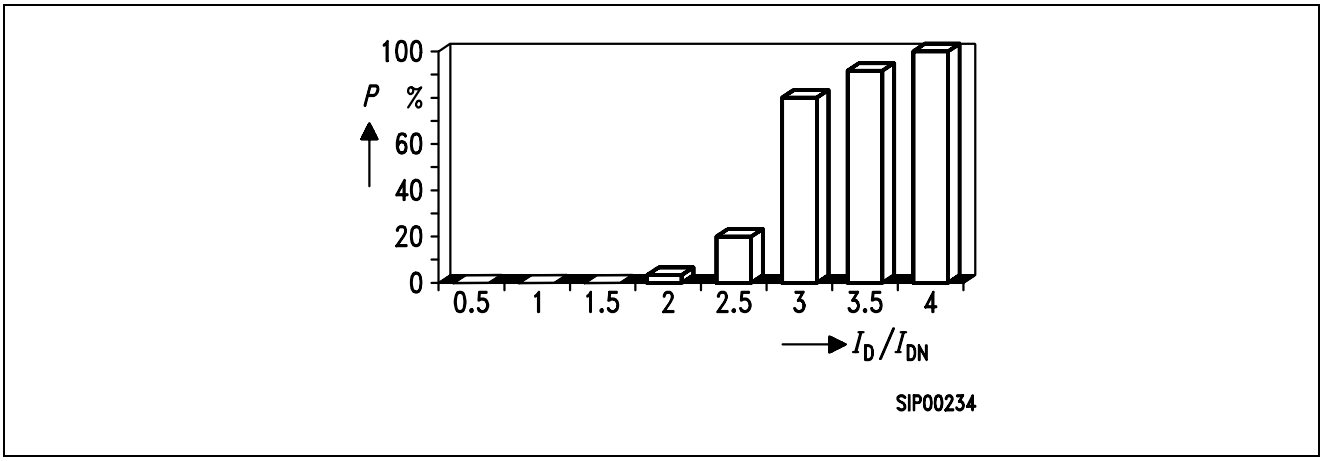

Figure 6
Failure Probability of Constant Avalanche Energy Level Versus Current Amplitude

Quartering the avalanche energy E_{AS} produced only slight changes in the failure probability of the components, i.e. for the same energy, a high current amplitude is far more critical than a high inductance.

Breakdown of Paralleled Devices

Figure 7 and **8** show the problem of MOSFETs connected in parallel with different breakdown voltages.

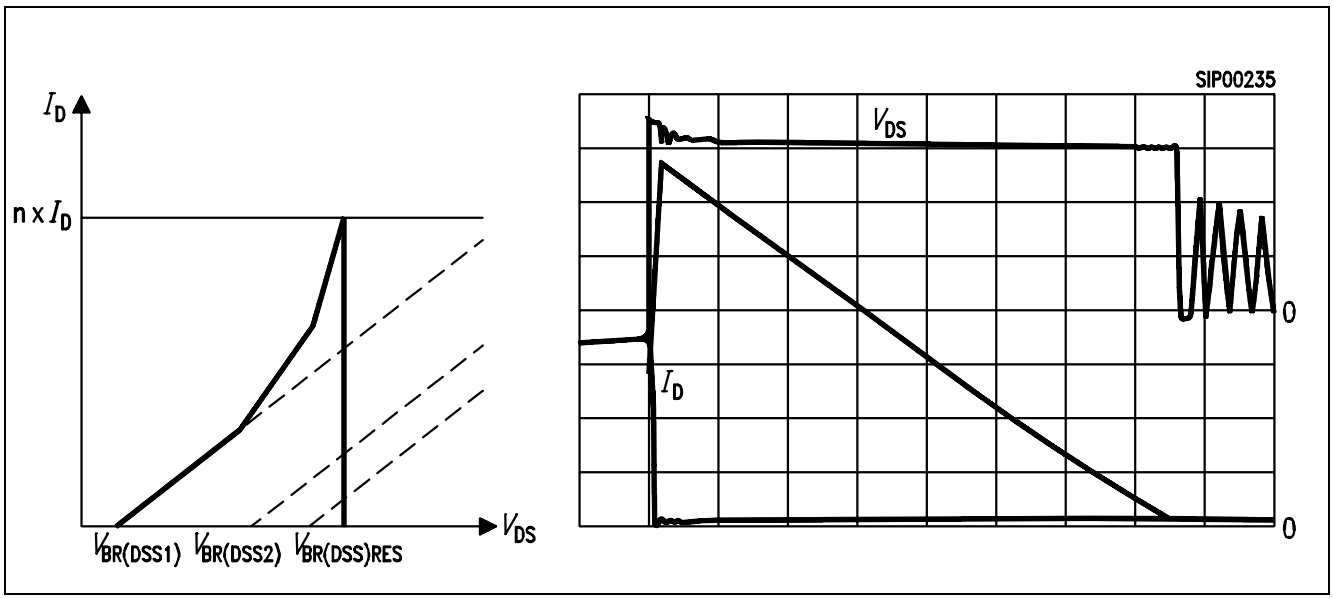

Figure 7
Principle Current Sharing of three Devices During Avalanche

Figure 8
Current Sharing of Two Devices During Avalanche I_D = 10 A/Div., V_{DS} = 20 V/Div., t = 5 µs/Div

The current sharing is a function of the different breakdown voltage $V_{BR(DSSn)}$ and the rise m of the current increase. On the one hand, the breakdown behavior of the individual components is shown here and the complete current $\sum I$.

$I_i = m \times (V_{BR(DSS)Res} - V_{BR(DSSi)})$ **equation 3**

i = 1 ... n

$\sum I_i = m \times \sum (V_{BR(DSS)Res} - V_{BR(DSSi)})$ **equation 4**

i = 1 ... n

Equation 3 describes the current components in the breakdown and equation 4 the complete current. $V_{BR(DSS)Res}$ is the voltage of the parallel circuit at which the required current occurs. This voltage is also directly measurable at the terminals. In order to establish what distribution of breakdown voltages is particularly critical, it is necessary to distinguish between individual cases (**Figure 9**).

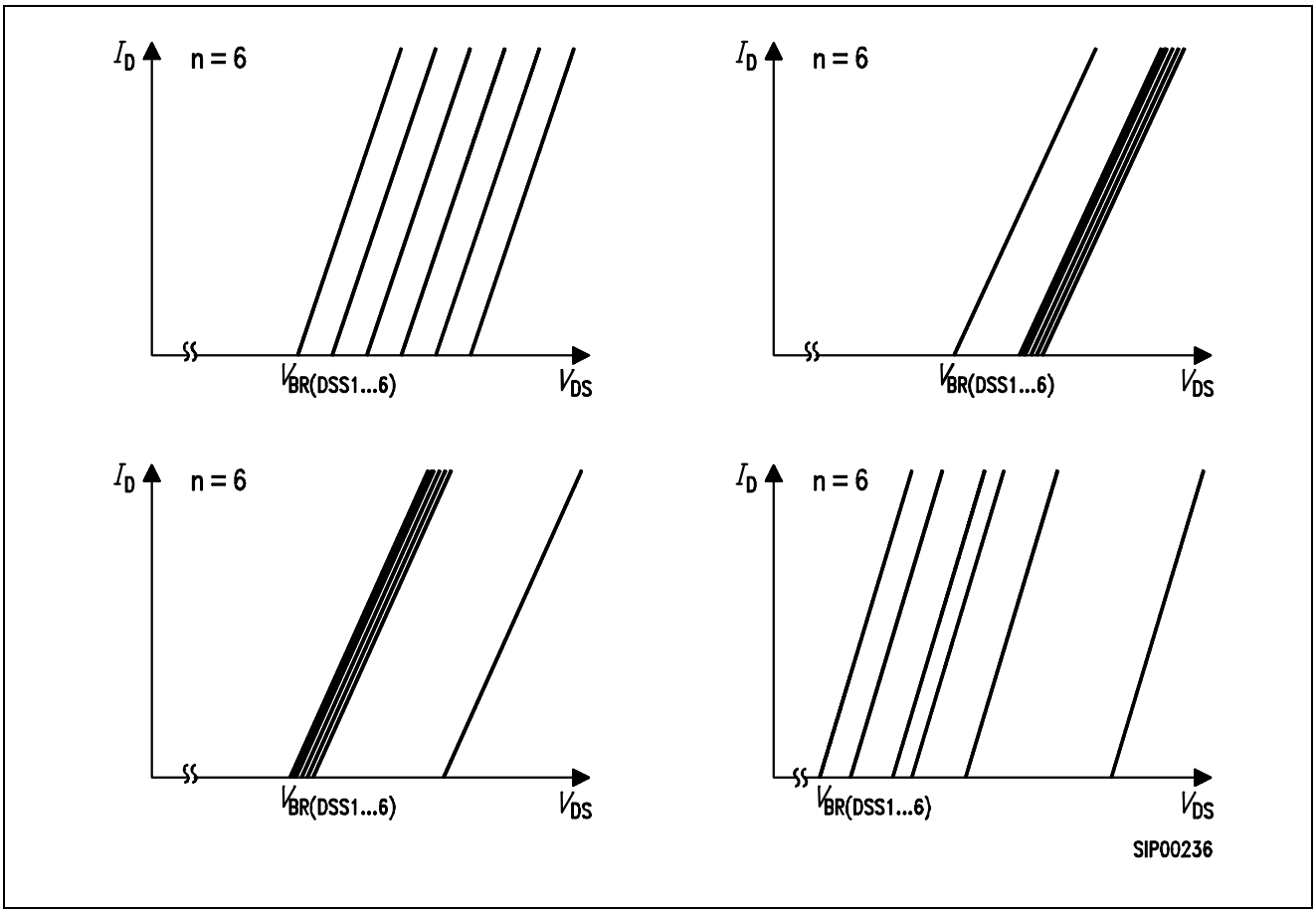

Figure 9
Different Critical Breakdown Voltage Distributions

- case 1, top left: the individual breakdown voltages are equidistant
- case 2, top right: 1 transistor has a small breakdown voltage and the rest undergo breakdown at virtually the same voltage
- case 3, bottom left: (n-1) transistors have a small but identical breakdown voltage and 1 transistor a higher breakdown voltage
- case 4, bottom right: the individual breakdown voltages have completely different values

In order to be on the safe side in each case, the following example uses 1.5 times the nominal current as the maximum permissible load for the individual transistor. The transistor with the lowest breakdown voltage is generally the one under the heaviest load. In addition, the following example uses a complete current n $\times$ I_{DN} applied to n transistors connected in parallel.

Example: Case 1

V_{DS} = 50 V I_D = 33 A n = 6 m = 6 A

$$I_1 = m \times \underbrace{(V_{BR(DSS)Res} - V_{BR(DSS1)})}_{\Delta V_{Res}}$$

$$I_2 = m \times (V_{BR(DSS)Res} - V_{BR(DSS2)})$$

.
.
.

$$V_{BR(DSSi+1)} = V_{BR(DSSi)} + \Delta V$$

$$I_{1max} = 1.5 \times I_D$$

$$I_2 + I_3 + I_4 + I_5 + I_6 = 4.5 \times I_D$$

$$\Delta V_{Res} = I_1/m = (1.5 \times I_D)/m = 8.25\ V$$

$$\Delta V = (5 \times m \times \Delta V_{Res} - 4.5 \times I_D)/15\ m = 1.1\ V$$

The difference in the breakdown voltages of the 6 paralleled transistors must be 1.1 V. The other cases will be solved in the same way.

Case 2 means that in total the breakdown voltages of the six devices must be much closer together than in case 1.

Case 3 is not critical and the transistor with the highest breakdown voltage very often conducts no avalanche

Case 4 The stress of the different devices depends very strongly on the differences in the breakdown voltages. There is no general statement possible.

Temperature Effects

As mentioned above, the breakdown voltage of MOSFETs increases with increasing temperature (**Figure 10**).

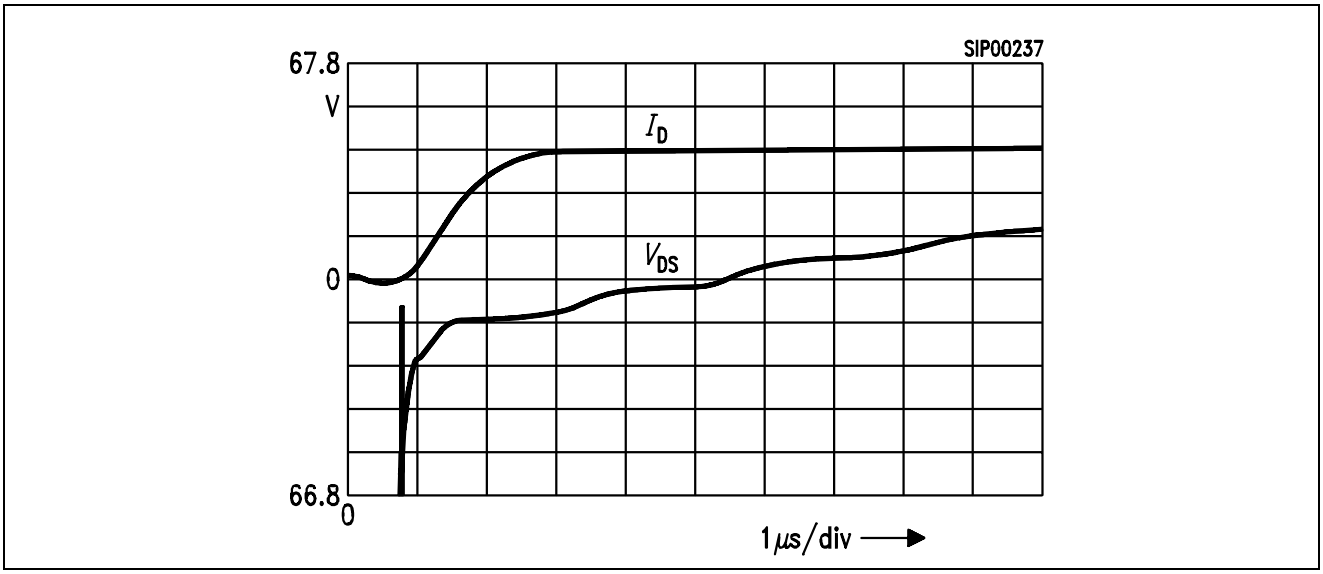

Figure 10
Increase of the Breakdown Voltage During Avalanche as a Result of the Temperature Rise

In the parallel circuit unfortunately, this effect cannot normally be utilized. The reason for this is that it is not permissible for a transistor to exceed its maximum permissible current even for a few ns during the avalanche transient. The rise in the junction temperature is therefore too slow to prevent avalanche failures in the dynamic phase in this case. If the dynamic phase lasts longer than a few hundred ns, equalization transients occur but they do nothing to mitigate the critical initial instant.

Summary

It was shown that by observing certain rules, n power MOSFETs connected in parallel also possess n times the avalanche capability of the individual components. The user need only determine the slope of the current rise in the breakdown phase and establish the distribution of breakdown voltages in order to relate his case to one of the above examples.