SIEMENS

Serial Connection of Power MOSFETs

As for MOS modules, there are two main reasons for the serial connection of power MOSFETs:

- To reduce the ON-resistance for a given voltage range. Since the ON-resistance for high-voltage MOSFETs is largely determined by the epi area, this increases at a higher than linear rate ($R_{DS} \approx V_{BR}^{2.5 .. 2.7}$).
  The R_{DSon}-resistance of two 500-V transistors connected in series is significantly lower than that of a 1000-V transistor.
- To increase the switchable voltage above V > 1000 V. The block schematic diagram in **Figure 1** shows the circuit concerned. This circuit can be used as a drive circuit for any of the MOS modules connected in series. Note that each MOS-FET is configured with an RCD network in the case of serial connection. Such a configuration is not normally required for SIPMOS transistors, since only very low inherent losses occur when disconnecting in this case. This measure is primarily intended to suppress voltage overshoots when disconnecting. RCD circuits are used with the high-voltage switch described, in order to ensure an equal voltage distribution to each stage. With optimum distribution of the static voltage, all transistors have the same output capacitance C_{OSS}. This can only be achieved if all the components correspond to each other. Even if the output capacitances and the predetermined voltage correspond, it is very probable that the transistors connected in series will not have the same switching time. An RCD connection is therefore required for each transistor to ensure dynamic voltage distribution. The protective capacitor should have a very low capacitance in order to limit the charge transfer losses to the protective circuit, which are calculated as follows:

  $$P_{max} = \frac{1}{2} C_S \times V^2 \times f$$

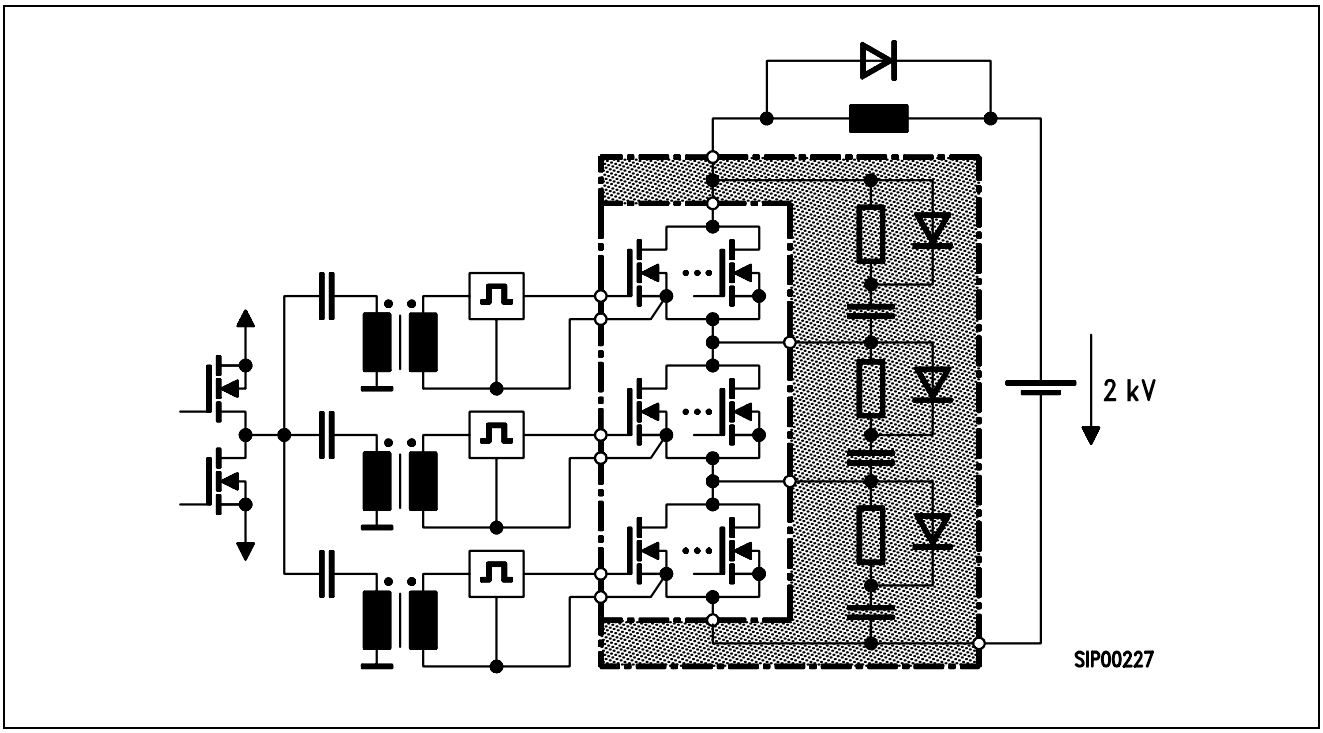

Figure 1
Simplified Electrical Circuit Diagram for the Sequential Connection of FET Modules with the Drive Circuit and Connections Required

The maximum voltage to each protective capacitor C_S cannot be greater than the maximum reverse voltage for each transistor. Careful circuit layout must consider the longest cutoff time and the biggest difference between the delay times of the individual stages. The capacitor in the protective element of the first stage to disconnect is charged with the full load current until the last stage is also disconnected. This can generate a clear “auxiliary” voltage in a stage. The protective capacitor must therefore be dimensioned to ensure that the peak voltage is kept below the breakdown voltage of the individual transistors. The voltage at the transistor during disconnection is:

$$V_e = \frac{I_m \times \Delta t_f}{2C_S}$$

whilst the additional voltage caused by the permanent charge at the t_{doff} phase is:

$$V = \frac{I_m \times \Delta t_{doff}}{C_S}$$

The total voltage is the sum of the two voltages defined above, and the minimum capacitance can therefore be calculated as follows:

$$C_{S\,min} = \frac{I_m \times t_{fmax} + 2I_m \times t_{d(off)max}}{2V_{(BR)DSS}}$$

If there is no difference in the cutoff delays between the stages, then the minimum capacitance is as follows:

$$C_{\text{S min}} = \frac{I_{\text{m}} \times t_{\text{fmax}}}{2V_{\text{(BR)DSS}}}$$

This value also ensures equal voltage distribution, because $C_{\text{S min}}$ is three to four times greater than the output capacitance C_{OSS}, and the capacitance differences between the stages is therefore reduced. The larger the C_{S}, the better the voltage distribution of the circuit.

Short-Circuit Performance

The power MOSFET is a “unipolar” component, i.e. no minority charge carriers are required for the control process. This is a significant advantage in terms of short-circuit performance. The short-circuit current amplitude is determined exclusively by the transistor characteristic $I_{\text{D}} = f(V_{\text{DS}})$ and the gate source voltage $V_{\text{gs}}(t)$.

When referring to short-circuit resistance in the context of power semiconductors, it is always important to differentiate between two cases. In short-circuit variant Number 1, the power semiconductor is connected to a voltage source (**Figure 2a**); in short-circuit variant Number 2, a second voltage source is connected to a conducting semiconductor switch (**Figure 2b**). In the case of short-circuit variant Number 1, both the current rise and the stationary short-circuit final value are dependent on the transistor characteristics alone. The drain source voltage V_{DS} remains virtually constant during the short-circuit phase. While there is a positive di/dt value, the parasitic inductance results in a voltage dip. In contrast, the negative di/dt value results in a voltage overshoot when the short-circuit is disconnected. Depending on the size of the di/dt value and the parasitic inductance, this overvoltage amplitude can reach values which result in the destruction of the transistor. The overvoltage amplitude can be rendered harmless by means of an active protective configuration (**Figure 2a**), consisting of a serial connection of diode and Z–diode. The Z–diode must be dimensioned as follows:

$$V_{\text{B}} < V_{\text{Z}} < V_{\text{DS Breakdown}}$$

A resistance of R_{S} (R_{S} > 10 Ω) is required for this active protective configuration to be effective. If the drain source voltage exceeds the Z-diode voltage, then the FET is conductively controlled. The conductive control allows the transistor to operate within the permitted range without being damaged. This operating condition is allowed on a periodic basis.

After a specific time, $t_{\text{K}} \leq 10$ µs (**Figure 2c**), the short-circuit must be disconnected to prevent the MOSFET from being thermally destroyed. The ON-resistance of the module can be used as a short-circuit detector in a protective circuit. External intervention takes place and the MOSFET is disconnected once the short-circuit is detected.

In the case of short-circuit variant Number 2, the MOSFET is conductively controlled by means of the internal current circuit, consisting of V_{B1}, R_1 and D, and switch S_1 is only closed in a conductive state (**Figure 2b**).

When the switch closes (S_1), the drain current rises to the short-circuit value which is predetermined by the module characteristics and the gate source voltage. The MOSFET must receive the total voltage V_B during this time. The initial rate of rise for the short-circuit current is calculated as follows:

$$di/dt = \frac{V_B - V_{DS}}{L_\sigma}$$

(at the outset, $V_{DS} << V_B$).

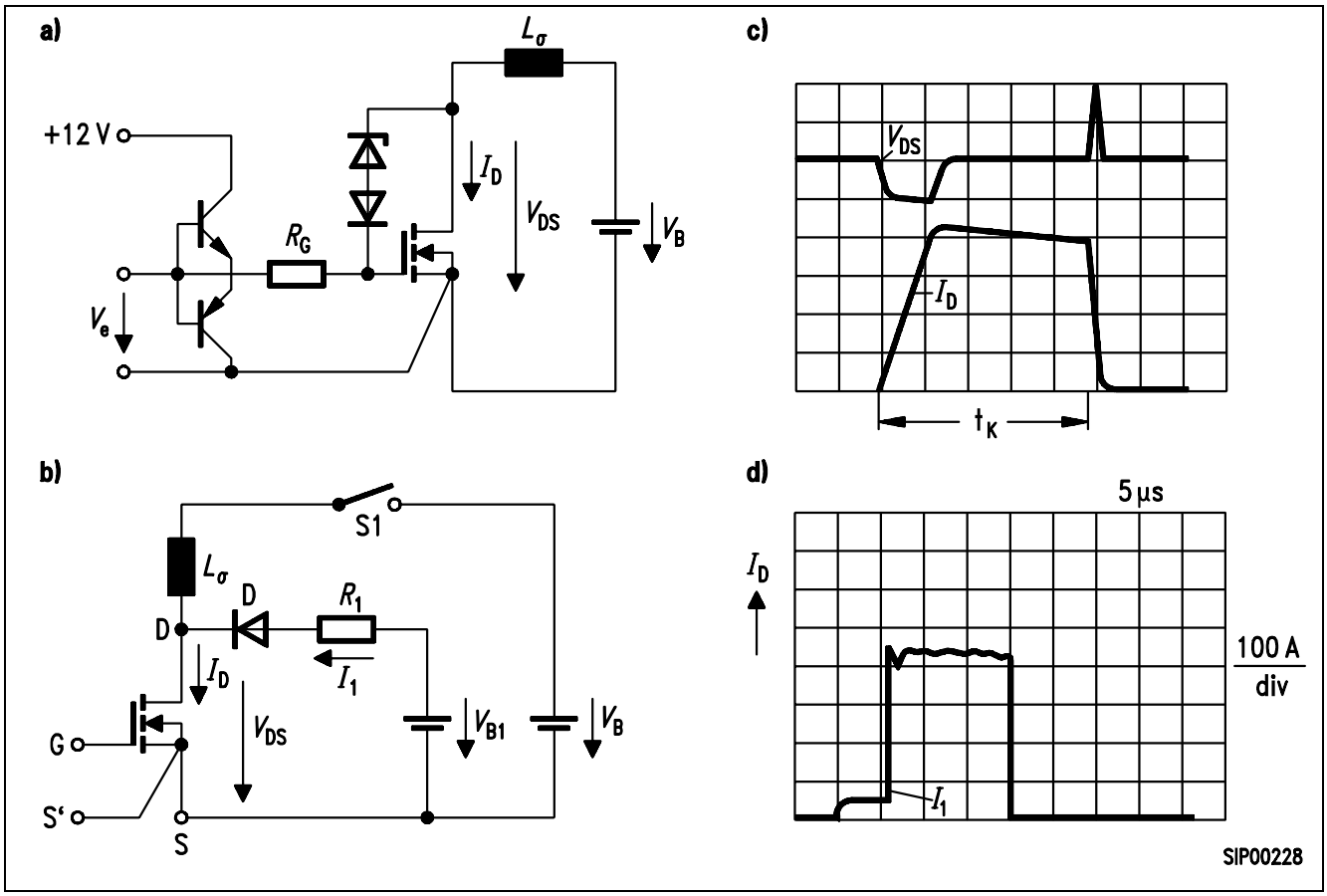

Figure 2
Short-Circuit Testing Circuit for Modules