SIEMENS

Power Transistors in SMD Packages: Calculating Power Dissipation the Right Way

More and more power transistors are being offered in surface mount variants of power packages. When calculating maximum permissible power dissipation, designers must take note of the different definitions of this parameter for SMD and power packages. When correctly calculated, the actual figure for the D-Pak (SMD variant of the TO-251 package), for example, turns out to be only slightly higher than for the SOT-223 package for SMDs.

When designing power packages, designers try to avoid hot spots in the dissipation of heat from chip to heat sink. This is done by generously dimensioning the cooling fin, which acts as a junction between the two. In the SMD variants of power packages, however, a cooling fin is of little benefit, because the circuit board (which is usually made of FR4 or epoxy material) can ultimately dissipate only a limited amount of heat (**Figure 2**). **Figure 1** lists the principal differences between the various packages.

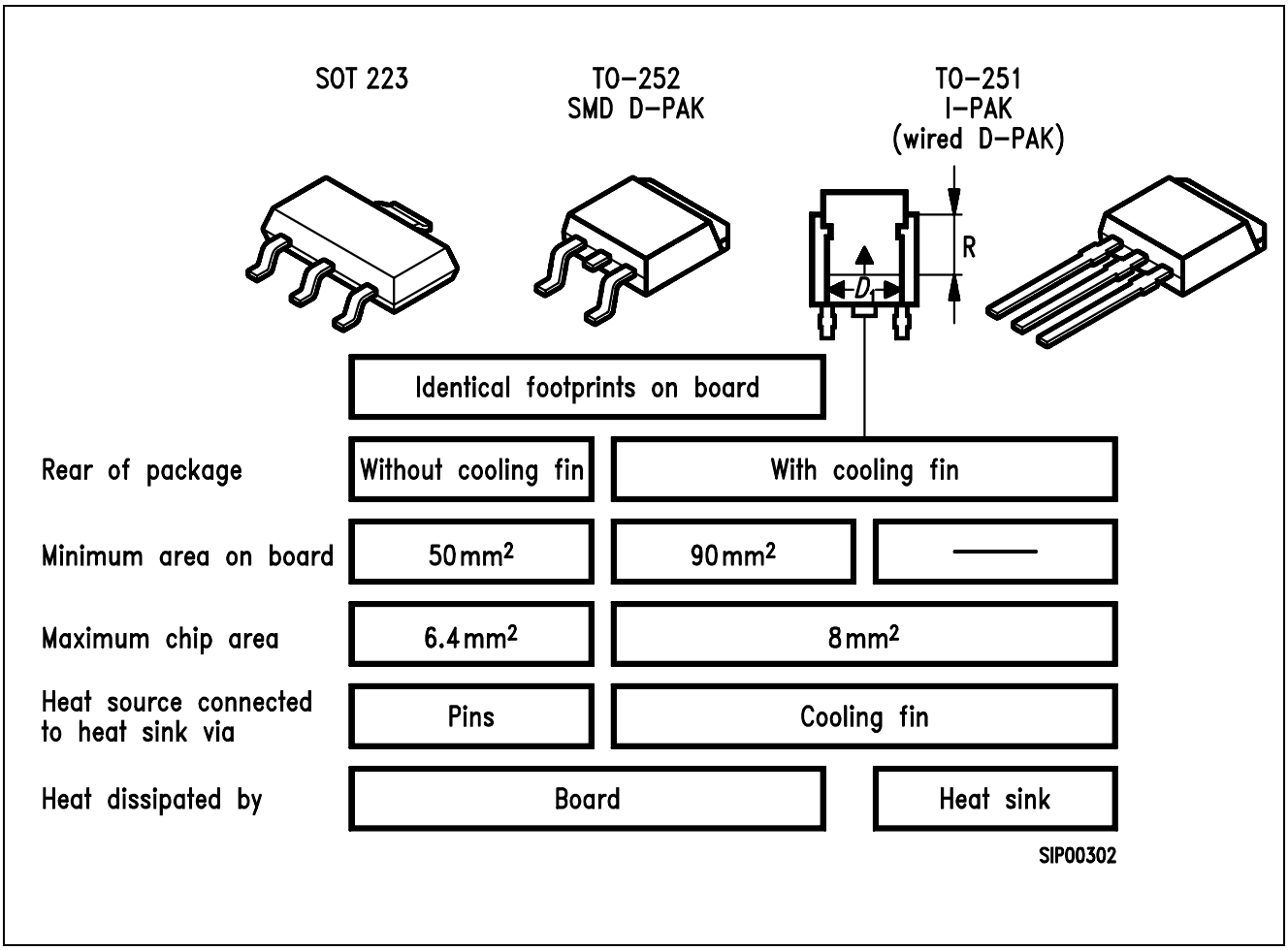

Figure 1
Comparison of Technical Data for an SMD Package, SMD Version of a Power Package, and a Wired Power Package

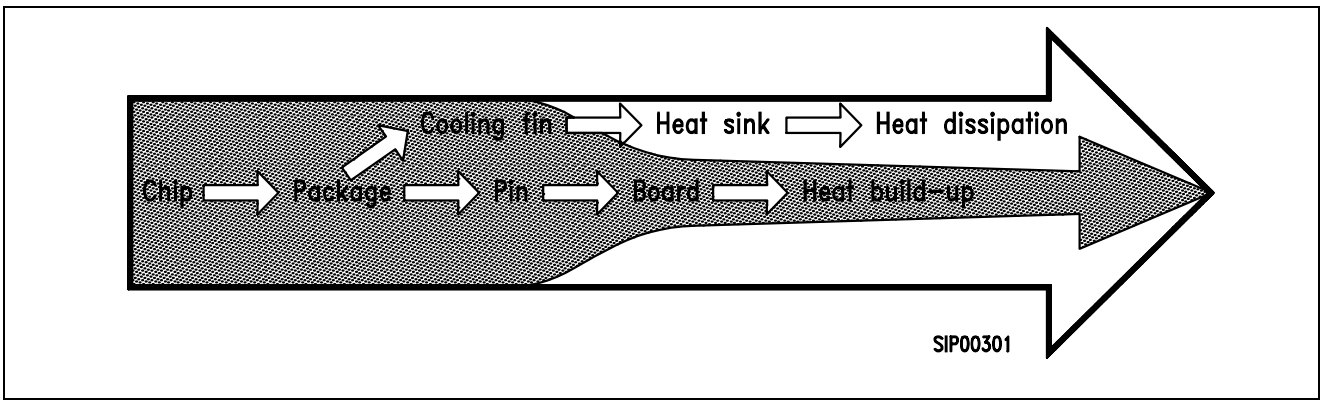

Figure 2
Whereas Heat is Dissipated in Power Transistors (Large Overall Arrow) via the Heat Sink, this is done in SMDs via the Board (thin Arrow)

Different Definitions of Power Dissipation

The quality of heat dissipation is described by the thermal resistance R_{th} and expressed in °C/W or K/W. The lower the thermal resistance, the better the heat dissipation and thus the power dissipation P_{tot}. The thermal resistance is measured between the two points where the temperature difference occurs (**Figure 3**). Depending on the application, ΔT is the difference between the junction temperature T_J and the ambient temperature T_A or case temperature T_C. In today's MOS transistors, the maximum junction temperature T_J ranges from 150 to 175 °C. Depending on the type of package, the power dissipation P_{tot} can vary by as much as 20% with otherwise identical parameters. The permissible drain current I_D is always calculated from the power dissipation P_{tot} with the following equation:

$$I_D = \sqrt{\frac{P_{tot}}{R_{DS(on)\ warm}}}$$

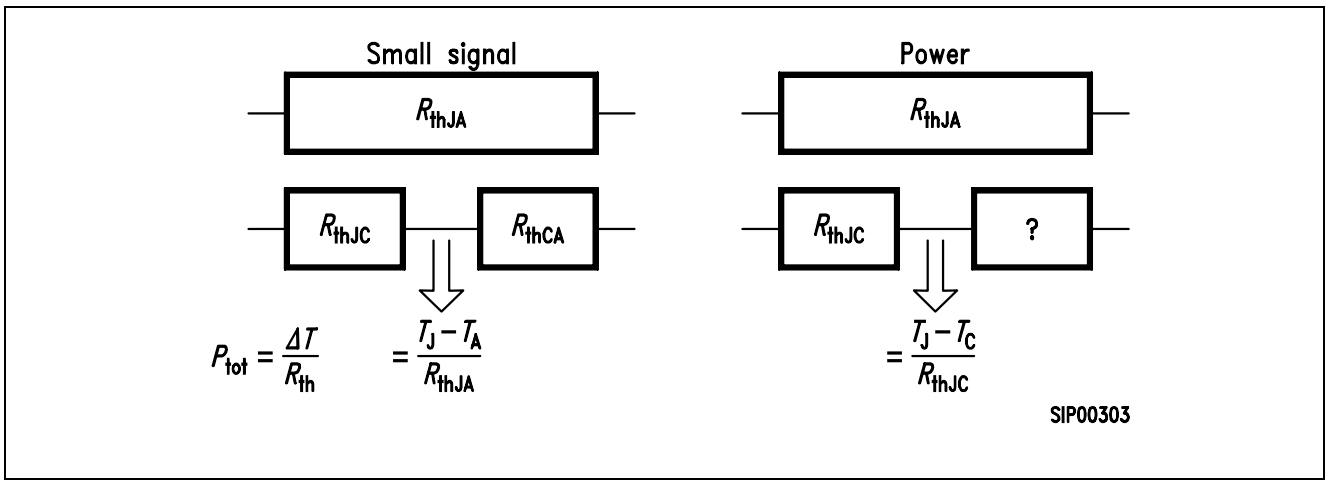

Figure 3
There are Different Definitions of Power Dissipation for Small-Signal and Power Applications

For power and small-signal transistors, there are widely varying definitions of both thermal resistance R_{th} and temperature gradient ΔT (**Table 1**).

Table 1
Depending on Application, Different Equations are Used to Calculate the Temparature Gradient and Thermal Resistance

Small-signal Application	Power Application	
	To data book	For designer
$\Delta T = T_J - T_A$ $R_{th} = R_{thJA} = R_{thJT} + R_{thTS} + R_{thSA}$ $= R_{thJS} + R_{thS}$	$\Delta T = T_J - T_C$ $R_{th} = R_{thJC}$	$\Delta T = T_J - T_A$ $R_{th} = R_{thJA} = R_{thJC} + R_{thCH} + R_{thHA}$

J: Junction; T: Carrier; S: Soldering point; A: Ambient; C: Case; H: Heatsink

SMD Transistors

In SMD transistors, the total thermal resistance is made up of the individual resistances between junction layer and carrier (R_{thJT}), between carrier and soldering point (R_{thTS}), and between soldering point and surroundings (R_{thSA}). The thermal resistance R_{thSA}, which is determined by the board, accounts for by far the largest share of overall thermal resistance. As a rule, data sheets specify the value of R_{thJS} as a function of the transistor as well as a value for R_{thJA}, but leave undefined the size and material of the board to which the latter refers. In an SOT-223 package (containing a BSP 92 transistor, for example), R_{thJS} is 9 K/W,and R_{thSA} is 63 K/W with reference to a standard epoxy board measuring 40 × 40 × 1.5 mm with a copper surface 6 mm^2 in area and 35 µm thick.

The power dissipation for an SOT-223 package can thus be defined as follows:

$$P_{tot} = \frac{150\ °C\ -\ 25\ °C}{9\ K/W\ +\ 63\ K/W} = 1.7\ W$$

Power Transistors

In power transistors, it is appropriate for data books to specify only the thermal resistance R_{thJC} between junction layer and package because the thermal resistance between the package and its surroundings depends on the choice of heat sink ($R_{thCH} – R_{thHA}$). The partial resistance R_{thCH} describes the junction resistance between the cooling fin and heat sink, R_{thHA} that between the heat sink and the surroundings. As heat is released in power transistors via the cooling fin and not via the terminal pins, C (case) instead of S (soldering point) is used as the reference parameter. Data book specifications assume that the package temperature is kept to 25 °C by external cooling so that the power dissipation of the various transistors can still be compared. Only R_{thJC}, which is approximately 3 K/W for the TO-251 and D-Pak, should then be considered. The power dissipation for a wired D-Pak can thus be defined as follows:

$$P_{tot} = \frac{150\ °C\ -\ 25\ °C}{3\ K/W\ +\ 63\ K/W} = 42\ W$$

This is, however, a hypothetical value, as a constant package temperature of 25 °C does not come near to the values prevailing in practice. To calculate total power dissipation, designers must therefore take into account either a higher package temperature or the thermal resistance of the heat sink plus junction.

SMDs in D-Paks

In addition to the wired D-Pak (TO-251), many manufacturers offer their chips in SMD versions in D-Paks. Key electrical parameters such as V_{DS}, $V_{GS(th)}$ and $R_{DS(on)}$ are thus identical in both cases. So it makes sense – and promotes clarity – to draw up just one data sheet for both versions and offer the SMD version as an option. Although manufacturers refer to the background conditions for calculation of power dissipation, joint presentation of a TO-25 with a D-Pak can easily create the impression that the latter could switch 42 W. But as the heat from an SMD is ultimately dissipated via the board, the power dissipation of the SMD D-Pak can be calculated as follows:

$$P_{tot} = \frac{150\ °C\ -\ 25\ °C}{3\ K/W} = 1.9\ W$$

This is only slightly higher than for the SOT-223 package. But the figure for permissible power dissipation P_{tot} can shift in favor of the D-Pak if the substrate resistance R_{thCA} is reduced (better heat sink). This can be obtained by using aluminum boards (thermal clads), which act as heat sinks. Their thermal resistance is significantly lower than that of epoxy boards.