SIEMENS

A Multichannel Power Switch – An Important Step in the Miniaturization of Electronic Systems

Over recent years, the planned application of IC technologies has opened up new opportunities for the development and manufacture of power semiconductors; for example, SIPMOS transistors produced using IC methods have shown themselves to be particularly outstanding as switching devices in the low-voltage field. Present-day technology in the area of chip assembly now offers plastic packages with excellent technical characteristics, high reliability and very small dimensions.

Power MOSFETs were developed as far back as the 1970s. The outstanding electrical attributes of this component are displacing bipolar transistors in many applications, and new fields of application are being opened up. The focus of further development is on reducing the on-resistance R_{DSon} and improving robustness. The particular considerations are the abilities to withstand overvoltage, dv/dt and di/dt. In the case of the new generation of SIPMOS transistors from Siemens, the resistance to excessive input circuit voltage, V_{GS}, and output circuit voltage, V_{DS}, have both been improved. In the input circuit this is due to redevelopment of the gate oxide, in the output circuit a high avalanche resistance has been achieved for low-voltage types by a homogeneous cell design and deeper diffusion of the p^+ islands. The intrinsic breakdown resistance of the transistors reduces the reverse voltage safety gap, which minimizes the static switch-on losses. As a consequence the voltage reserve for MOSFETs no longer needs to be designed for the unfavorable case of non-periodic variations in the mains voltage. As shown in **Figure 1**, during the period when it is operating in avalanche mode additional energy in the device is converted into heat.

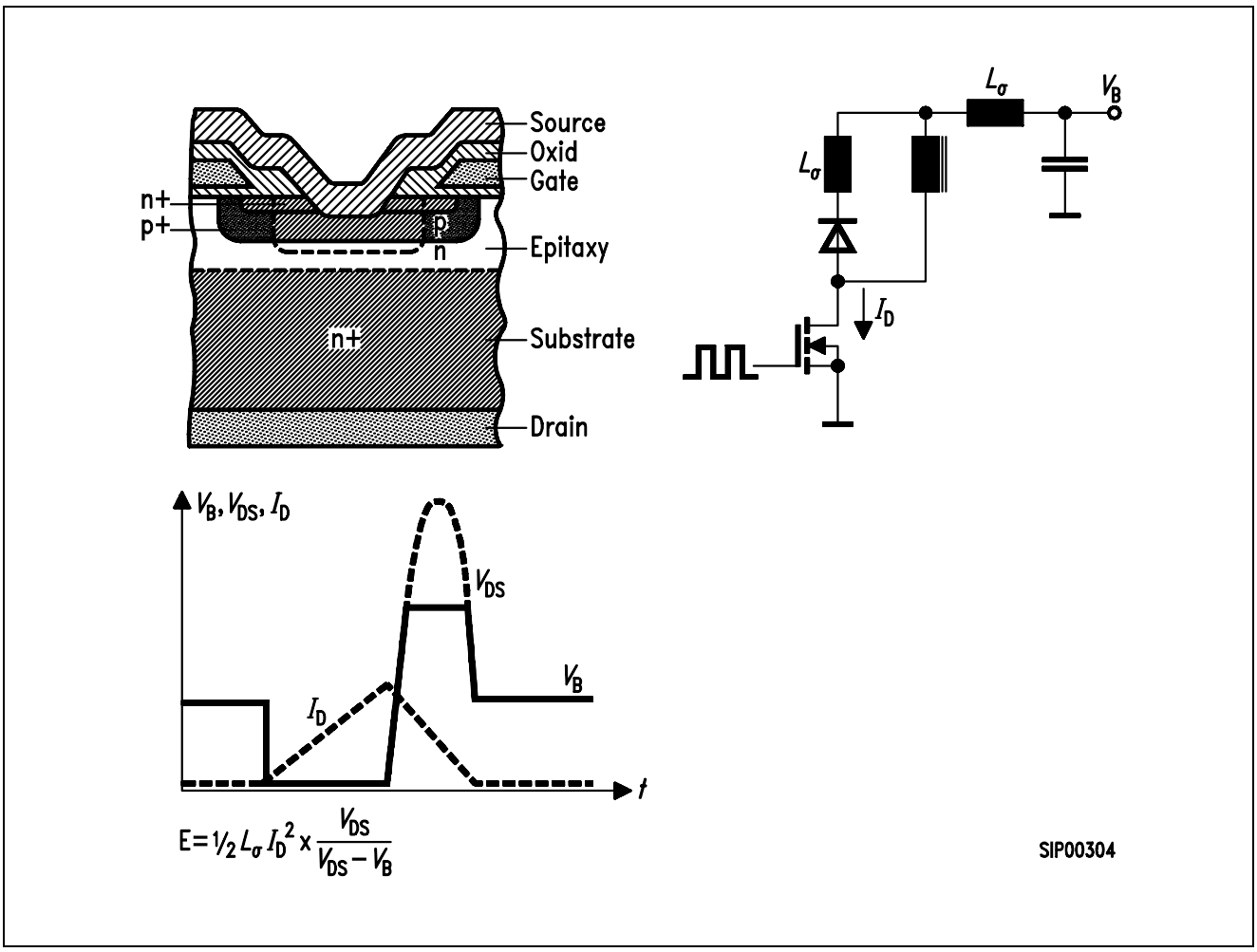

Figure 1
Cross-Section through a SIPMOS Transistor Cell (Milli-FET).
Avalanche Resistance has been Increased by a Homogeneous Cell Design and Deeper Diffusion of the p^+ Islands. While it is Operating in Avalanche Mode (due to Unclamped Wiring Inductances, L_σ) additional Energy in the Device is Converted into Heat

$$E = \frac{1}{2} L_\sigma \times I_D^{\,2} \frac{V_{DS}}{V_{DS} - V_B} \qquad \textbf{equation 1}$$

V_B = Operating voltage
V_{DS} = Breakdown voltage
L_σ = Unclamped inductance in the current circuit

Care must be taken in this operating situation to ensure that the maximum junction temperature of the transistor is not exceeded. The single pulse avalanche energy and the avalanche energy for cyclic operation are itemized in the databook. However, the avalanche resistance is only specified up to the transistor's nominal current. If the transistor is driven into voltage breakdown by a multiple of the nominal current or by a short-circuit, and is subject to a "hard" switch-off by an unclamped wiring inductance then, even if the stray

inductance is low, fault-free operation can no longer be guaranteed. In this case it is recommended that a safe operating condition is produced by means of “active Zener clamping”. In addition, the transistor may be subject to the effects of higher energy levels. Avalanche-mode lasts for such a short time (t < 1 µs) that no heat flows out of the transistor during it; the Si-chip is the heat store. The very good commutation resistance of the transistor is achieved by the completely self-adjusting cell process. This ensures that the parasitic bipolar transistor structure does not come into effect even with very short commutation processes (high values of di/dt and dv/dt).

The second focus of development work is on reducing the transistor’s on-resistance, R_{DSon}. Whereas the on-resistance is determined in the upper voltage range of 500 V ≤ V_B ≤ 1000 V mainly by the epi material (zone required for resisting the reverse voltage), in the lower voltage range (V_{Br} ≤ 60 V) the on-resistance is made up of a series of partial resistances (see **Figure 2**). Optimization of the cell design (horizontal transistor optimization) and selective development work (vertical transistor optimization) directed at milli-FETs (the present generation of transistor technology) and S-FET technology (the new generation of transistor technology) have led to the on-resistance being reduced by a factor of 6 relative to SIP-III technology (1988). This chip-development work makes it possible to realize on-resistances of R_{DSon} ≤ 8 mΩ in the TO-220 package. This enormously reduces the power loss in the transistors, permitting even power transistors to be made in SMD packages, which until now have been reserved only for ICs. Ever smaller power chips combined with low R_{DSon} values make possible multichannel transistor systems in a P-DSO package.

A New Packaging Strategy for Miniaturization

A cost-effective system solution requires the choice of power package to be carefully checked for each application. For high power loss and pulse frequencies, the classical power packages such as the TO–220 or TO–218 must be used. With these power packages, heat is transported through the cooling fins, and not via the connecting pins. With these, and depending on the heat sink, a thermal resistance of down to 1 K/W can be achieved. The smaller the thermal resistance, the better is the heat dissipation, and so much less critical is the power loss P_{tot} generated in the transistor. The following equation specifies the power loss (comprising the static, dynamic and avalanche losses) which may be produced in the transistor for a given level of cooling:

$$I^2 \times R_{DSon\,(warm)} \times D + (E_{on} + E_{off}) f_T$$

$$+\frac{1}{2} L_\sigma \times {I_D}^2 \frac{V_{DS}}{V_{DS} - V_B} f_T = \frac{T_j - T_c}{R_{thIC} + R_{thCH} + R_{thHA}} \qquad \textbf{equation 2}$$

R_{thIC} = thermal resistance between junction and package
R_{thCH} = thermal resistance between cooling fins and heat sink
R_{thHA} = thermal resistance between heat sink and ambient environment

For transistors in this package it is only meaningful to specify in the databook the thermal resistance between the junction and package, because the thermal resistance to the

environment is determined by the heat sink. For the new generation of MOSFETs, in the voltage range up to 60 V, the maximum permitted junction temperature is T_j = 175 °C.

In addition, there is an increasing number of applications in the fields of vehicle electronics, telecommunications and computers, in which chip-on-board applications or multichip modules in SM format are becoming more important. In all these applications, the maximum power loss must be limited, and ventilation foregone. Low resistance power MOSFETs in SM-compatible multichip packages present themselves as a cost-effective solution. For the application engineer this produces many advantages:

- reduced power loss from lower-impedance chips,
- lower system costs from SM assembly of multi-channel transistors and high packing density,
- less cooling cost and weight,
- higher reliability from automated handling of SM components,
- increase in the current range or reduction of the on-resistance, and correspondingly power loss, through parallel connection of the individual channels,
- miniaturization of the system integration

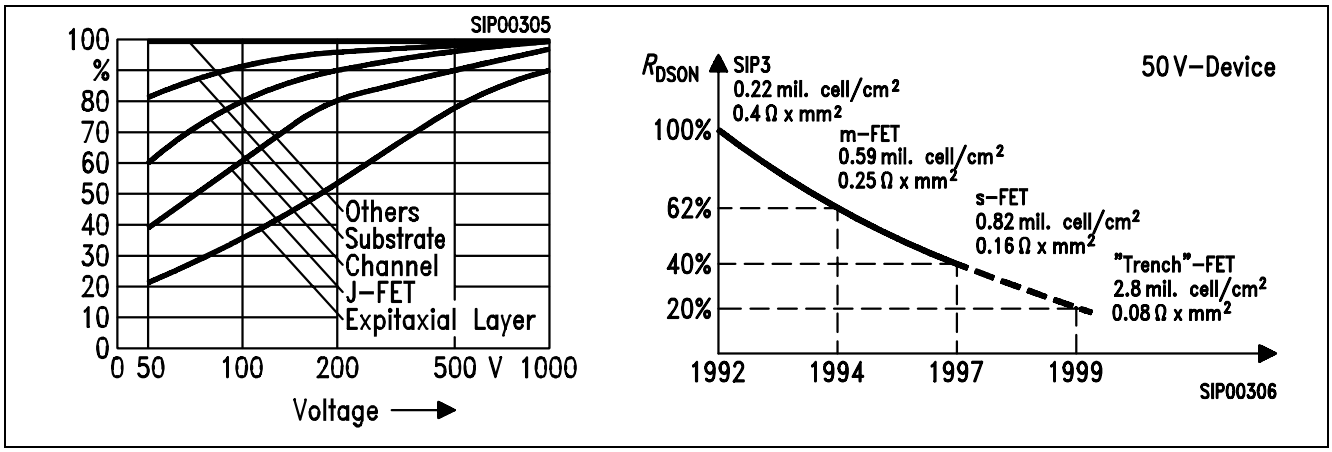

Figure 2
Showing how the Partial Resistances for a SIPMOS Transistor in SIP-III Technology (1992) Vary with Increasing Voltage
New Technologies Reduce R_{DSon} down to 0.08 Ω mm²

Optimizing the system solution in terms of costs, weight, volume, efficiency and reliability can require the use of a low-resistance switch. Although this has a greater area of silicon, making it initially expensive as an individual component, the additional system costs – such as cooling and efficiency – drop. For applications requiring minimal power loss (because it cannot be conducted away – e.g. in enclosed housings or with very high packing densities) a low-resistance power switch is the only solution. But even for electronic systems where such rigorous requirements do not apply, the low-resistance power switch may be entirely logical and may reduce system costs. Nowadays, the power loss produced in many devices is rated in DM per Watt. Generally this results in a better ratio for the low-resistance power switch. Regardless of this, the cooling overhead should also be taken into account in considering system costs. In order to permit power switches to be soldered directly onto a p.c.b. – without

heat dissipation via a heat sink – the P-DSO-20 package was developed with multichannel transistors (**Figure 3**).

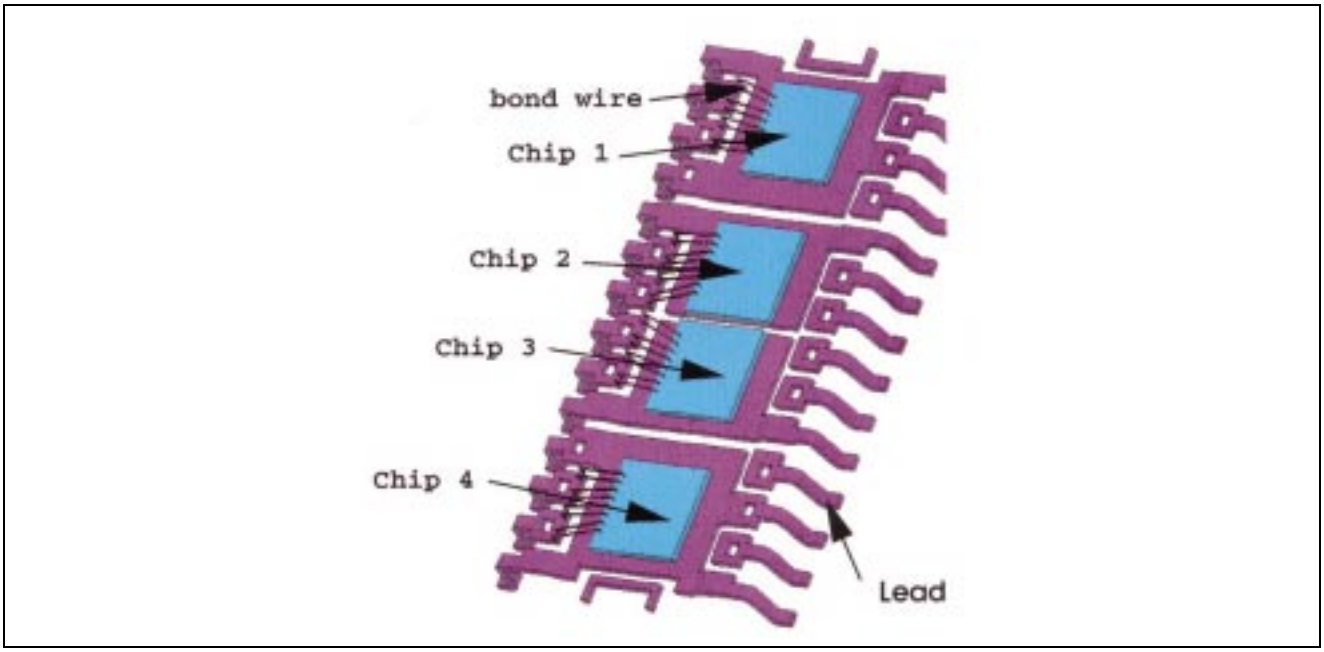

Figure 3
A 4-Channel Power MOSFET in a P-DSO-28 Package (6 cm² Cooling Surface, as a Layer on one Side) can be Soldered Directly to the P.C.B. without a Heat Sink

When mounted on a p.c.b. this package exhibits the same electronic characteristics as pure power packages, but has heating characteristics which are adequate for the intended power range. These SM-standard SO packages can be used for single- or double-sided insertion using standard assembly technology, and can be processed by reflow or a flow-soldering bath. The essential difference between the SO packages and the classical power packages is that they have no exposed copper area, but this offers no advantage in terms of the thermal resistance R_{th} when mounted on a p.c.b. The copper block only provides any heat capacity for periods of milliseconds, to absorb brief power spikes.

Thermal Considerations for the P-DSO Package

The operational dependability and life of electronic components and modules depend critically on their thermal loading. For this reason it is important to have an adequate knowledge of the thermal load on a component in the system environment, and its thermal equivalent circuit.

In the case of a standard P-DSO package with conventional leadframes, the silicon chip and the bondpads are surrounded by the molding material, and is connected to the connecting pins by bond wires (see **Figure 4a**). The power loss injected into the chip distributes itself throughout the package and the p.c.b. by conduction, and is dissipated into the environment by radiation and convection. In this situation, typical coefficients of thermal conductivity for common molding materials are R = 70 to 100 K/W. This value depends on the value of the thermal conductivity for the molding material (λ = 0.6 W/mK for common materials and λ = 2 W/mK for highly conductive ones). The modified P-DSO-28 package brings dramatic improvements in heat conduction (**Figure 4b**). In this design, the chip is connected to the leadframe, so that the main heat flow is through the connecting pins. This allows heat conduction values of R_{thJA} = 10 to 60 K/W to be achieved, depending on the p.c.b. mounting used.

In the case of the classical power package, TO-220-SMD, shown in **Figure 4c**, the heat flow is mainly via the cooling fins. For this package the only data that can reasonably be specified in the databooks is the thermal resistance between the junction and the package (R_{thJC}), because the thermal resistance from the package to the environment is determined by the choice of heat sink ($R_{thCH} – R_{thHA}$). The partial resistance R_{thCH} specifies the transfer resistance between the cooling fins and the heat sink, R_{thHA} that between the heat sink and the environment. Because the heat transport for power transistors in a classical power package is via the cooling fins and not the connecting pins, the reference point used is C (case), and not S (soldering point). When there are high power losss, e.g. at high currents or high pulse frequencies, power packages as shown in **Figure 4c** are a cost-effective solution provided that the heat developed can be conducted away via an appropriately optimized heat sink.

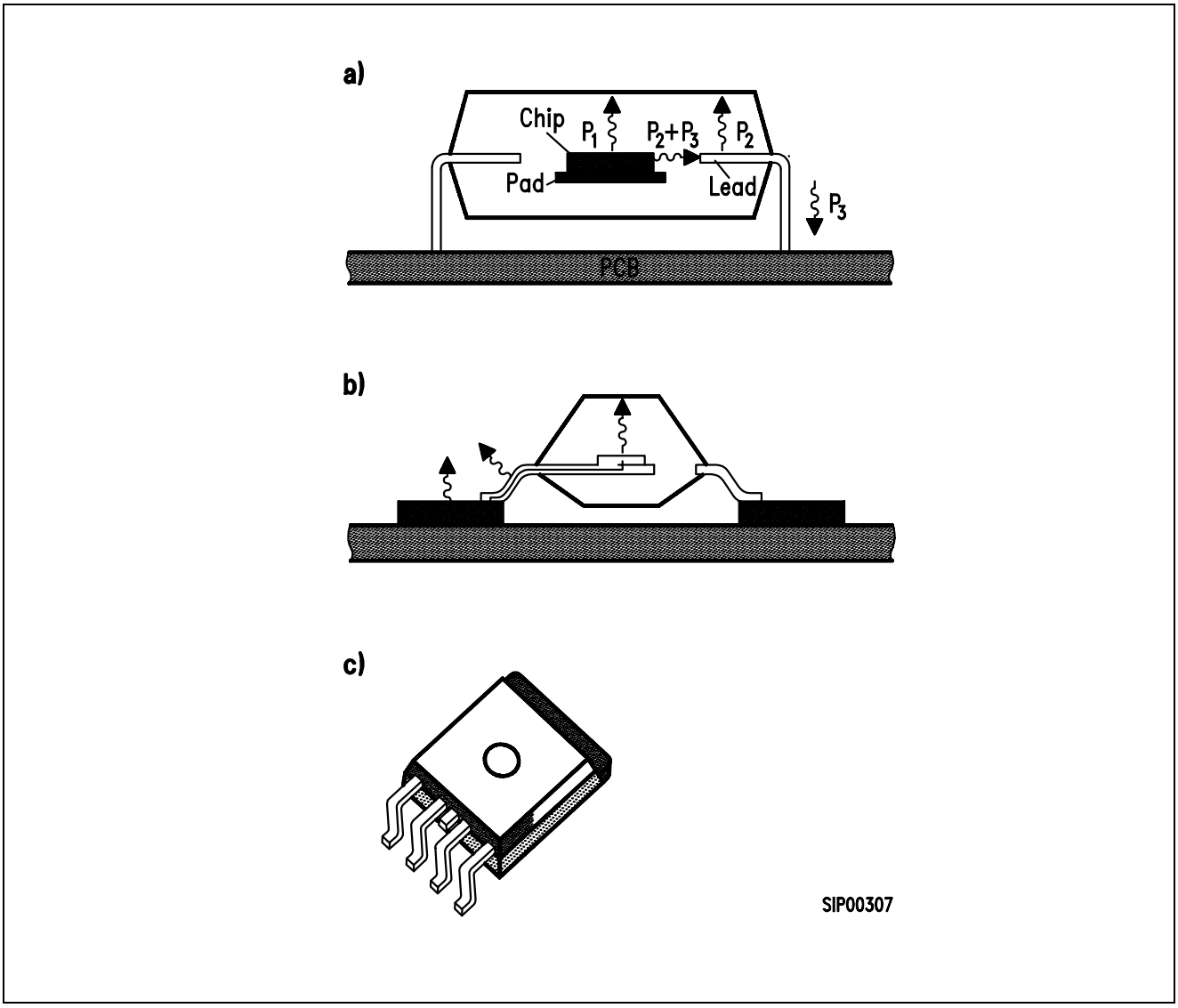

Figure 4
Schematic Structure of Various Plastic Packages

Dissipation of the heat from the semiconductor package to the environment becomes ever more difficult with increasing miniaturization and power density on the chip. If the dimensions of the semiconductor package become smaller without an accompanying change in the technology, then the thermal resistance R_{th} (heat transfer from the chip to the environment) increases. In order to dissipate exactly the same amount of heat with a smaller package, appropriate technology must be developed. One requirement is a good knowledge of the relationships for heat transfer from the chip to the environment.

If a power P is generated in the chip, then a thermal flux of Θ flows from the chip to the colder environment. In the balanced state (constant temperature difference, ΔT), the power is equal to the heat flux, and the definition of the thermal resistance is completely analogous to that of electrical resistance: $R_{th} = \Delta T/P$. According to this, at constant power the resulting temperature difference will be higher the greater is the thermal resistance. The objective is thus to minimize the thermal resistance. A semiconductor package can be regarded as a network of many individual thermal resistances, which in total form an overall resistance down to the environmental temperature T_A (ambient). Here, the overall resistance is calculated analogously to the equations applying in electrical theory for parallel and series circuits ($R = R_{th}$, $\Delta V = \Delta T$ and $P = I$). The thermal characteristics of a semiconductor package are frequently specified by the thermal resistance R_{thJA} (junction to ambient). This relates to the difference between the maximum junction temperature and the environment (ambient) temperature. This environment-related thermal resistance serves to characterize a package on a p.c.b. with no additional cooling measures. Heat is transferred from the package and p.c.b. to the environment by convection and thermal radiation.

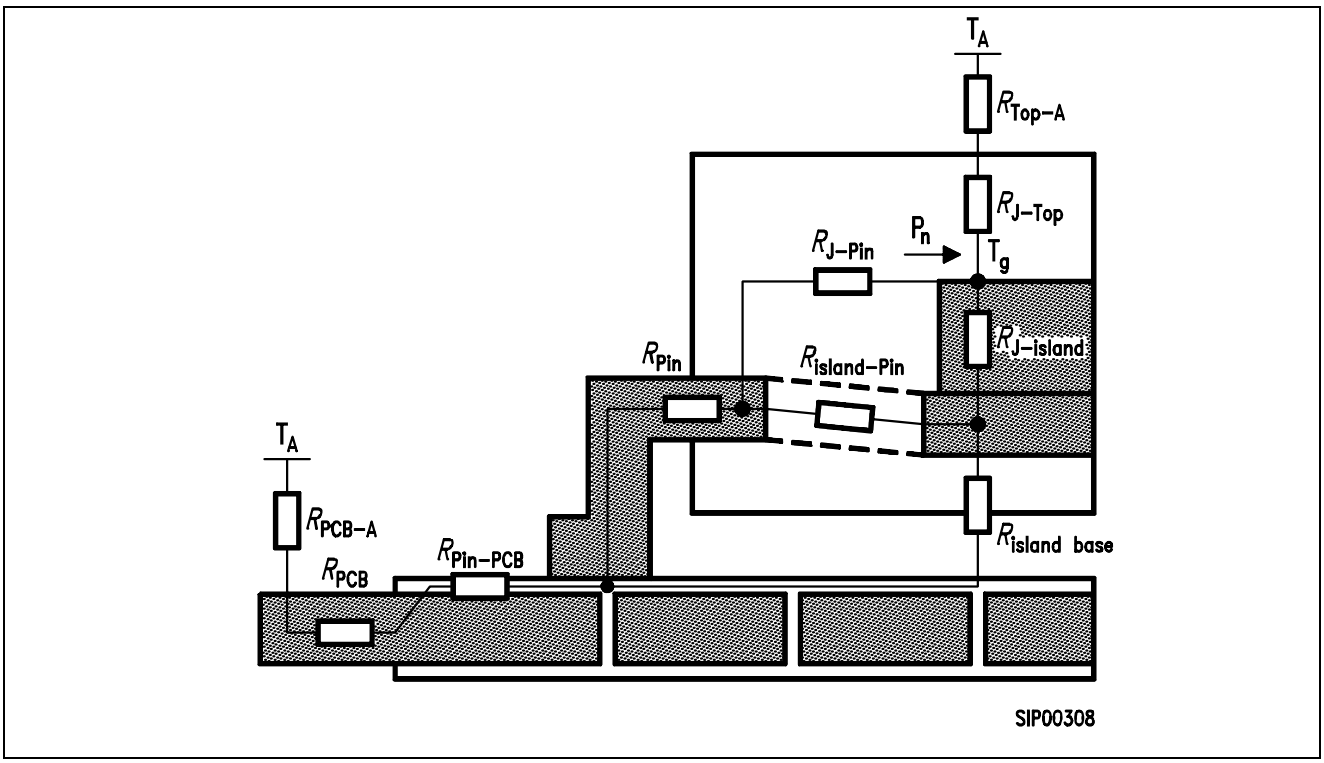

Figure 5
Equivalent Circuit Diagram of the Thermal Resistances for a P-DSO Package
The Majority of the Heat flows out of the Chip via the Island ($R_{\text{Island-Pin}}$), and is Dissipated to the Environment by the P.C.B.

For an understanding of heat transfer from the semiconductor package it is important to introduce a simple equivalent circuit. This must describe the basic effect of the individual characteristics of the package on the total thermal resistance. In addition, it is important to know the material variables which describe the heat transfer. For static considerations, the thermal conductivity (W/mK) of the material used is sufficient for this purpose.

Table 1

Material	Chip	Lead	Bond	Molding Material	Adhesive	Track Conductor	PCB
W/mK	140	270	310	0.62	1.25	380	0.3

Heat Flow in the P-DSO Package

Figure 5 shows a detailed thermal equivalent circuit diagram, with the thermal partial resistances. The power loss is generated in the upper thin layers of the chip, from where it is transferred to the body of the chip. Depending on the thermal conductivity of the molding material and the size of the package, a certain proportion of it flows through the molding material ($R_{\text{J-Top}}$) to the upper surface of the package, from where it is dissipated to the ambient environment by convection and radiation ($R_{\text{Top-A}}$). If the package is bonded to a p.c.b., then by far the greatest proportion of the heat flows through the chip and the adhesive bond ($R_{\text{J-Island}}$) to the island. In the case of the modified P-DSO package, the lead and the island have a high thermal conductivity. A small proportion of the heat is given up to the top side of the p.c.b. via the molding material and the air gap ($R_{\text{Island-Base}}$). However, by far the greatest proportion of the heat is transferred from the island to the connecting pins ($R_{\text{Island-Pin}}$). This resistance is greatly reduced if there are 'massive' island-lead connections, i.e. they have good thermal conductivity. A significantly smaller proportion of the heat is also transferred directly from the chip to the pins ($R_{\text{J-Pin}}$) via the molding material. The pins then conduct the heat to the p.c.b. (R_{pin}).

Heat conduction in the p.c.b. is very greatly affected by the fractions of its surface which are conducting tracks and cooling surfaces. The conducting tracks and cooling surfaces have a thermal conductivity which is greater than that of the p.c.b. by a factor of around 1000. The conducting tracks and cooling surfaces distribute the heat to the p.c.b. ($R_{\text{Pin-PCB}}$). Heat is dissipated from the p.c.b. to the ambient environment by radiation and convection ($R_{\text{PCB-A}}$). If the p.c.b. is attached to a heat sink, then the majority of the heat flows directly to this heat sink, and the thermal resistance ($R_{\text{PCB-A}}$) is significantly reduced.

Figure 6 shows the thermal resistance of the P-DSO package mounted on a p.c.b. for different versions of the package and layout. The left-hand region is for a standard P-DSO package as shown in **Figure 4a**. In this case, the package is mounted on a p.c.b. and there are no pad-lead connections. Here, the thermal resistance is higher by a factor of almost 2 than for the modified packages. The second region relates to a modified P-DSO package (see **Figure 4b**) on a standard p.c.b. with copper (Cu) areas of various sizes (up to 6 cm^2) as cooling surfaces. It can be clearly seen that as the Cu area gets larger the thermal resistance drops. With a 6 cm^2 Cu area, and power distributed across four transistors in the package with a total power of 2 W, R_{thJA} drops to 40 K/W; if the p.c.b. has a copper layer on both sides, an improvement to 33 K/W can be achieved. **Figure 7a** shows the temperature profile for a 6 cm^2 copper layer on one side. The total power loss is distributed across four transistors. The maximum chip temperature and greatest heat densities arise in the center of the P-DSO package, because there the chips have a mutual thermal interaction, and the energy is only conducted away to a limited extent via the leads. If the Cu area is kept down to the soldering areas for the leads (Cu area 2.2 cm^2), an R_{thJA} value of 45 K/W results (**Figure 7b**). With a minimum Cu area on both sides, R_{thJA} reduces to 36 K/W. A deterioration in the thermal resistance results if the power loss of P_{tot} = 2 W arises in a single chip. In this case, R_{thJA} deteriorates to 68 K/W for Cu p.c.bs. with a layer on one side and 56 K/W with a layer on both sides. The temperature profile for a one-sided layer is shown in **Figure 7c**.

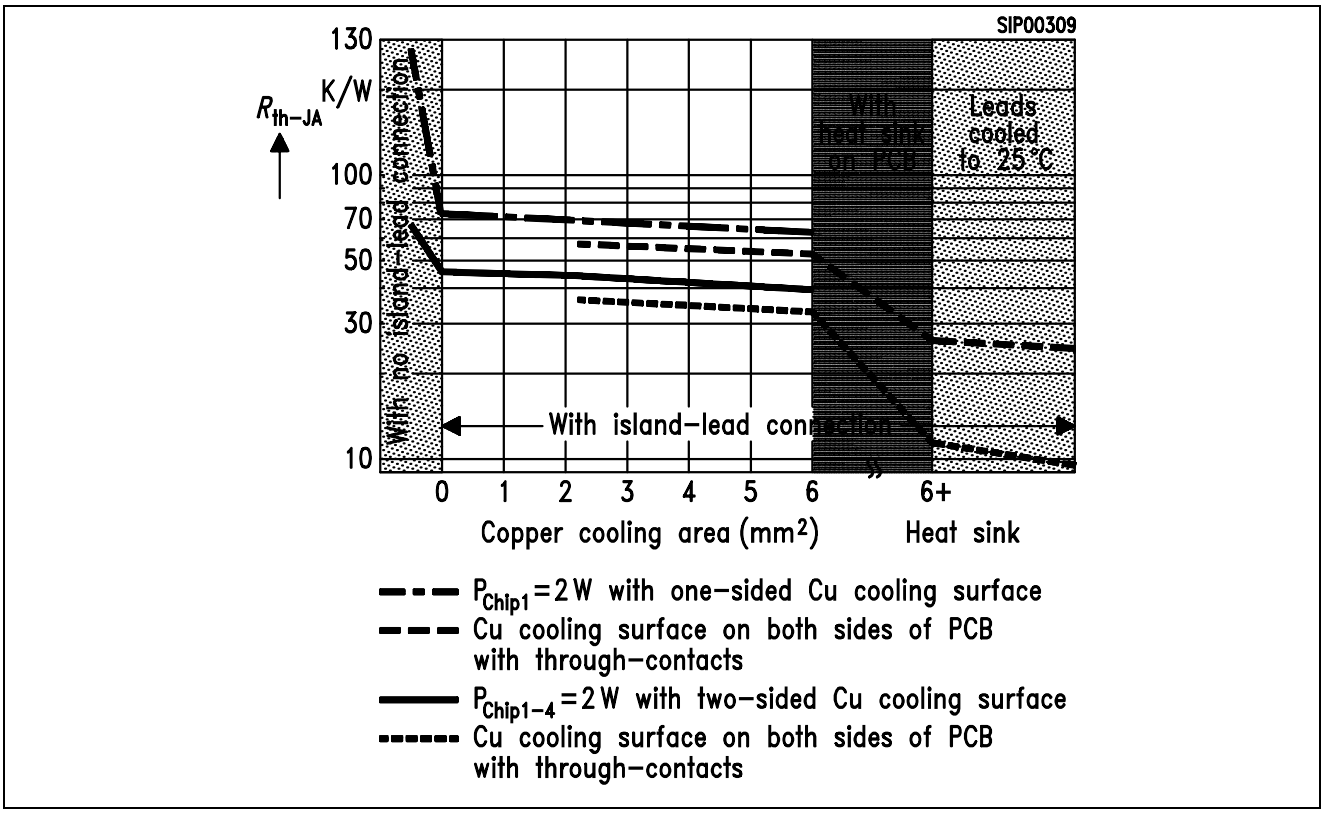

Figure 6
Showing how the Thermal Resistance for a P-DSO Package Depends on the Layout and the Power Distribution within the Package

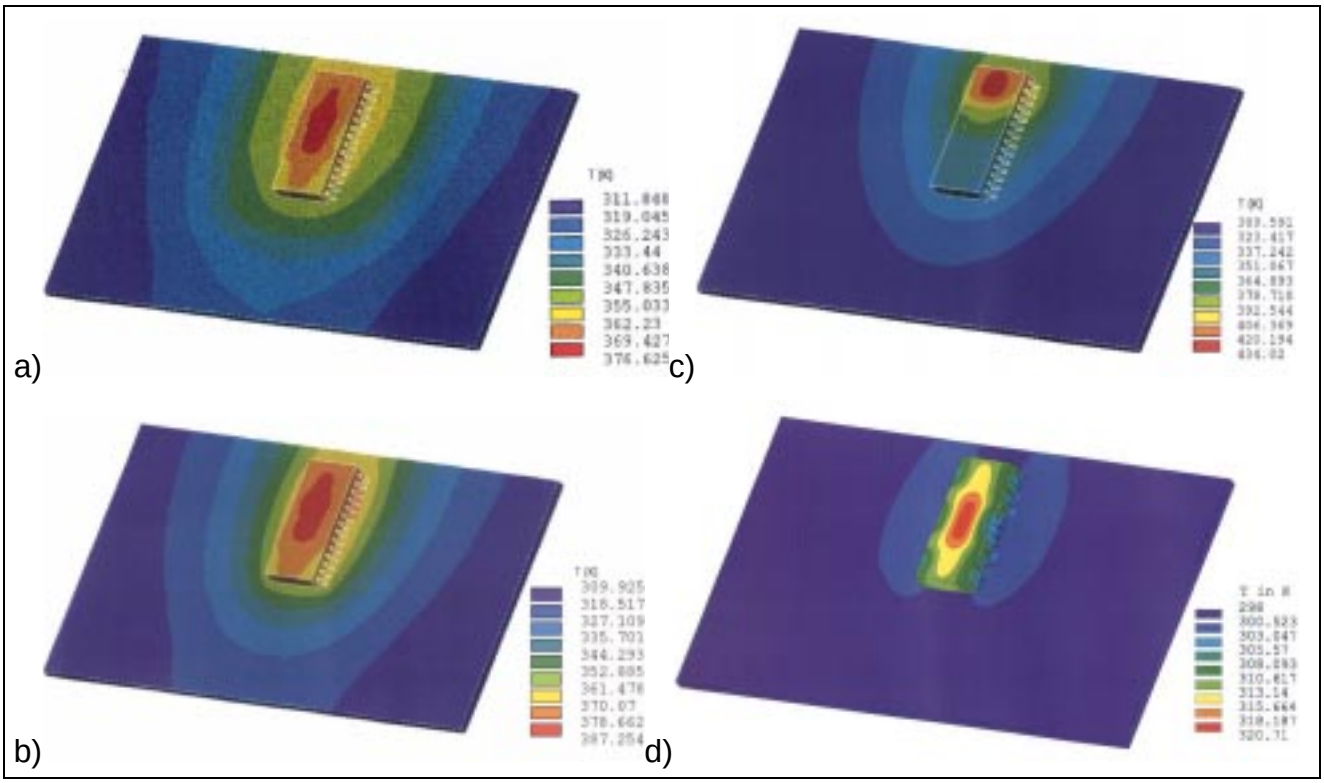

Figure 7
Temperature Profile of the Mounted P-DSO Package
Figures a) and d) refer to a 6 cm² Cu Surface on one Side,
while Figures b) and c) are for a 2.2 cm² Cu Surface on two Sides of the P.C.B.

An additional heat sink on the back of the p.c.b. improves the thermal resistance enormously (cf.**Figure 6**, regions 3 and 4). By comparison with **Figure 7a**, it reduces R_{thJA} by a factor of 3 to 12 K/W. This value can be further improved by cooled leads (25 °C). **Figure 7d** shows the temperature profile for the case of an AC heat sink which is in contact with the p.c.b. As the diagram in **Figure 6** clearly shows, the thermal resistance of the P-DSO-28 package is strongly dependent on where the power is generated in the package and how the package is mounted on the p.c.b. Taking the optimization measures into account, very good thermal values can be achieved, and hence a cost-effective solution combined with miniaturization of future electrical systems.