Short-Circuit Capability

In the case of converter switches, even the occurrence of short-circuits on the output side must not cause permanent damage to the transistors. The transistors themselves must therefore be short-circuit-proof. It must be possible at any time to handle the connection of a transistor onto a short-circuit, and the connection of a short-circuit onto a saturated transistor. Additional facilities in the power supply, or changes in the drive circuit (such as output inductances to limit control or intervention in the control circuit) are not desirable. Reduced usage of the transistors or a reduction in switching times, which lead to an increase in the dynamic losses, are not permitted.

When considering the short-circuit resistance of transistors, it is important to differentiate between the two short-circuit cases shown in **Figure 1**. The first short-circuit case, as shown in **Figure 1**, represents the connection of the transistor to a short-circuit. In this case, the rate of current increase is largely dependent on the characteristics of the transistor, the drive conditions and the stray inductance L_σ of the load circuit. The rate of rise for the IGBT is set so that the short-circuit lies in the safe range, even with the full control voltage ($V_{GE} \leq 15$ V). The transistor limits the short-circuit current, and removes the current during the time of the short-circuit due to the heating of the IGBT. Depending on the transistor characteristics and technological design, the short-circuit current may reach different current amplitude values. The short-circuit current amplitudes are adjusted by means of the reverse voltage for a given IGBT design. The short-circuit current amplitude drops as the temperature increases. The IGBTs offer excellent short-circuit characteristics across the whole voltage range (see **Figure 2**). The amplitude of the short-circuit current can easily be adjusted by the gate voltage amplitude. However, a low gate voltage causes an increase in V_{CEsat} and therefore increased forward losses. As a result of the parasitic temperature coefficients of the short-circuit current, there is no thermal “runaway”. This is also an important requirement for simple parallel switching.

In addition to the first short-circuit case described above, there is also the considerably more critical second short-circuit case, where a short-circuit is connected onto a saturated transistor. The load current flows through the transistor, and the collector-emitter voltage has taken the value V_{CEsat}. If a load short-circuit occurs at this time, then a short-circuit process is initiated which only terminates when the transistor has received the full intermediate circuit voltage. The initial rate of rise is then only determined by the stray inductance of the circuit ($\mathrm{d}i/\mathrm{d}t \approx V_Z/L_\sigma$). As soon as the short-circuit process is initiated, the voltage rises across the transistor. As a result of this voltage edge $\mathrm{d}v_{CE}/\mathrm{d}t$, a dielectric current flows over the feedback capacitance. Depending on the output impedance of the drive circuit, this dielectric current also charges the gate emitter capacitance and drives the transistor channel by means of an additional control voltage. The dynamic control voltage causes a dynamic short-circuit current amplitude which may be a multiple of the static short-circuit current, irrespective of $\mathrm{d}v_{CE}/\mathrm{d}t$ and the impedance of the drive circuit. This overcurrent amplitude can be drastically reduced if the input voltage is restricted by a Z-diode or is limited to the control voltage source.

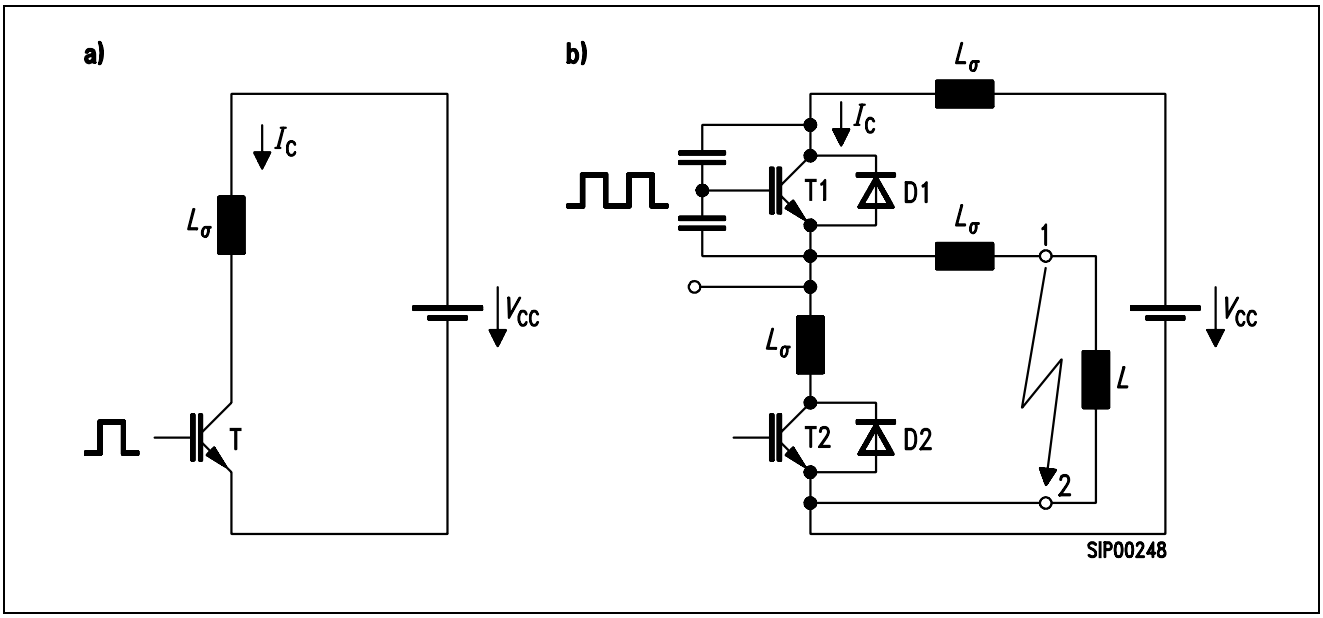

Figure 1
Different Cases of Short-circuits
a) The Transistor connected to a Short-circuit
b) A Short-circuit connected to the Conducting Transistor

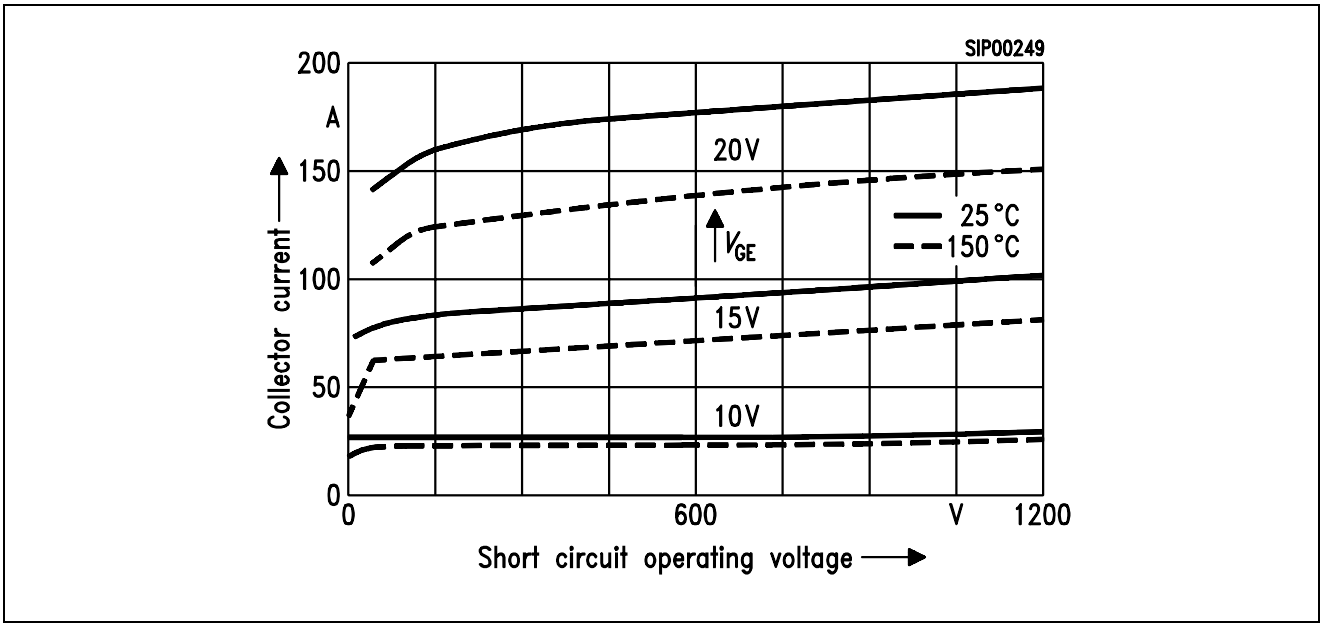

Figure 2
Short-circuit characteristics of an NPT IGBT

SOA Range and Latch-Up Effect

The latch-up effect involves connection of the parasitic thyristor structure. This results in the destruction of the IGBT, since disconnection is no longer possible. Factors affecting the threat of latch-up with a predetermined intermediate circuit voltage are the size of the drain current and the rate of voltage rise which occurs when disconnecting. This means that the greater the drain current and the faster the disconnection speed, the greater the danger of a latch-up. The injected holes flow vertically upwards (see semiconductor structure diagram for IGBTs) and reduce the resistance of the n^- area. It is important to use appropriate technology to prevent the upward flow of holes from stimulating the n^+ emitter in the source area into electron emission. In the case of NPT IGBTs, it has been demonstrated that suitable design measures can eliminate the latch-up effect across the whole of the technically affected area. As shown in **Figure 3**, the familiar rectangular SOA diagram applies with regard to short-circuit current amplitude and the full forward voltage of this semiconductor switch. The reduction of limit values as a matter of principle, by activating the parasitic npnp structure, is not necessary.

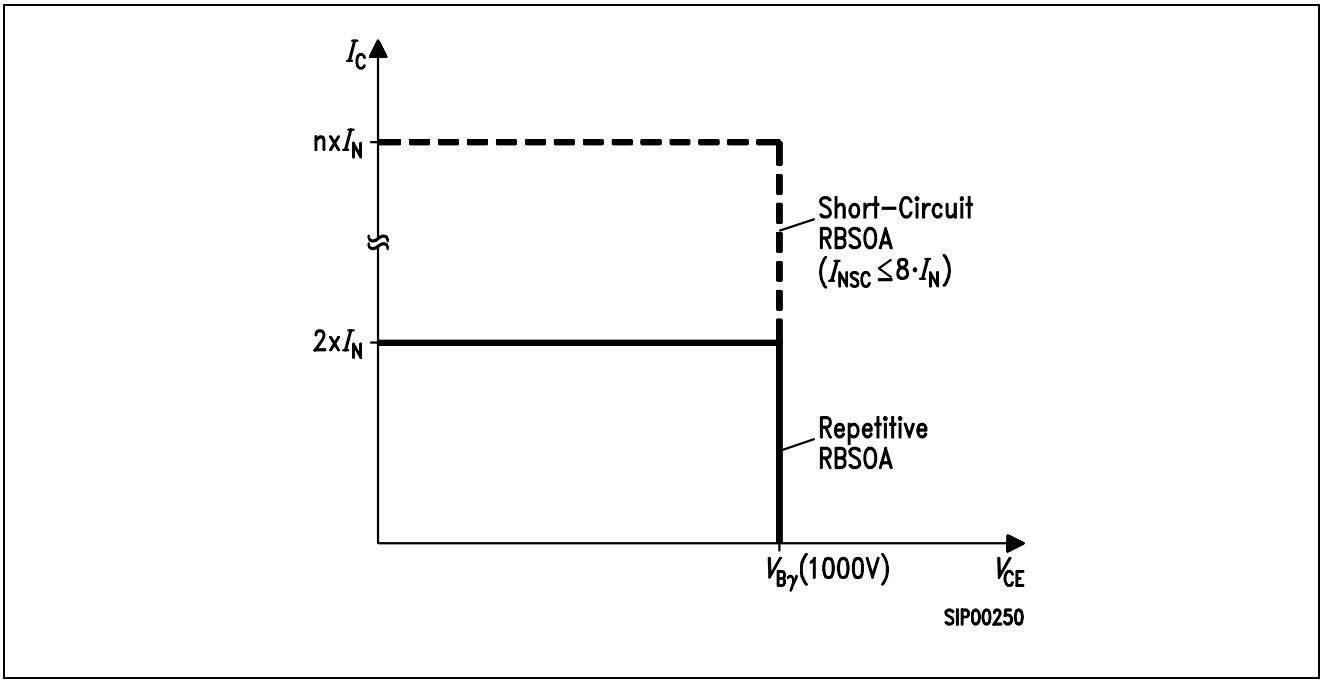

Figure 3
SOA Diagram for the NPT IGBT