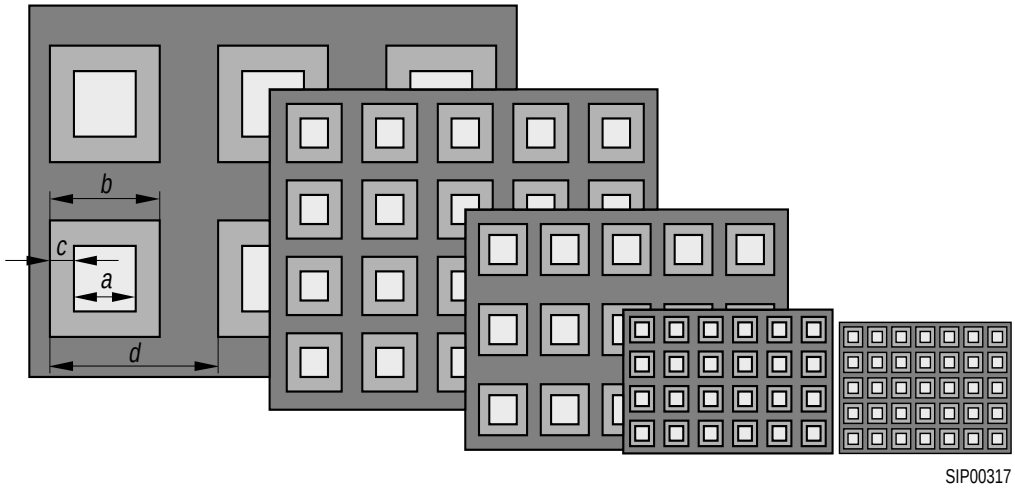
SIEMENS

Higher Cell Density, More Rugged Design

MOS-based power semiconductors in S-FET technology can switch currents from a few milliamperes up to several hundred amperes at a voltage of 55 V. Extremely short source lengths make them commutation-proof and more resistant to avalanche breakdowns. At the same time, their specific drain-source on resistance has been reduced by 25%.

With the new S-FET power transistors from Siemens, designers can implement semiconductor switches with a drain-source on resistance as low as 8 mΩ T0-220 packages (dual in-line and SMDs) and with only 40 mΩ in SOT-223 packages. S-FET transistors also feature gate drive voltages of 5 and 10 V respectively for these two package types at a drain-source breakdown voltage of 55 V, which will benefit applications in automotive and industrial electronics in particular.

The key design aims of the S-FET power transistors were minimum drain-source on resistance and maximum ruggedness. These requirements led to development of a cell concept with extremely short source lengths C between the opening of the cell and the through-plated hole (**Figure 1**). This design increases cell density and thus reduces drain-source on resistance while minimizing the base length of the parasitic bipolar transistor formed by the n-drift path, p-body region and n^+ source region (**Figure 2**). This parasitic component, which is inevitable in DMOS structures, profoundly affects the ruggedness of the transistors in terms of avalanche breakdown and commutation stability.



	SIP 1	SIP 2	SIP 3	m-FET	S-FET
$R_{DS\ (On)} \times A$ in mΩ mm^2	1000	800	380	220	165
Cell density in 10^6/cm^2	0.028	0.128	0.207	0.592	0.826
Cell Spacing (d) in µm	60	28	22	13	11
Through-plated hole opening (a) in µm	20	10	8	4	4
Cell Opening (b) in µm	40	20	14	7	5
Source Length (c) in µm	10	5	3	1.5	0.5
Year of development	1978	1985	1988	1992	1996

Figure 1
Ongoing Development of SIPMOS Power MOSFETs has Reduced Length by a Factor of 20 Over the past 15 Years

Self-Adjusting Cell Design

Based on spacer technology, the cell concept makes a planar, completely self-adjusted cell design possible for the first time ever. It is achieved by depositing a dielectric layer (BPSG) after diffusion of the source regions and then removing it again by anisotropic plasma etching. This combination of deposition and etching produces narrow, insulating side walls along the polysilicon edges known as spacers (**Figure 2**). The process is derived from the submicron CMOS technology used for LDD transistors and has been applied here to fabricate power MOSFETs for the first time. It allows the source length to be shortened by two-thirds from 1.5 to 0.5 µm, considerably reducing the gain of the parasitic bipolar transistor and substantially improving the ruggedness of the semiconductor switch.

In addition, the cell pitch has been reduced from the 13 µm common in m-FET technology to 11 µm. The resulting cell density – 830,000 instead of 590,000 cells per square centimeter –

is 40% higher. Simultaneous reduction of the effective channel length and optimization of the epitaxial layer reduce the maximum specific drain-source on resistance by 25% altogether, from 220 to 165 mΩ per mm^2 at a real gate source voltage of 7 V.

The real drain source on resistance of power DMOS transistors depends on other factors as well as technology data (**Figure 3**). The source wire resistances have reduced from a total of 1.2 to 0.7 mΩ thanks to improved, integrated assembly on a linked power line (LPL). The LPL concept also sets a new milestone in production quality (AOQ < 1 dpm). With their consistently high quality and particularly rugged chip technology, S-FET power switches can be used under the extreme conditions of automotive applications, for example.

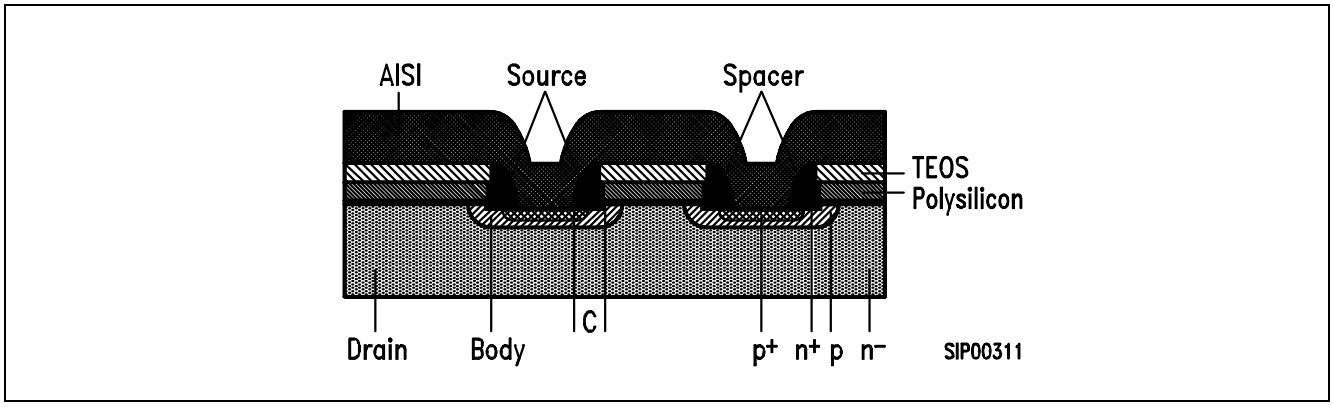


Figure 2
The Spacer has Significantly Improved the Ruggedness of S-FET Components

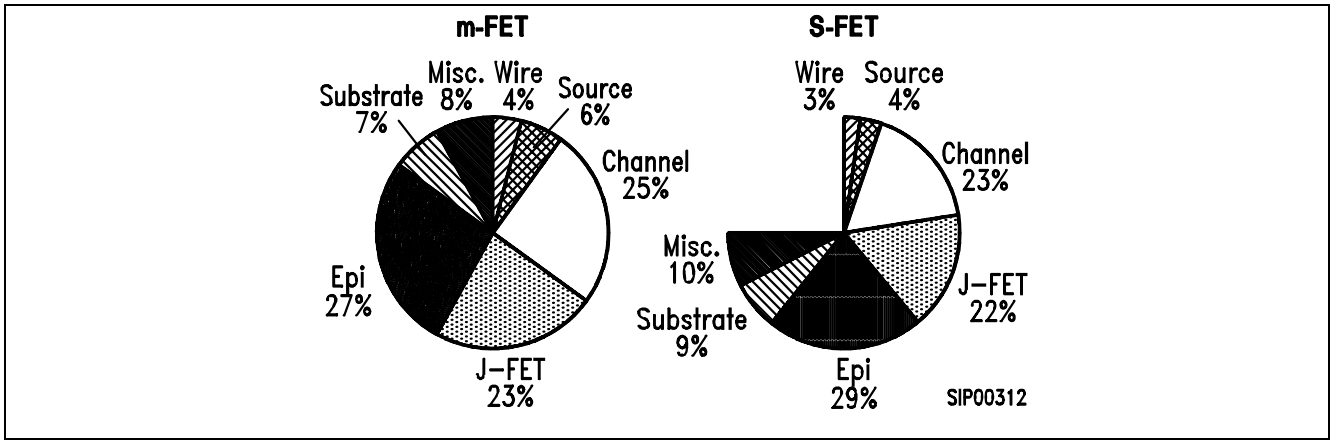


Figure 3
Breakdown of Resistance in M-FET and S-FET Technologies

S-FET Properties At a Glance

- The breakdown voltage has been raised from 50 V at – 40 °C to 50 V at – 55 °C (equivalent to 55 V at 25 °C) to ensure an adequate voltage reserve in the application and optimum drain-source on resistance with good CPK values. The new, more rugged process has also improved avalanche stability considerably.
- Switching times are largely determined by the input capacitance C_{iss} and reverse transfer capacitance C_{rss}. With the new cell design, a lower input capacitance can be obtained despite the higher cell density, which considerably reduces switching times.
- The smaller chip area is also reflected in higher thermal resistance This results in lower maximum power dissipation and thus lower current handling capacity (**Figure 4**).
- Since the introduction of the SIPMOS improvement program, chip thickness has now been reduced from 525 to 220 µm, thus improving both the reliability (HTRB,H3TRB, HTGS > 2000 h) and thermal resistance of the component.
- Although the operating voltage window still extends from 2.1 to 4 V at the standard level and 1.2 to 2 V at the logic level, it is no longer specified at 1 mA, but at 90 µA for the BUZ 102SL, for example. This means that at a gate-source voltage of 3 V, a current of only 90 µA flows instead of 1 mA previously. This improves operational reliabitity in the application so that the component remains safely turned off even at residual driver voltages V_{GS} of less than 0.8 V. An S-FET power transistor in a TO-220 package and with a drain-source on resistance of only 8 mΩ can thus switch currents up to 125 A. In many applications (e.g. ABS), connection of several FETs in parallel can thus be avoided.

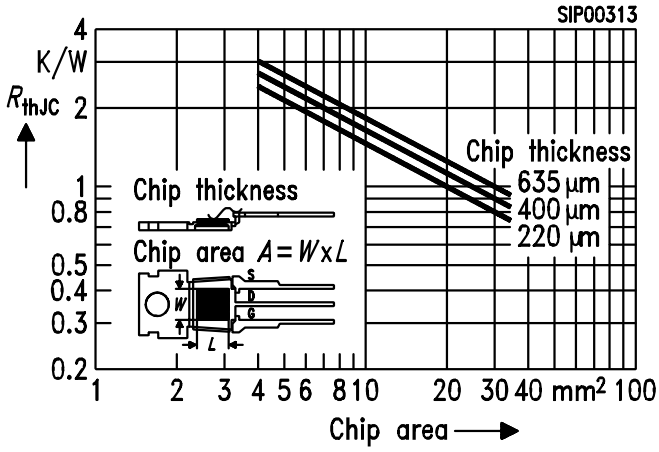


Figure 4
Influence of Chip Area on Thermal Resistance

Thanks to S-FET technology, quad switches (BUZ 103-4) capable of handling up to 5 A per channel can now be offered in P-DSO-28 packages as well. Prospective applications are DC/DC converters. step-down converters (**Figure 5**), battery management, stepper motor controllers, ABS valves, etc.

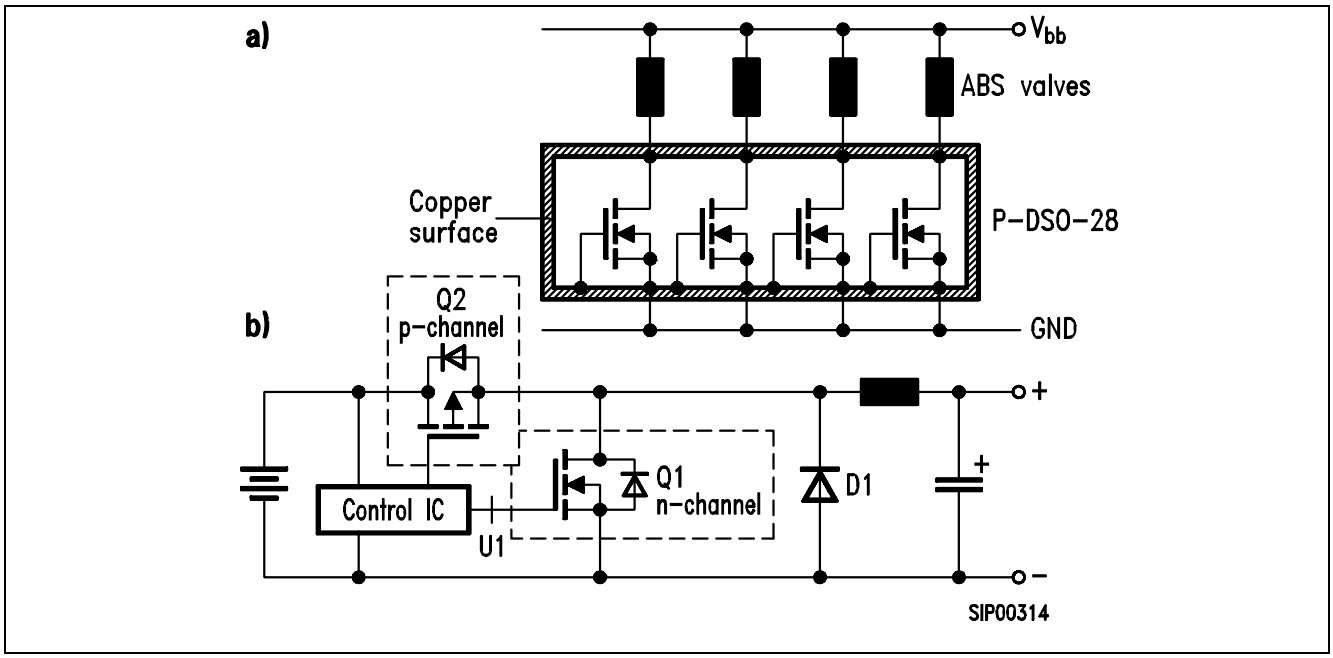


Figure 5
S-FETs Simplify Circuit Design for many Applications, especially in the Automative Sector
a) ABS Circuit with Quad Switch in P-DSO-28 Package
b) Basic Circuit for Step-down Converter

New Packages, More Miniaturization

Parallel to the introduction of 55 V MOSFETs, develepment aktivities are under way to extend S-FET technology to the 20-30 V range. Principal applications for such 30 V power transistors will be found in telecommunications and data processing. In packaging technology, there is a distinct trend toward a higher degree of automation for production of packages at lower cost and with more compact dimensions.

A new family of multichannel switches in P-DS0-28 packages (two and four-channel versions) will soon be launched. A higher level of system integration with multichannel transistors will offer users numerous benefits, such as greater miniaturization, higher packaging density and more flexible circuit design. The product range covers 55 V, 100 V and 200 V transistors capable of switching currents from 1 to 6 A. In addition, power MOSFETs in D-packages will be available from mid-1997. This new package design is the ideal link between the TO-220 package for SMDs and the SOT 223 dual in-line package. Siemens plans to offer a range of S-FET power transistors which will eventually extend from 55 V to 600 V.